Data Sheet

MM32F0010

32-bit Microcontroller Based on Arm®Cortex®-M0

Revision: 1.14

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1 General Introduction

1.1 Introduction

This product is a 32-bit microcontroller using the high-performance Arm® Cortex®-M0. The highest operating frequency is up to 48MHz. It has built-in high speed memory, rich enhanced I/O ports and peripherals which are connected to the external bus. This product contains one 12-bit ADC, one 16-bit universal timer, one 16-bit basic timer and one 16-bit advanced timer. It also contains standard communication interfaces: one I2C interface, one SPI interface and two UART interfaces.

The operating voltage of this product series is 2.0V~5.5V. The operating temperature range of conventional type is -40℃~+85℃。Multiple low power modes are provided to ensure the requirements of low-power applications.

The configuration of peripherals for the product varies according to different packages.

Rich peripherals make the microcontroller suitable for a variety of applications:

- Node control
- Wireless charging
- Motor control
- Toys
- Lighting circuit
- Fire-fighting devices
- 8/16-bit MCU upgrade

This product offers three package types: QFN20, TSSOP20 and SOP8.

1.2 Product Characteristics

- Core and system
  - Arm® Cortex®-M0
  - Operating frequency up to 48MHz
  - Single cycle 32-bit hardware multiplier
- Memory
  - Flash memory up to 16K bytes
  - SRAM up to 2K bytes
- CRC computing unit
- Clock, reset, and power management
  - Power supply 2.0V ~ 5.5V
  - Power-on reset/Power down reset (POR/PDR), programmable voltage detector (PVD)
  - POR reset voltage as low as 1.7V

  - PVD voltage threshold as low as 1.8V
  - External 2~24MHz high speed crystal oscillator
  - Embedded 48 MHZ high speed oscillator with factory calibration
- Low power
  - Sleep mode, Stop mode and Standby mode
- 6 timers
  - One 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead time generation and emergency stop functions
  - One 16-bit timer providing up to 3 input captures/output compares, which can be used for IR control decoding
  - One 16-bit timer providing 1 input capture/output compare
  - Two watchdog timers (IWDG and WWDG)
  - One Systick timer: 24-bit autodecrement counter
- Up to 4 communication interfaces
  - 2 UART interfaces
  - 1 I2C interface
  - 1 SPI interface
- Up to 18 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports can input and output V_{DD} signals
- One 12-bit ADC, 1μS conversion time (up to 8 input channels)
  - Conversion range: 0~VDD
  - Support the configuration of sampling time and resolution
  - On-chip voltage sensor
- Debug mode
  - Serial wire debug (SWD)
- Adopt QFN20, TSSOP20 and SOP8 package types

2 Specification

2.1 Model List

2.1.1 Ordering Information

Table 1 Ordering information

Peripheral interface \ Model		MM32F0010A1N (V)	MM32F0010A1T (V)	MM32F0010A6T (V)
Flash memory - KB		16	16	16
SRAM - KB		2	2	2
Timer	General-purpose (16 bit)	1	1	1
	Basic	1	1	1
	Adavnced	1	1	1
Communication interface	UART	2	2	2
	I2C	1	1	1
	SPI	1	1	1
Number of GPIO		18	18	6
12 位 ADC	Number	1	1	1
	Number of channels	8	8	6
CPU frequency		48 MHz		
Working voltage		2.0V ~ 5.5V		
Working temperature		-40℃ ~ +85℃/-40℃ ~ +105℃ (V as suffix)		
Package		QFN20	TSSOP20	SOP8

2.1.2 Marking Information

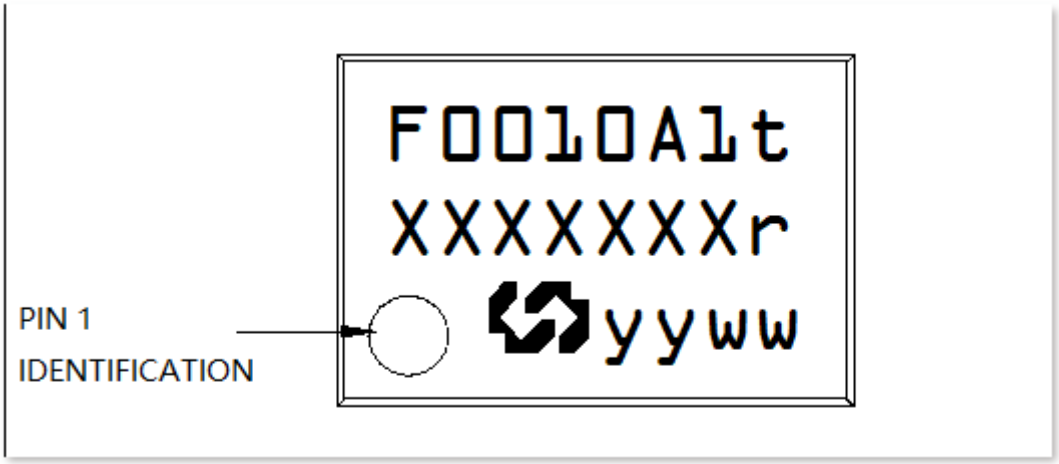

Figure 1 TSSOP20 package marking

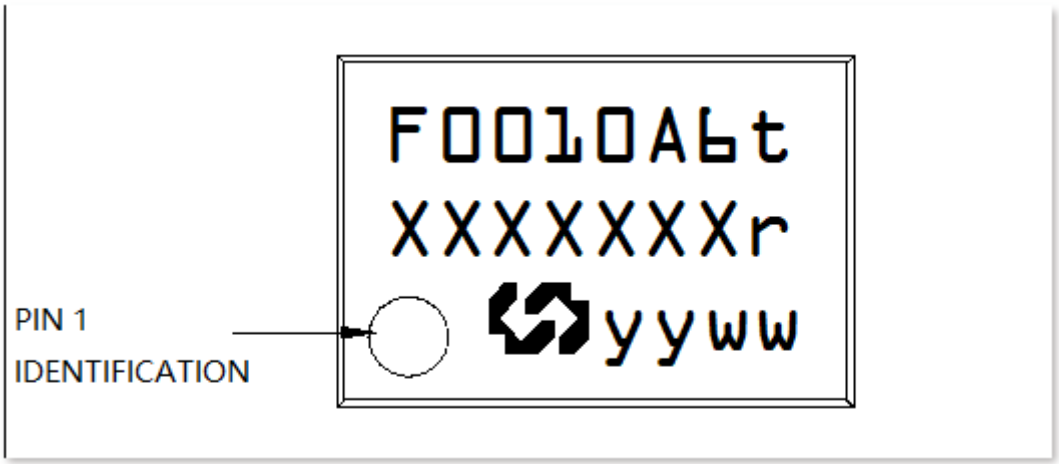

Figure 2 SOP8 package marking

TSSOP and SOP packages have the following topside marking:

- Line 1：F0010xxt
  - Product name, where “t” represents temperature level. “t” = “T” means -40 to 85°C, “t” = “V” means -40 to -105°C.
- Line 2：xxxxxxxr
  - Trace code + chip version number, where “r” represents the number of chip version
- Line 3：company logo + yyww
  - Date code, “yy” means year and “ww” means week

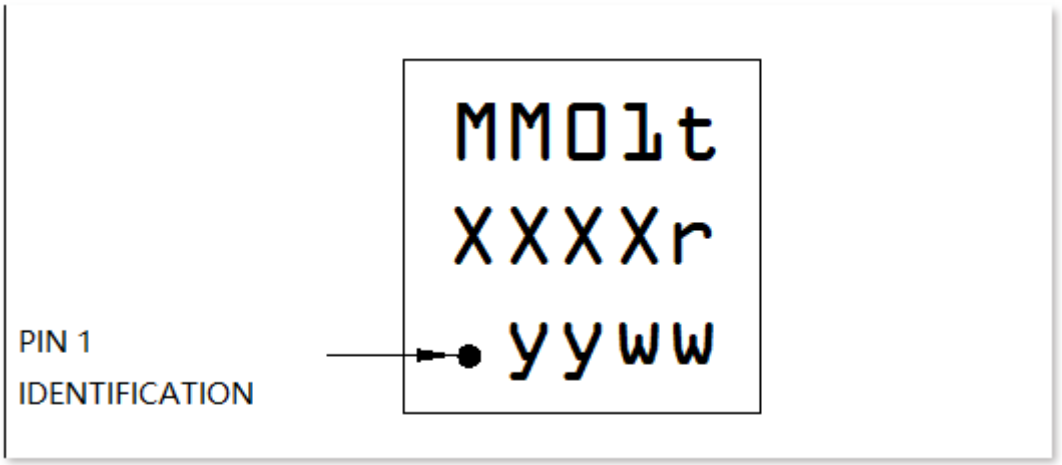

Figure 3 QFN20 package marking

QFN20 package has the following topside marking:：

- Line 1：MM01t
  - Abbreviation of the product name. “MM01” means QFN20 package of MM32F0010 series, where “t” represents temperature level. “t” = (N) means -40 to 85°C, “t” = “V” means -40 to -105°C.
- Line 2：xxxxxxxr
  - Trace code + chip version number, where “r” represents the number of chip version
- Line 3：company logo + yyww
  - Date code, “yy” means year and “ww” means week

2.1.3 Block Diagram

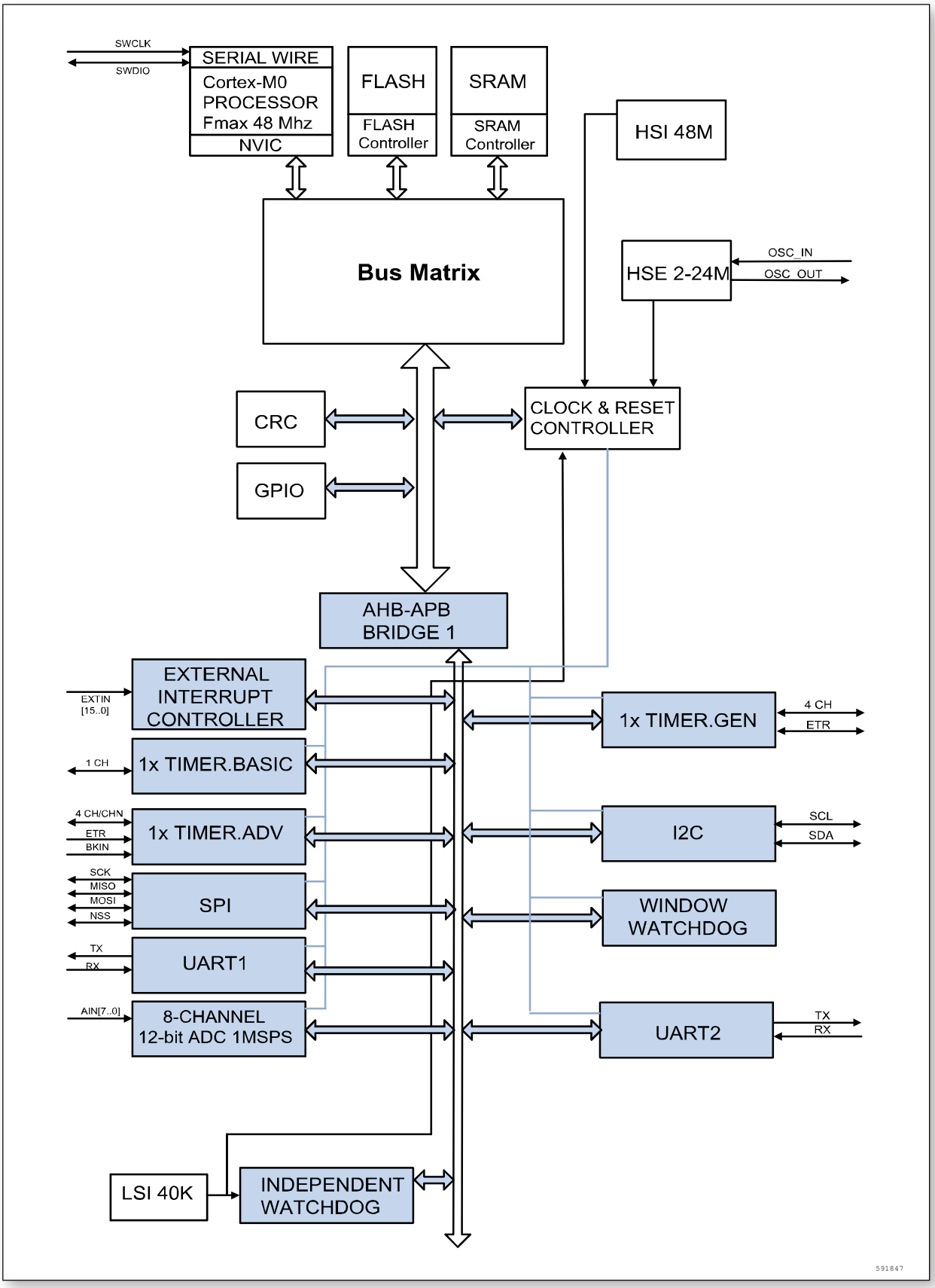

Figure 4 Block diagram

2.2 Functional Description

2.2.1 Core Introduction

Arm® Cortex® -M0 processor is a configurable and has multilevel pipeline 32-bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Memory Map

Table 2 Memory map

Bus	Address range	Size	Peripheral	Remark
Flash	0x0000 0000–0x0000 3FFF	16 KB	Mapped to Main Flash memory	
	0x0000 4000–0x07FF FFFF	~ 127 MB	Reserved	
	0x0800 0000–0x0800 3FFF	16 KB	Main Flash memory	
	0x0800 0000–0x1FFD FFFF	~ 383 MB	Reserved	
	0x1FFE 0000–0x1FFE 1BFF	7 KB	Reserved	
	0x1FFE 1C00–0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400–0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800–0x1FFF F80F	16 B	Option bytes	
SRAM	0x2000 0000–0x2000 07FF	2 KB	SRAM	
	0x2000 0700–0x2FFF FFFF	~ 255 MB	Reserved	
APB1	0x4000 0000–0x4000 03FF	1 KB	Reserved	
	0x4000 0400–0x4000 07FF	1 KB	TIM3	
	0x4000 0800–0x4000 0BFF	1 KB	Reserved	
	0x4000 2800–0x4000 2BFF	1 KB	Reserved	
	0x4000 2C00–0x4000 2FFF	1 KB	WWDG	
	0x4000 3000–0x4000 33FF	1 KB	IWDG	
	0x4000 3400–0x4000 37FF	1 KB	Reserved	
	0x4000 3800–0x4000 3BFF	1 KB	Reserved	
	0x4000 4000–0x4000 43FF	1 KB	Reserved	
	0x4000 4400–0x4000 47FF	1 KB	UART2	
	0x4000 4800–0x4000 4BFF	3 KB	Reserved	
	0x4000 5400–0x4000 57FF	1 KB	I2C1	
	0x4000 5800–0x4000 6BFF	5 KB	Reserved	
	0x4000 6C00–0x4000 6FFF	1 KB	Reserved	
	0x4000 7000–0x4000 73FF	1 KB	PWR	
	0x4000 7400–0x4000 FFFF	35 KB	Reserved	
APB1	0x4001 0000–0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400–0x4001 07FF	1 KB	EXTI	
	0x4001 0800–0x4001 23FF	7 KB	Reserved	
	0x4001 2400–0x4001 27FF	1 KB	ADC1	

Bus	Address range	Size	Peripheral	Remark
	0x4001 2800–0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00–0x4001 2FFF	1 KB	TIM1	
	0x4001 3000–0x4001 33FF	1 KB	SPI1	
	0x4001 3400–0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800–0x4001 3BFF	1 KB	UART1	
	0x4001 3C00–0x4001 3FFF	1 KB	Reserved	
	0x4001 4000–0x4001 43FF	1 KB	TIM14	
	0x4001 4400–0x4001 47FF	1 KB	Reserved	
	0x4001 4800–0x4001 4BFF	1 KB	Reserved	
	0x4001 4C00–0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000–0x4002 03FF	1 KB	Reserved	
	0x4002 0400–0x4002 0FFF	3 KB	Reserved	
	0x4002 1000–0x4002 13FF	1 KB	RCC	
	0x4002 1400–0x4002 1FFF	3 KB	Reserved	
	0x4002 2000–0x4002 23FF	1 KB	Flash Interface	
	0x4002 2400–0x4002 2FFF	3 KB	Reserved	
	0x4002 3000–0x4002 33FF	1 KB	CRC	
	0x4002 3400–0x47FF FFFF	~ 127 MB	Reserved	
	0x4800 0000–0x4800 03FF	1 KB	GPIOA	
	0x4800 0400–0x4800 07FF	1 KB	GPIOB	
	0x4800 0800–0x4800 0BFF	1 KB	Reserved	
	0x4800 0C00–0x4800 0FFF	1 KB	Reserved	
	0x4800 1000–0x5FFF FFFF	~ 384 MB	Reserved	

2.2.3 Embedded Flash Memory (FLASH)

Embedded flash memory up to 16KB for storing programs and data.

2.2.4 Embedded SRAM (SRAM)

Embedded SRAM up to 2KB.

2.2.5 Cyclical Redundancy Check Computing Unit (CRC)

The CRC (Cyclic Redundancy check) computing unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. The CRC-based technique is used to verify the consistency of data transfer or storage in its numerous applications.

Within the scope of the EN/IEC60335-1 standard, it provides a method of detecting flash memory errors. CRC computing unit can be used to calculate the software signature in real time and compare it to the signature generated when linking to and generating the software.

2.2.6 Nested Vectored Interrupt Controller (NVIC)

This product has a built-in nested vectored interrupt controller, which can process multiple

maskable interrupting channels (excluding 16 Cortex™-M0 interrupt lines) and 4 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry addresses directly passes into the kernel
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher-priority interrupts that arrive late
- Support tail link of interrupts
- Automatically save the processor state

Offer automatic recovery when the interrupt returns with no additional instruction. This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains multiple edge detectors which are used to generate interrupt/event requests. All IO pins can be connected to 16 external interrupt lines. Each interrupt line can be independently configured with its trigger event (rising edge or falling edge or both) and can be masked separately. A pending register maintains the states of all interrupt requests.

EXTI can detect level changes with pulse widths less than the internal AHB bus clock period.

2.2.8 Clock and Startup

Multiple prescalers are used to configure AHB frequency and high-speed APB areas. The highest frequency of AHB and high-speed APB is 48MHz. Please refer to the clock tree diagram in Figure 5.

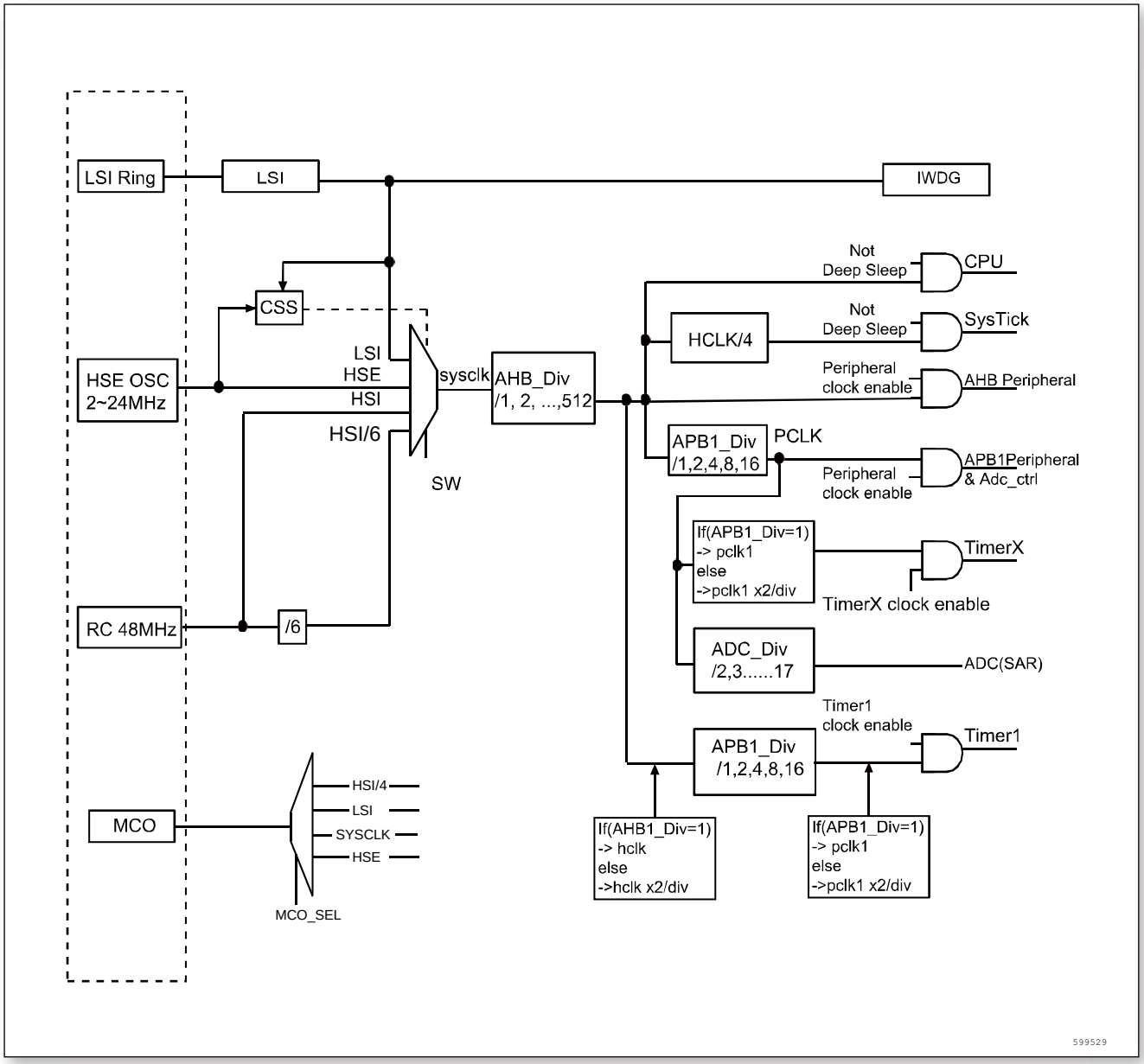

Figure 5 Clock tree

2.2.9 Scheme of Power Supply

V_{DD} = 2.0V~5.5V：the V_{DD} pin supplies power to the I/O pins and the internal voltage regulator.

2.2.10 Power Supply Monitor

This product is integrated with power on reset (POR)/power down reset (PDR) circuit. The circuit remains in the working state to ensure the system works when the power supply exceeds 2.0V. When V_{DD} is below the set threshold ($V_{POR/PDR}$), the device will be placed in the reset state. An external reset circuit is not necessary.

Additionally, there is a programmable voltage detector (PVD) in the device that monitors the V_{DD} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, the device can be interrupted. The interrupt handler will send a warning message or switch the microcontroller to safe mode. The PVD function can be enabled by a

program.

2.2.11 Voltage Regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low Power Mode (LP)

The product supports various low power modes that provide the best balance among low power requirements, short startup time, and multiple wake-up events.

Table 3 Low power mode list

Mode	Entry	Wake-up	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
Sleep (SLEEP NOW or SLEEP ON EXIT)	WFI (Wait for Interrupt)	Any interrupt	CPU clock off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wake-up interrupt			
Stop	PDDS=0 LPDS=0 or 1 (1) SLEEPDEEP=1 WFI or WFE	Any arbitrary interrupt (set in the external interrupt register)	All 1.5V area clocks are off	HSI and HSE oscillator off	On
Standby	PDDS=1 SLEEPDEEP=1 WFI or WFE	WKUP pin rising edge, NRST pin external reset, IWDG reset			Off

1) When LPDS=1, lower power consumption can be achieved. For more details, please refer to table 5.

Table 4 IP state table in different power consumption modes

Module/Mode	Run	Sleep	Stop (LPDS=0)	Stop (LPDS=1)	Standby
RCC	ON	ON	ON	ON	Power Down
EXTI	ON	ON	ON	ON	Power Down
CPU	ON	OFF	OFF	OFF	Power Down
UARTx	Optional	Optional	OFF	OFF	Power Down
I2Cx	Optional	Optional	OFF	OFF	Power Down
WWDG	Optional	Optional	OFF	OFF	Power Down
SPIx	Optional	Optional	OFF	OFF	Power Down
CRC	Optional	Optional	OFF	OFF	Power Down
TIMERx	Optional	Optional	OFF	OFF	Power Down
FLASH	ON	Standby	Standby	Deep Standby	Power Down
SRAM	ON	ON	Retention	Retention	Power Down
HSE (2-24MHz)	Optional	Optional	OFF	OFF	OFF
HSI RC 48M	ON	Optional	ON	ON	Power Down
LSI RC (40Khz)	Optional	Optional	Optional	Optional	Optional
IWDG	Optional	Optional	Optional	Optional	Optional
PVD	Optional	Optional	Optional	Optional	OFF
PWR	ON	ON	ON	ON	ON

Module/Mode	Run	Sleep	Stop (LPDS=0)	Stop (LPDS=1)	Standby
ADC	Optional	Optional	OFF	OFF	OFF
GPIO_CTRL	Optional	Optional	Optional	Optional	Power Down
IO	ON	ON	ON	ON	ON

1) Power Down: Module power down and data will be lost
2) Optional: ON or OFF configured by software
3) ON: Working
4) OFF: Module in off state
5) Retention: Data are kept but unchangeable

Sleep Mode

In the sleep mode, only the CPU stops working. All peripherals are working and can wake up the CPU in the event of an interrupt/event.

Stop Mode

The Stop mode minimizes the power consumption while keeping the SRAM and register contents intact. In the Stop mode, the HSI oscillator and HSE crystal oscillator are shut down. The microcontroller can be woken from the Stop mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The Standby mode can minimize the power consumption of the system. In the Standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V domain are disconnected. HSI, and HSE oscillators are also turned off. The microcontroller can be woken by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. The microcontroller also can be woken and reset by the watchdog timer. The contents of SRAM and registers will be lost.

2.2.13 Timer and Watchdog (TIM & WDG)

The product includes one advanced timer, one general-purpose timer, one basic timer, two watchdog timers and one Systick timer.

The following table compares the functions of advanced timer, general-purpose timer and basic timer:

Table 5 Timer function comparison

Timer type	Name	Counter resolution	Counter type	Prescaler factor	Capture/compare channel	Complementary output
Advanced	TIM1	16 bit	Up, down, up/down	Any integer between 1~65536	4	Yes
General-purpose	TIM3	16 bit	Up, down, up/down	Any integer between 1~65536	4	None
Basic	TIM14	16 bit	Up	Any integer between 1~65536	1	None

Advanced Control Timer (TIM1)

Advanced control timer is composed of one 16-bit counter, 4 capture/compare channels and three-phase complementary PWM generators. It has complementary PWM output with dead time insertion and can be used as a complete universal timer. Four separate channels can be used for the followings:

- Input capture
- Output compare
- PWM generation (edge or center alignment mode)
- Single pulse output

When it is configured as a 16-bit general-purpose timer, it has the same function as a TIM3 timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In the debug mode, the counter can be frozen while the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many of its features are the same as the general-purpose TIM timer. Their internal structures are identical. Therefore, the advanced control timer can be used in conjunction with the TIM timer to support synchronization or event linking.

General-purpose Timer (TIM3)

One synchronously running general-purpose timer (TIM3) is built into the product. The universal timer has one 16-bit automatic up-down counter, one 16-bit prescaler and three separate channels. Each channel can be used for input capture, output compare, PWM and single pulse output.

They can also be used in conjunction with the advanced control timer to support synchronization or event linking. Counters can be frozen in the debug mode. Any general-purpose timer can be used to produce PWM output.

These timers can also handle signals from incremental encoders and digital outputs from 1~3 Hall sensors. Each timer can produce PWM output, or be seen as a simple time reference.

Basic timer (TIM14)

The timer contains one 16-bit automatically reloadable count-up counter and one 16-bit prescaler. It has a single channel for input capture/output compare, PWM or single pulse output. Its counter can be frozen in the debug mode.

Independent watchdog (IWDG)

The independent watchdog contains one 12-bit count-down counter and one 8-bit prescaler. There is an internal independent 40KHz clock oscillator. This oscillator is independent of the master clock, so it can work in the Stop and Standby modes. It can be used to reset the entire system in the event of system failure or used as a free timer to provide timeout management for applications. The options can be configured to boot watchdog via software or hardware.

In the debug mode, the watchdog is off.

Window Watchdog (WWDG)

The window watchdog has one 7-bit count-down counter and can be set to run freely. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. In the debug mode, the watchdog is off.

System Time Base Timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a standard count-down counter. It has the following characteristics:

- One 24-bit count-down counter
- Automatic reloading
- One maskable system interrupt can be raised when the counter is 0
- Programmable clock source

2.2.14 Universal Asynchronous Receiver and Transmitter (UART)

The UART interface supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be 5, 6, 7, 8 and 9 bits, which are configurable. The highest baud rate can be up to 3Mbps.

2.2.15 I2C Bus (I2C)

I2C bus interface can operate in the multi-master mode or slave mode and it supports the standard and fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

Slave mode supports multiple address response.

2.2.16 Serial Peripheral Interface (SPI)

The SPI interface can be configured as 1-32 bits per frame in the slave or master mode. The maximum speed of master mode is 24M, and the maximum speed of slave mode is 12M.

2.2.17 General Purpose Input/Output Interface (GPIO)

Each GPIO pin can be set as an output (push-pull or open-drain), an input (with or without pull-up/pull-down), or a multiplexed port of peripherals via software. Most GPIO pins are shared with digital or analog multiplexed peripherals.

If required, the peripheral function of the I/O pins can be locked with a specific operation to avoid accidental writing into the I/O register.

2.2.18 Analog-to-Digital Converter (ADC)

The product is embedded with one 12-bit analog-to-digital converter (ADC), with up to 8 external channels available for single, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

The analog watchdog function allows to monitor one or all selected channels precisely. An

interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by a general timer (TIM3) and an advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can control the ADC conversion synchronized with the clock.

2.2.19 Serial Wire Debug Port (SWD)

Two-wire serial debug port (SW-DP) is embedded in Arm.

The Arm SW-DP allows debugging tools connect to the microcontroller through SWD port.

3 Pin Definition and Multiplex Functions

3.1 Pin Definition

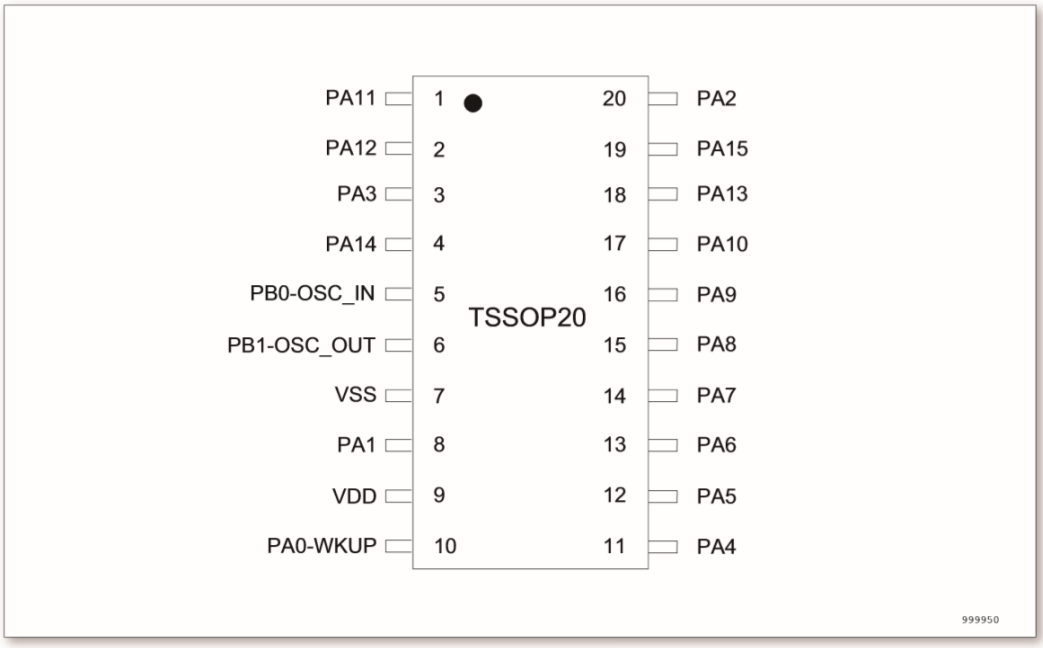

Figure 6 TSSOP20 Pinout

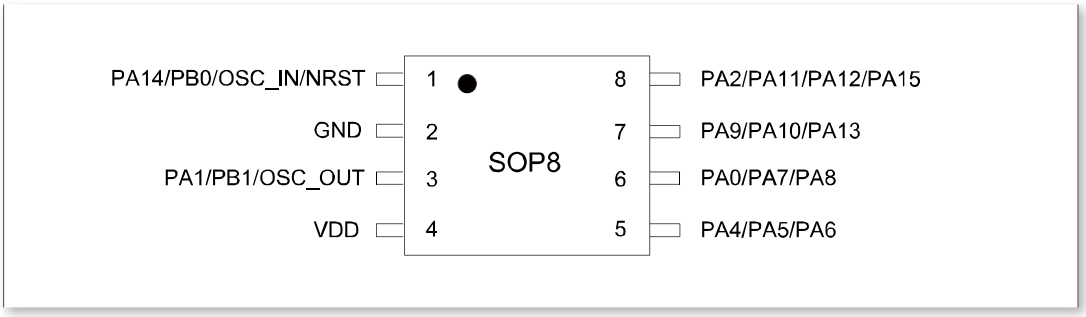

Figure 7 SOP8 Pinout

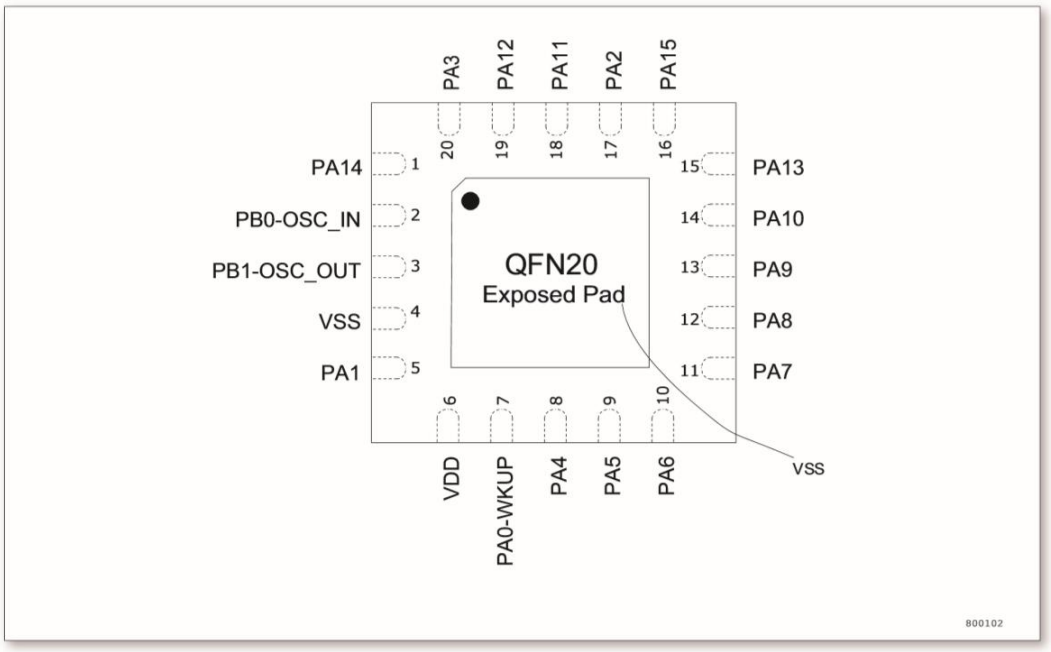

Figure 8 QFN20 Pinout

3.2 Pin Definition Table

Table 6 Pin definition

Pin Code			Pin name	Type (1)	I/O Level (2)	Main function	Optional multiplex function	Additional function
QFN20	TSSOP20	SOP8						
1	4	1	PA14	I/O	TC	PA14	SWDCLK/ UART1_TX	nRST (3)
2	5	1	PB0 OSC_IN	I/O	TC	PB0	-	ADC1_VIN[1]
3	6	3	PB1 OSC_OUT	I/O	TC	PB1	-	ADC1_VIN[0]
4	7	2	VSS	S	-	VSS	-	-
5	8	3	PA1	I/O	TC	PA1	UART2_TX/ I2C1_SDA	-
6	9	4	VDD	S	-	VDD	-	-
7	10	6	PA0	I/O	TC	PA0	SPI1_NSS/ UART1_RX/ TIM1_CH3N/ I2C_SCL/ TIM3_CH3	WKUP
8	11	5	PA4	I/O	TC	PA4	I2C1_SDA/ TIM1_BKIN	-
9	12	5	PA5	I/O	TC	PA5	SPI1_SCK/ I2C1_SCL	-
10	13	5	PA6	I/O	TC	PA6	SPI1_MOSI/ TIM1_CH1/ TIM1_CH1N/ TIM1_CH3	-
11	14	6	PA7	I/O	TC	PA7	SPI1_MISO/ TIM1_CH1N/ TIM1_CH2N/ MCO/ TIM1_CH4	ADC1_VIN[7]
12	15	6	PA8	I/O	TC	PA8	SPI1_SCK/ TIM1_CH2/ TIM3_CH1	-
13	16	7	PA9	I/O	TC	PA9	SPI1_MOSI/ TIM1_CH2N/ TIM1_CH1/ TIM14_CH1	-
14	17	7	PA10	I/O	TC	PA10	SPI1_MISO/ TIM1_CH3/ TIM1_CH2	-
15	18	7	PA13	I/O	TC	PA13	SWDIO/ UART1_RX/ UART2_RX/ I2C1_SCL	-
16	19	8	PA15	I/O	TC	PA15	SPI1_NSS/ TIM1_CH3N/ TIM3_CH3	ADC1_VIN[6]
17	20	8	PA2	I/O	TC	PA2	TIM1_CH2N/ TIM3_CH2	ADC1_VIN[5]
18	1	8	PA11	I/O	TC	PA11	TIM1_CH2/ TIM14_CH1/ TIM3_CH1	ADC1_VIN[4]
19	2	8	PA12	I/O	TC	PA12	UART1_TX	ADC1_VIN[3]
20	3	-	PA3	I/O	TC	PA3	UART1_RX	ADC1_VIN[2]

1) I = Input, O = Output，S = Power Supply, HiZ = High Resistance.

2) TC: Standard IO, input signal does not exceed V_{DD} voltage.

3) When SFT_NRST_RMP bit of RCC_SYSCFG is set to 1, PA14 is mapped as an nRST external reset and should be held low for at least 4us for reliable reset.

3.3 Multiplex Function Table

Table 7 PA port multiplex

Pin	AF0	AF1	AF2	AF3	AF4
PA0	SPI1_NSS	UART1_RX	TIM1_CH3N	I2C1_SCL	TIM3_CH3
PA1	-	-	UART2_TX	I2C1_SDA	-
PA2	-	-	TIM1_CH2N	-	TIM3_CH2
PA3	-	UART1_RX	-	-	-
PA4	-	-	TIM1_BKIN	I2C1_SDA	-
PA5	SPI1_SCK	-	-	I2C1_SCL	-
PA6	SPI1_MOSI	TIM1_CH1	TIM1_CH1N	-	TIM1_CH3
PA7	SPI1_MISO	TIM1_CH1N	TIM1_CH2N	MCO	TIM1_CH4
PA8	SPI1_SCK	TIM1_CH2	-	-	TIM3_CH1
PA9	SPI1_MOSI	TIM1_CH2N	TIM1_CH1	TIM14_CH1	-
PA10	SPI1_MISO	TIM1_CH3	TIM1_CH2	-	-
PA11	-	-	TIM1_CH2	TIM14_CH1	TIM3_CH1
PA12	-	UART1_TX	-	-	-
PA13	SWDIO	UART1_RX	UART2_RX	I2C_SCL	
PA14	SWDCLK	UART1_TX	-	-	-
PA15	SPI_NSS	TIM1_CH3N	-	-	TIM3_CH3

Table 8 PB port multiplex

Pin	AF0	AF1	AF2	AF3	AF4
PB0	-	-	-	-	-
PB1	-	-	-	-	-

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Load Capacitance

The load condition during the measurement of pin parameters is shown in the figure below.

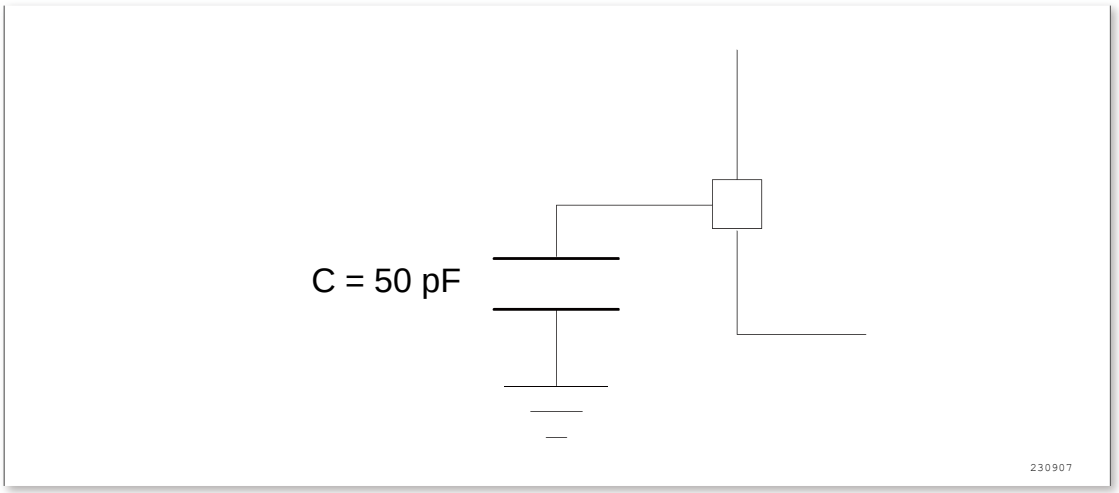

Figure 9 Pin load condition

4.1.2 Input Voltage on Pin

The measurement of input voltage on pin is shown in the figure below.

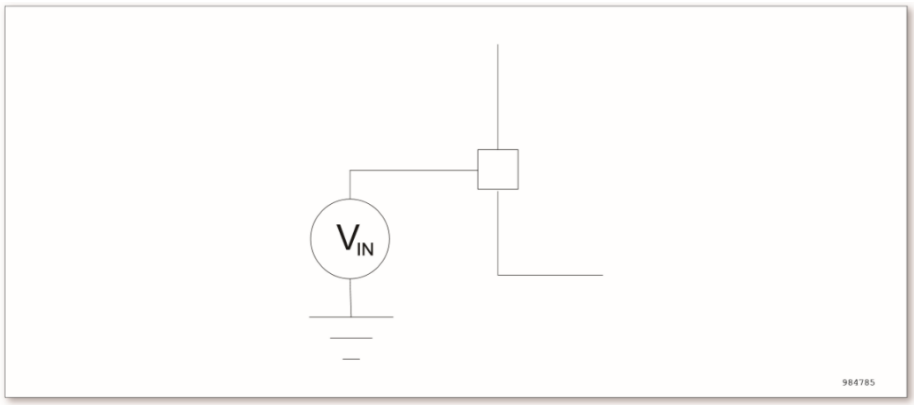

Figure 10 Input voltage on pin

4.1.3 Scheme of Power Supply

The power supply designing plan is shown in the figure below.

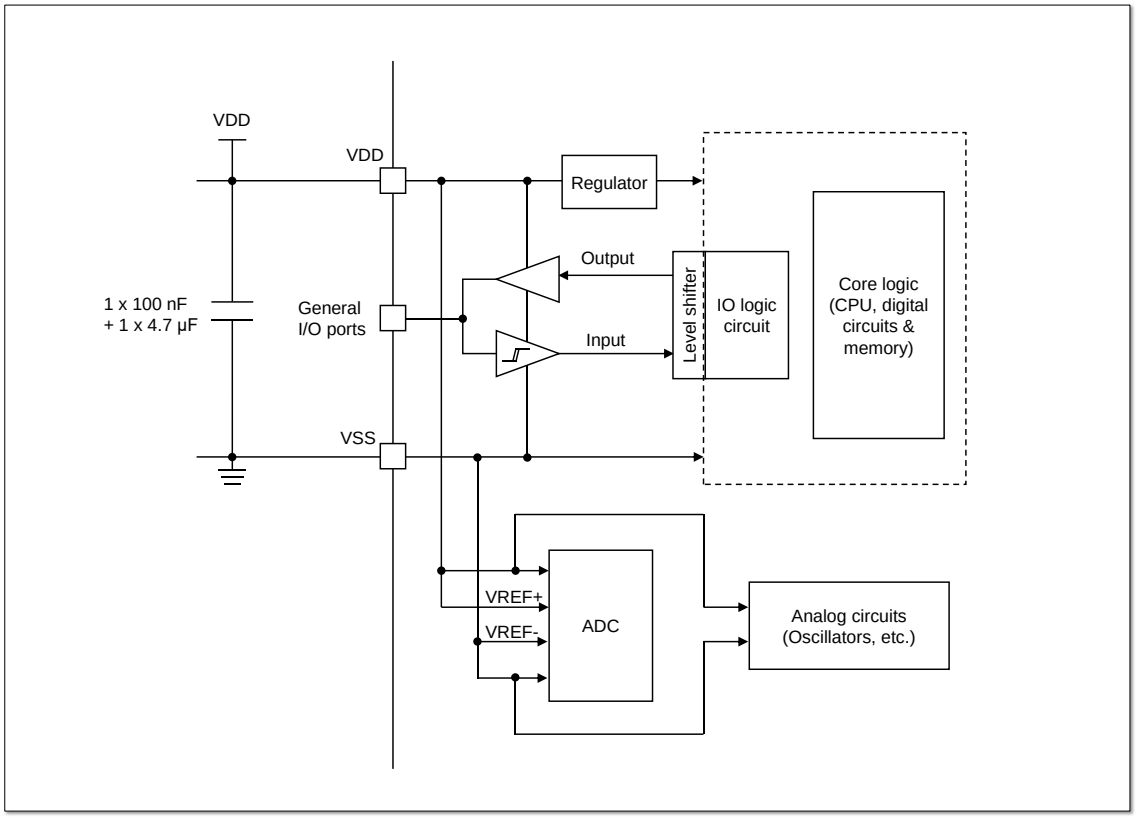

Figure 11 Scheme of power supply

4.1.4 Measurement of Current Consumption

The measurement of current consumption on pin is shown in the figure below.

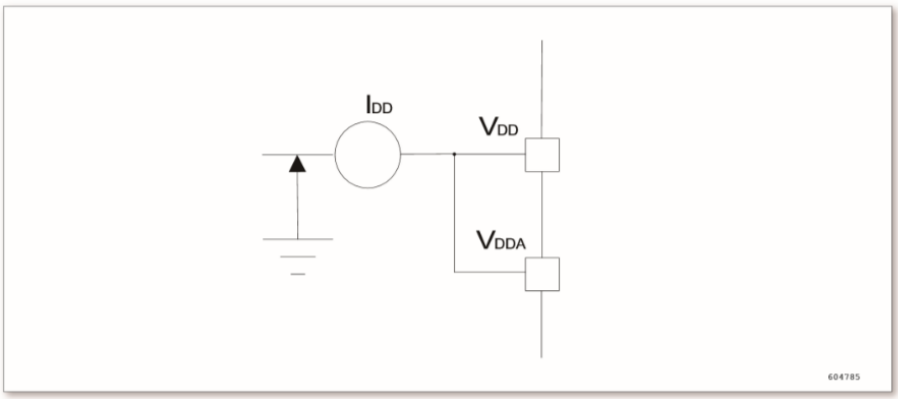

Figure 12 Scheme of current consumption measurement

4.2 Absolute Maximum Rating

If the load applied to the device exceeds the value in the list of 'absolute maximum ratings' (Tables 9 and 10), the device may be damaged permanently. The list shows the maximum load that the device can bear. It does not mean that the functional operation of the device under these conditions is normal. The reliability of the device will be affected if the device works for a long time under the maximum condition.

Table 9 Voltage characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (1)	- 0.3	5.8	V
V_{IN}	Input voltage on other pins (2)	Vss-0.3	V_{DD}+0.3	

1) All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply system within the permissible range.
2) The maximum value of V_{IN} must always be observed. For information about the permitted maximum current values, please see the table below.

Table 10 Current characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
I_{VDD}	Total current through V_{DD} power cord (supply current)(1)	-	+60	mA
I_{VSS}	Total current through VSS ground wire (outflow current)(1)	-	-60	
I_{IO}	Sink current through any I/O and control pins	-	+25	
	Output current through any I/O and control pins	-	-25	
$I_{INJ\ (PIN)}$ (2) (3)	Injection current through nRST pin	-	±5	
	Injection current through OSC_IN pin of HSE	-	±5	
$\sum I_{INJ\ (PIN)}$ (4)	Injection current through other pins	-	±25	

1) All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply system within the permissible range.
2) $I_{INJ(PIN)}$ must not exceed its limit, that is to ensure the V_{IN} does not exceed its maximum. If you cannot guarantee that the V_{IN} does not exceed its maximum value, please make sure that the $I_{INJ(PIN)}$ does not exceed its maximum value under external constraint. When $V_{IN} > V_{DD}$, there is a forward injection current; When $V_{IN} < V_{SS}$, there is a reverse injection current.
3) The reverse injection current will interfere with the analog performance of the device.
4) When injection currents go through several I/O ports at the same time, the maximum $\Sigma I_{INJ\ (PIN)}$ is the sum of absolute values of the forward and reverse injection currents in the real time. The result is based on the characteristics of the maximum $\Sigma I_{INJ\ (PIN)}$ on all the I/O ports.

4.3 Operating Condition

4.3.1 General Operating Condition

Table 11 General operating condition

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	48	
V_{DD}	Standard operating voltage	-	2.0	-	5.5	V
P_D	Power dissipation Temperature： T_A = 85℃ (1) Or temperature： T_A = 105℃ (1)	QFN20	-	-	196	mW
		TSSOP20	-	-	270	
$R_{JA-QFN20}$	QFN20 junction to ambient thermal resistance	-	-	75	-	℃/W
T_A	T_A=85℃	Maximum power dissipation	-40	-	85	℃
	T_A=105℃	Maximum power dissipation	-40	-	105	℃
T_J	Junction temperature range(2) (3)	Regular type (T_A=85℃)	-40	-	105	℃
		Extended type (T_A=105℃)	-40	-	125	

1) If T_A is low, a higher P_D value is allowed as long as T_J does not exceed T_{Jmax}.
2) In the state of lower power dissipation, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.
3) Use equation $T_J = T_A + R_{JA} * P_D$ to calculate junction temperature.

4.3.2 Operating Condition of Power Up and Power Down

The parameters in the table below are tested under general operating conditions.

Table 12 Operating condition when power is on and power is down (1) (2)

Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time t_r	10	-	500000	us
	V_{DD} fall time t_f	50	-	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1) Drawn from comprehensive evaluation and not tested in production.
2) The power-up and power-down V_{DD} waveforms should strictly follow the t_r and t_f phases in the following waveform diagram. Voltage dropping down is not allowed during power-up process.
3) Note: To confirm the power-on reliability on chip, the chip should be power-on at 0V.

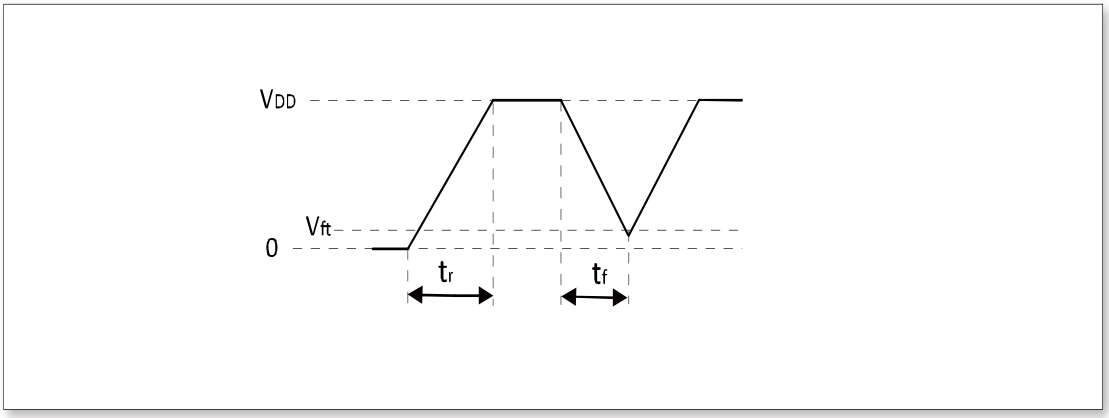

Figure 13 Waveforms during power-up and power-down

4.3.3 Characteristics of Embedded Reset and Power-Control Moduels

The parameters in the table below are tested based on the ambient temperature and V_{DD} supply voltage listed in the following table.

Table 13 Characteristics of embedded reset and power-control moduels (1)

Symbol	parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	

Symbol	parameter	Condition	Minimum value	Typical value	Maximum value	Unit
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	
		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	POR/PDR threshold	Flipping point	-	1.65	-	V
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	4.6	-	ms

1) 1) Guaranteed by design, not tested in production

2) Note: Reset duration is measured from the power-on moment (POR reset) to the moment the first IO flipping by the user's application code.

4.3.4 Supply Current Characteristics

Current consumption is an index of multiple parameters and factors, which include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, program location in memory and executed code, etc. The current consumption readings in all operating modes given in this section execute a set of simple codes.

```
int main ( )
{
System Init ( ) ;
. . . . . .
        while ( 1 ) { }
}
```

Typical current consumption

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 wait cycle at 0~24 MHz; 1 wait cycle at 24~48 MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in the following table.
- The instruction prefetch function enabled. When the peripheral is enabled: $f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 14 Typical current consumption under operating mode at high and low temperature (1) (2)

Symbol	Parameter	Condition	f_{HCLK} (HZ)	Typical value Enable all peripherals				Typical value Disable all peripherals				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in operating mode	Internal clock	48M	6.77	6.94	7.12	7.20	4.02	4.16	4.32	4.40	mA
			24M	4.19	4.32	4.49	4.56	2.54	2.64	2.80	2.87	
			8M	1.86	1.98	2.17	2.23	1.40	1.52	1.71	1.77	
			4M	1.37	1.48	1.64	1.72	1.10	1.20	1.37	1.45	
			2M	1.08	1.18	1.33	1.40	0.95	1.05	1.19	1.26	
			1M	0.94	1.04	1.17	1.24	0.87	0.97	1.11	1.17	
			500K	0.87	0.96	1.10	1.16	0.84	0.93	1.07	1.13	
			125K	0.82	0.91	1.05	1.11	0.81	0.90	1.03	1.10	

Table 15 Typical current consumption under Sleep mode at high and low temperature (1) (2)

Symbol	Parameter	Condition	f_{HCLK} (HZ)	Typical value Enable all peripherals				Typical value Disable all peripherals				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Sleep mode	Internal clock	48M	4.60	4.73	4.90	4.97	1.83	1.94	2.08	2.15	mA
			24M	3.00	3.12	3.26	3.34	1.33	1.43	1.57	1.63	
			8M	1.43	1.53	1.67	1.73	0.97	1.06	1.20	1.26	
			4M	1.16	1.26	1.39	1.46	0.88	0.98	1.11	1.18	
			2M	0.98	1.07	1.21	1.27	0.84	0.94	1.07	1.13	
			1M	0.89	0.98	1.12	1.18	0.82	0.91	1.05	1.11	
			500K	0.84	0.94	1.07	1.13	0.81	0.90	1.04	1.10	
			125K	0.81	0.91	1.04	1.10	0.80	0.89	1.03	1.09	

1) The typical value is tested at VDD=3.3V.

2) It's obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division

Table 16 Typical supply current in the Stop and Standby modes at high and low temperatures

Symbol	Parameter	Condition	Typical value				Maximum value	Unit
			-40℃	25℃	85℃	105℃	25℃	
I_{DD}	Supply current in the Stop mode	PWR->CR register bit0 is set to 1	1.3	2.1	12.6	31.0	15.0	μA
	Supply current in the Standby mode	LSI and IWDG On	1.0	1.1	2.4	6.2	-	
	Supply current in the Standby mode	IWDG Off	0.4	0.4	1.7	5.5	1.0	

1) The typical value is tested at T_A=25℃ and V_{DD}=3.3V.

2) Drawn from the comprehensive evaluation, not tested in production. IO state is analog input.

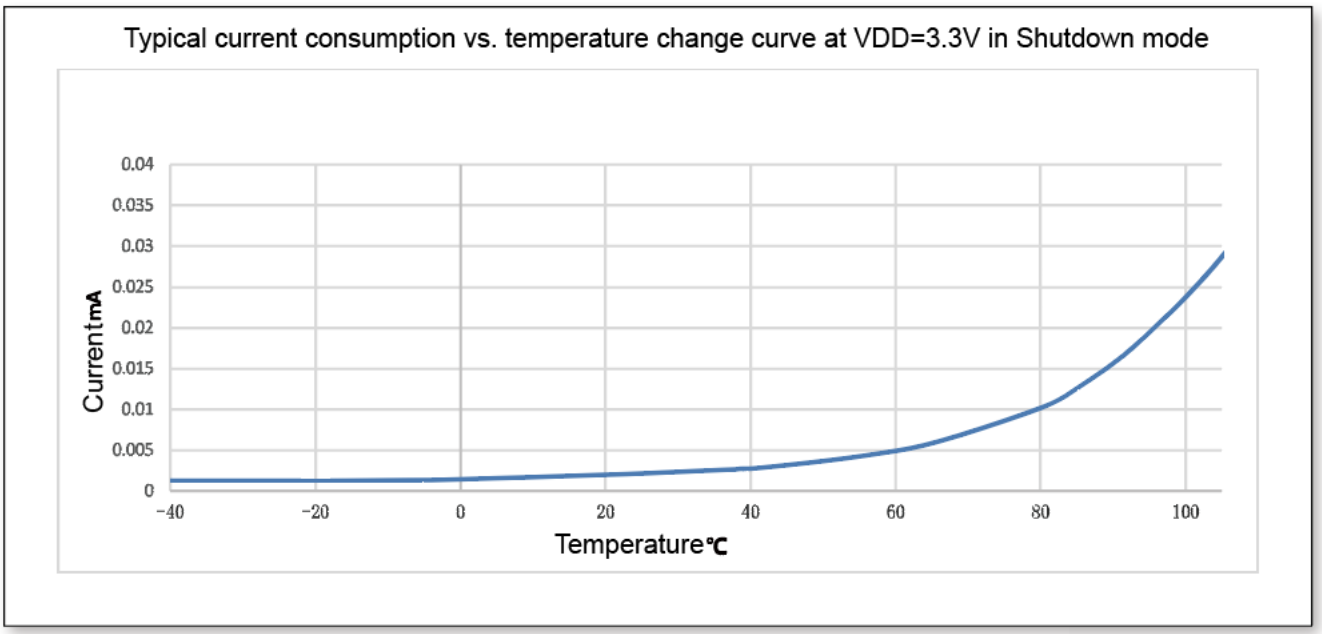

Figure 14 Typical current consumption vs. temperature at VDD = 3.3V in Stop mode

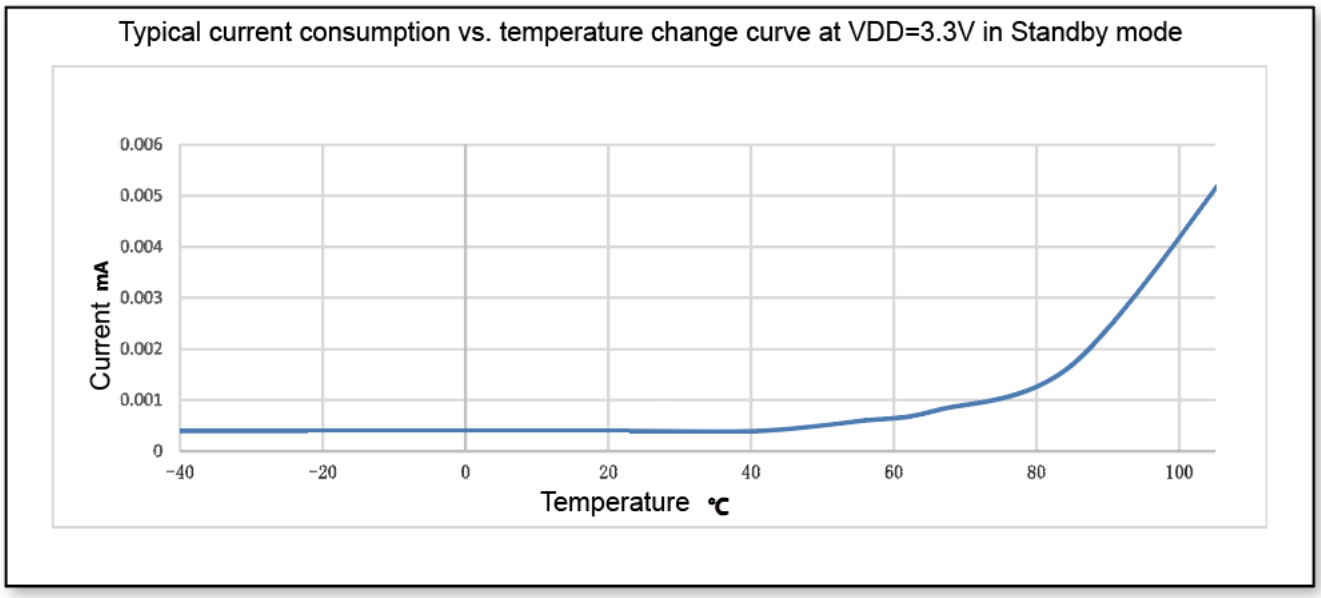

Figure 15 Typical current consumption vs. temperature at VDD = 3.3V in Standby mode

Embedded Peripheral Current Consumption

The embedded peripheral current consumption is listed in thetable below and the MCU is working in the following conditions:

- All I/O pins are in input mode and connected to a static level—VDD or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The values given are calculated by measuring the current consumption
  - Disable all peripheral clocks
  - Only enable one peripheral clcok
- Ambient temperature and V_{DD} supply voltage conditions are listed in the following table.

Table 17 Embedded peripheral current consumption

Bus	Embedded peripheral	Typical value	Unit
AHB	CRC	1.4	uA/MHz
	GPIOA	0.8	
	GPIOB	0.6	
APB1	SYSCFG	0.3	
	ADC1	1.5	
	TIM1	12.3	
	SPI1	7.7	
	UART1	7.2	
	TIM14	3.0	
	DBG	0.2	
	TIM3	8.0	
	WWDG	0.5	
	UART2	6.7	
	I2C1	10.0	
	PWR	0.5	

1) f_{HCLK} = 48MHz，f_{APB1} = f_{HCLK}/2，the prescaler factor of each peripheral is the default value.

Wake-up time from low power mode

The wake-up times listed in the following table are measured during the wake-up phase of the internal clock HSI. The clock source used for wake-up depends on the current operation mode.

- Stop or Standby mode: clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering the sleep mode. All time are measured when the operating environment temperature and supply voltage conform to the general operating condition.

Table 18 Wake-up time from low power mode

Symbol	Parameter	Condition	Typical value	Unit
$t_{WUSLEEP}$ (1)	Wakeup from the Sleep mode	System clock is HSI	2.81	μS
t_{WUSTOP} (1)	Wakeup from the Stop mode (the regulator is in operation mode)	System clock is HSI	9.69	
t_{WUSTOP} (1)	Wakeup from the Stop mode (the regulator is in operation mode)	System clock is HSI	7.65	
$t_{WUSTDBY}$ (1)	Wakeup from the Standby mode	PWR->CR[15:14] = 0x0	400	
$t_{WUSTDBY}$ (1)	Wakeup from the Standby mode	PWR->CR[15:14] = 0x1	342	

Symbol	Parameter	Condition	Typical value	Unit
$t_{WUSTDBY}$ (1)	Wakeup from the Standby mode	PWR->CR[15:14] = 0x2	299	
$t_{WUSTDBY}$ (1)	Wakeup from the Standby mode	PWR->CR[15:14] = 0x3	217	

1) The wake-up time is the time from the wake-up edge to the time in which program execues IO flip.

4.3.5 External Clock Source Characteristics

High-speed external user clock from external oscillator source

The characteristic parameter given in the following table is measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating condition.

Table 19 High-speed external user clock characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{HSE_ext}	User external clock frequency (1)	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage	VSS	-	0.3	VDD
$t_{w\ (HSE)}$	OSC_IN high or low time (1)	15	-	-	ns
$C_{in\ (HSE)}$	OSC_IN input capacitive reactance (1)	-	5	-	pF
DuCy (HSE)	Duty cycle	-	50	-	%

1) Guaranteed by design, not tested in production.

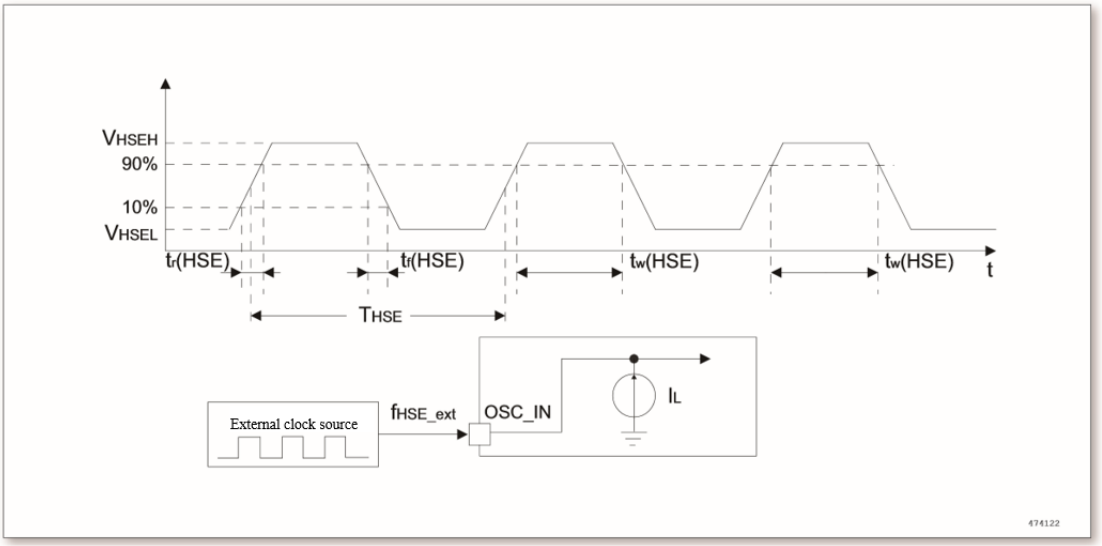

Figure 16 AC timing diagram of external high-speed clock source

High-speed external clock generated by a crystal/ceramic resonator

The high-speed external clock (HSE) may be generated by an oscillator composed of a 8~24MHz crystal/ceramic resonator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external elements listed in the table below. In application, the resonator and load capacitor must be maximally close to the oscillator pin to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 20 HSE 8 ~ 24MH oscillator characteristics (1) (2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	2V<VDD<3.6V	2	8	12	MHz
		3.0V<VDD<5.5V	8	16	24	MHz
R_F	Feedback resistance (3)	-	-	500	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2} (4) 16pF)	f_{OSC_IN} =24M VDD=3V	-	-	60	Ω
		f_{OSC_IN} =12M VDD=2V	-	-	150	Ω
I_2	HSE drive current	f_{OSC_IN} =24M ESR=30 V_{DD} = 3.3V， C_{L1} C_{L2} (3) 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Startup	-	9	-	mA/V
$t_{SU\ (HSE)}$ (5)	Startup time	V_{DD} is stable	-	3	-	mS

1) The characteristic parameter of the resonator is given by the crystal/ceramic resonator manufacturer.

2) Drawn from comprehensive evaluation, not tested in production.

3) The relatively low R_F resistance value can provide protection and avoid problems when operating in a humid environment. The leakage and bias conditions generated in this environment have changed. However, if the MCU is used in harsh humid conditions, such parameters need to be taken into account in the design.

4) For C_{L1} and C_{L2}, it is recommended to use 5pF~25pF (typical value) high-quality ceramic capacitor designed for high-frequency applications, as well as crystal or resonator that meets the requirements. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the capacitance between the pins and the PCB board can be roughly estimated as 5pF).

5) $t_{SU(HSE)}$ is the start-up time, which is the time duration with the measurement starting when the software enables HSE until a stable 8MHz oscillation is obtained. This value is drawn based on readings on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

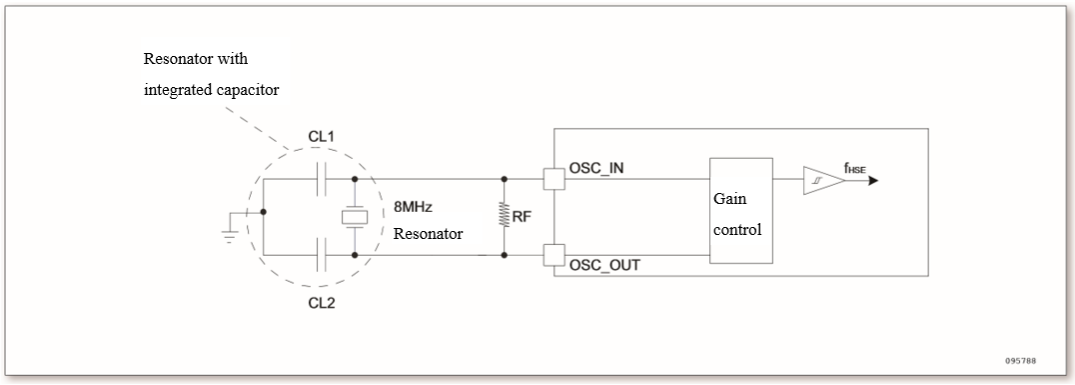

Figure 17 Typical application using 8MHz crystal

4.3.6 Internal Clock Source Characteristics

The characteristic parameter given in the following table is measured when ambient temperature and power supply voltage meet with the general operating condition.

High-speed internal (HSI) oscillator

Table 21 HSI oscillator characteristics (1) (2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
		T_A = -40℃~ 85℃	-2.5	-	+2.5	%
		T_A = -40℃~ 105℃	-3	-	+3	%
		T_A = 25°C	-1	-	+1	%
$t_{SU\ (HSI)}$	HSI oscillator startup time	-	-	12	16	μS
$I_{DD\ (HSI)}$	HSI oscillator power consumption	-	-	519	-	μA

1) V_{DD} = 3.3V, unless otherwise specified.

2) Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 22 LSI oscillator characteristics (1) (2)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSI} (2)	Frequency	-	40	-	KHz
$t_{SU\ (LSI)}$ (2)	LSI oscillator startup time	-		100	μS
$I_{DD\ (LSI)}$ (2)	LSI oscillator power consumption	-	0.91	1.4	μA

1) V_{DD} = 3.3V, T_A = -40℃~ 85℃, unless otherwise specified.

2) Drawn from comprehensive evaluation, not tested in production.

4.3.7 Memory Characteristics

Table 23 FLASH Memory characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16bit programming time	-		26	-	μS
f_{EWCLK}	Erase and write frequency	-	8	-	-	MHz
t_{ERASE}	Page (1024 bytes) erase time	-	8	-	10	mS
t_{ME}	Full erasing time	-	20	-	40	mS
I_{DD}	Supply current	Read mode 40MHz	-	3	4.5	mA
		Write mode	-	-	3.5	mA
		Erase mode	-	-	2	mA
V_{prog}	Programming voltage	-	-	1.5	-	V

Table 24 FLASH memory life and data retention period (1) (2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
N_{END}	Life (erasing and programming times)		20000	-	-	Times
T_{DR}	Data retention	T_A = 125℃	10	-	-	Year
		T_A = 25℃	100	-	-	

1) Drawn from comprehensive evaluation, not tested in production.

2) Cyclical tests are performed over the entire temperature range.

4.3.8 EMC Characteristics

Sensitivity testing is carried out by sampling during product comprehensive evaluation.

Functional EMS (electromagnetic sensitivity)

When running a simple application (2 LEDs flash via the I/O port), the test sample is applied with one electromagnetic interference until an error is generated, and the LED flashes to indicate and error.

- EFT：In V_{DD} and V_{SS}, impose a pulse group (forward and backward) with a transient voltage by a 100 pF capacitor until a functional error is generated. This test complies with the IEC61000-4-4 standard.

Chip reset can restore normal operation of the system. The test results are listed in the table below.

A represents normal operation of function.

B indicates normal operation after the chip generates a reset.

Table 25 EMS characteristics (1)

Symbol	Parameter	Condition	Level/Type
V_{EFT}	In VDD and VSS, the limit of voltage imposed on pulse group with a transient	V_{DD} = 3.3V，T_A = +25℃，f_{HCLK} = 48MHz. Compliance with IEC61000-4-4	4A

Symbol	Parameter	Condition	Level/Type
	voltage by a 100 pF capacitor until a functional error is generated		
V_{ESD}	Voltage limit imposed on either I/O pin, resulting in functional error	V_{DD} = 3.3V，T_A = +25℃，f_{HCLK} = 48MHz. Compliance with IEC61000-4-2	2B

1) Drawn from comprehensive evaluation, not tested in production.

Design reliable software to avoid noise

EMC evaluation and optimization at the device level are carried out in a typical application environment. It should be noted that good EMC performance is closely related to user applications and specific software.

Therefore, it is recommended that users implement EMC optimization on the software and conduct EMC-related certification tests.

Software recommendations

The software flow must include the control of program runaway, such as

- Corrupted program counter
- Unexpected reset
- Critical data destroyed (control registers, etc...)

Test before certification

Many common failures (unexpected reset and corrupted program counter) can be reproduced by manually introducing a low level on NRST or introducing a 1-second low level on the crystal oscillator pin.

During ESD test, a voltage exceeding the application requirement can be directly applied to the chip. When an unexpected action is detected, the software part needs to be strengthened to prevent unrecoverable errors.

4.3.9 Functional EMS (electromagnetic susceptibility)

Based on three different tests (ESD, LU), a specific measurement method is used to conduct a strength test on the chip to determine its electrical sensitivity performance.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse and then a negative pulse after one second interval) is applied to all the pins of all samples. The size of the sample is related to the number of power supply pins on the chip (3 pieces x (n + 1) power supply pin). This test complies with the standard ESDA/JEDEC JS-001-2017/JS-002-2018.

Static latch-up

In order to evaluate the latch performance, 2 complementary static latch-up tests need to be performed on 6 samples:

- Provide a supply voltage exceeding the limit for each power supply pin.

- Inject current into each input, output, and configurable I/O pin. This test complies with the EIA/JESD78E integrated circuit latch-up standard.

Table 26 ESD characteristics (1)

Symbol	Parameter	Condition	Maximum value	Unit
$V_{ESD\ (HBM)}$	Electrostatic discharge voltage (human body model)	TA = 25℃, compliance with ESDA/JEDECJS-001-2017	±8000	V
$V_{ESD\ (CDM)}$	Electrostatic discharge voltage (charging device model)	TA = 25℃, compliance with ESDA/JEDECJS-002-2018	±2000	V
I_{LU}	Static latching (Latch-up current)	TA = 25℃, compliance with JESD78E	+150 / -200	mA

1) Drawn from comprehensive evaluation, not tested in production.

4.3.10 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameter listed in the table below is measured according to the condition in Table 11. All I/O ports are compatible with CMOS.

Table 27 IO static characteristics (1)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	3.3V CMOS port	-0.3	-	0.8	V
V_{IL}	Input low level voltage	5V CMOS port	-0.3	-	0.3*VDD	V
V_{IH}	Input high level voltage	3.3V CMOS port	2	-	3.3	V
V_{IH}	Input high level voltage	5V CMOS port	0.7*VDD	-	5	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis (2)	3.3V	0.1*VDD	-	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis (2)	5V	0.1*VDD	-	-	V
I_{lkg}	Input leakage current (2)	3.3V	-	-	1	μA
I_{lkg}	Input leakage current (2)	5V	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistanc (3)	3.3V $V_{IN} = V_{SS}$	22	-	100	kΩ
R_{PU}	Weak pull-up equivalent resistanc (3)	5V $V_{IN} = V_{SS}$	22	-	100	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V $V_{IN} = V_{DD}$	20	-	50	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	5V $V_{IN} = V_{SS}$	20	-	50	kΩ
C_{IO}	I/O pin capacitance	3.3V	-	-	10	pF
C_{IO}	I/O pin capacitance	5V	-	-	10	pF

1) Drawn from comprehensive evaluation, not tested in production.

2) The hysteresis voltage of Schmitt trigger switching level.

3) In case of reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

4) The pull-up and pull-down resistors are MOS resistors.

Output drive current

GPIO (General Purpose Input /Output Port) can input or output up to ±20mA current.

- In user applications, the number of I/O pins must ensure that the drive current cannot exceed the absolute maximum ratings given in section 4.2:
- The sum of the current drawn by all I/O ports from V_{DD}, plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the current drawn by all I/O ports and output from VSS, plus the maximum operating current output by the MCU on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 11 General operating condition. All I/O ports are CMOS compatible.

Table 28 Output voltage static characteristics (3)

SPEED	Symbol	Parameter	Conditions	Typical	Unit
11 (50MHz)	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 6mA, V_{DD} =2.0V	0.41	V
	V_{OH}(2)	Output high voltage		1.31	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 6mA, V_{DD} =3.3V	0.21	
	V_{OH}(2)	Output high voltage		3.00	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 6mA, V_{DD} =5.0V	0.15	
	V_{OH}(2)	Output high voltage		4.79	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 8mA, V_{DD} =2.0V	0.64	
	V_{OH}(2)	Output high voltage		-	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 8mA, V_{DD} =3.3V	0.29	
	V_{OH}(2)	Output high voltage		2.88	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 8mA, V_{DD} =5.0V	0.21	
	V_{OH}(2)	Output high voltage		4.71	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 20mA, V_{DD} =2.0V	-	
	V_{OH}(2)	Output high voltage		-	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 20mA, V_{DD} =3.3V	0.94	
	V_{OH}(2)	Output high voltage		1.78	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 20mA, V_{DD} =5.0V	0.55	
	V_{OH}(2)	Output high voltage		4.20	
10 (2MHz)	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 6mA, V_{DD} =2.0V	0.18	
	V_{OH}(2)	Output high voltage		1.73	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 6mA, V_{DD} =3.3V	0.11	
	V_{OH}(2)	Output high voltage		3.15	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 6mA, V_{DD} =5.0V	0.08	
	V_{OH}(2)	Output high voltage		4.88	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 8mA, V_{DD} =2.0V	0.26	
	V_{OH}(2)	Output high voltage		1.61	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 8mA, V_{DD} =3.3V	0.15	
	V_{OH}(2)	Output high voltage		3.09	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 8mA, V_{DD} =5.0V	0.11	
	V_{OH}(2)	Output high voltage		4.84	
	V_{OL}(1)	Output low voltage	$\|I_{IO}\|$= 20mA, V_{DD} =2.0V	1.76	

SPEED	Symbol	Parameter	Conditions	Typical	Unit
	V_{OH}(2)	Output high voltage		-	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 20mA, V_{DD} =3.3V	0.4	
	V_{OH}(2)	Output high voltage		2.72	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 20mA, V_{DD} =5.0V	0.28	
	V_{OH}(2)	Output high voltage		4.59	
01 (10MHz)	V_{OL}(1)	Output low voltage	|I_{IO}|= 6mA, V_{DD} =2.0V	0.18	
	V_{OH}(2)	Output high voltage		1.73	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 6mA, V_{DD} =3.3V	0.11	
	V_{OH}(2)	Output high voltage		3.15	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 6mA, V_{DD} =5.0V	0.08	
	V_{OH}(2)	Output high voltage		4.89	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 8mA, V_{DD} =2.0V	0.26	
	V_{OH}(2)	Output high voltage		1.61	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 8mA, V_{DD} =3.3V	0.15	
	V_{OH}(2)	Output high voltage		3.09	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 8mA, V_{DD} =5.0V	0.11	
	V_{OH}(2)	Output high voltage		4.84	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 20mA, V_{DD} =2.0V	1.66	
	V_{OH}(2)	Output high voltage		-	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 20mA, V_{DD} =3.3V	0.40	
	V_{OH}(2)	Output high voltage		2.72	
	V_{OL}(1)	Output low voltage	|I_{IO}|= 20mA, V_{DD} =5.0V	0.28	
	V_{OH}(2)	Output high voltage		4.59	

1) The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.

2) The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.

3) Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are shown in Figure 18 and Table 28, respectively.

Unless otherwise specified, the parameter listed in Table 28 is measured by the ambient temperature and supply voltage in accordance with the condition in Table 11.

Table 29 Input and output AC characteristics (1) (2)

MODEx[1：0] configuration	Symbol	Parameter	Condition	Typical value	Unit
11	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF VDD=3.3V	7.2	ns
	$t_{r(IO)out}$	Output low to high level rise time		7.2	ns
10	$t_{f(IO)out}$	Output high to low level fall time		4.4	ns
	$t_{r(IO)out}$	Output low to high level rise time		4.4	ns
01	$t_{f(IO)out}$	Output high to low level fall time		3.73	ns
	$t_{r(IO)out}$	Output low to high level rise time		3.73	ns

1) I/O port speed can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in the Chip Reference Manual.

2) Guaranteed by design, not tested in production

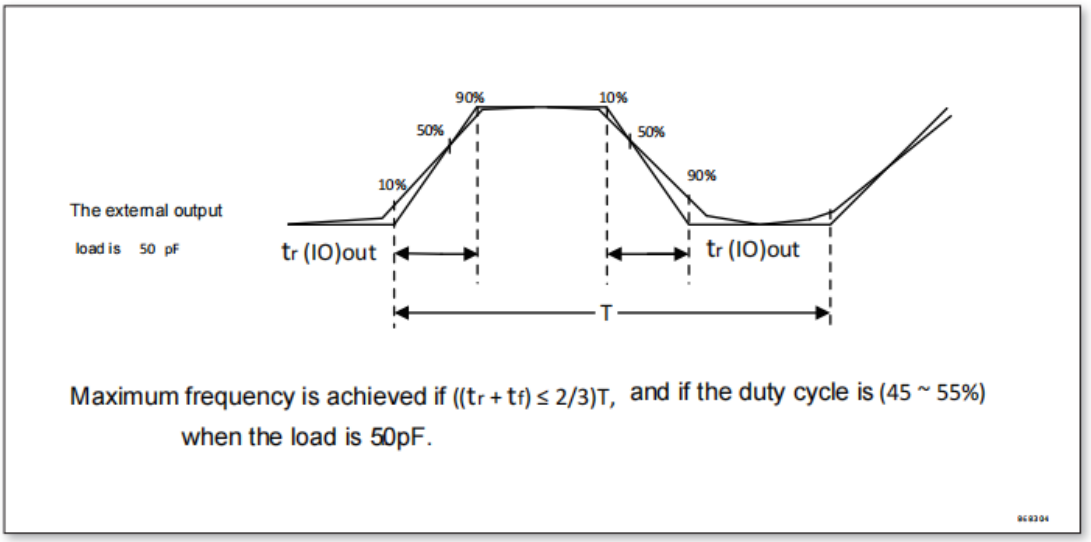

Figure 18 Definition of input and output AC characteristics

4.3.11 NRST Pin Characteristics

NRST pin input driver uses CMOS technology, and it is connected with a pull-up resistor, R_{PU}.

Table 30 NRST pin characteristics (1)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$V_{IL\ (NRST)}$	NRST input low level voltage	-0.3	-	0.8	V
$V_{IH\ (NRST)}$ (2)	NRST input high level voltage	2	-	V_{DD}	V
$V_{hys\ (NRST)}$	NRST Schmitt trigger voltage hysteresis	0.1*VDD	-	-	V
$V_{F\ (NRST)}$ (3)	NRST input filtered pulse	-	-	1.0	uS
$V_{NF\ (NRST)}$ (3)	NRST input non-filtered pulse	4.0	-	-	uS

1) Guaranteed by design, not tested in production

2) The pull-up resistor is a MOS resistor.

3) 5.1KΩ pull-up resistor is required externally when using NRST function.

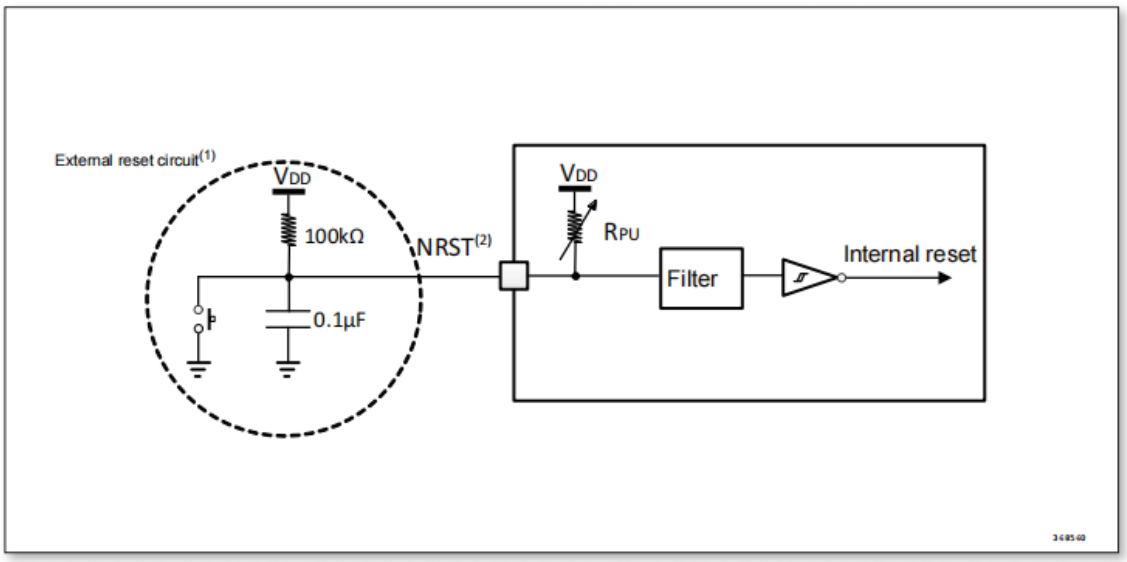

Figure 19 Recommended NRST pin protection

1) The reset network is to prevent parasitic reset.
2) The user must ensure that the NRST pin voltage can be lower than the maximum $V_{IL(NRST)}$ listed in Table 30, otherwise the MCU cannot be reset.

4.3.12 TIM Timer Characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input/output multiplex function pins (output compare, input capture, external clock, PWM output), see section 4.3.10.

Table 31 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{res\ (TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$ (2)
		$f_{TIMxCLK}$ = 48MHz	20.8	-	nS
f_{EXT}	CH1 to CH4 timer external clock frequency	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	Bit
$t_{COUNTER}$	When selecting the internal clock, the 16-bit counter clock cycle	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365	µS
t_{MAX_COUNT}	Maximum possible count (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	1365	uS

1) TIMx is a generic name.
2) $f_{TIMxCLK}$ value varies linearly with f_{EXT}, $t_{COUNTER}$ and t_{MAX_COUNT}.

4.3.13 Communication Interface

I2C Interface Characteristics

Unless otherwise specified, the parameters listed in Table 31 are measured when the

ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage meet the condition of Table 11.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: SDA and SCL are not "true open-drain" pins. When it's configured as open-drain output, the PMOS between the pin and V_{DD} is turned off, but it still exists.

I2C interface characteristics are listed in Table 31. For details on the characteristics of input/output multiplex function pins (SDA and SCL), see section 4.3.10.

Table 32 I2C interface characteristics (1) (2)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Minmum value	Maximum value	Minimun value	Maximum value	
$t_{w\ (SCLL)}$	SCL clock low time	8*t_{PCLK}	-	8*t_{PCLK}	-	μs
$t_{w\ (SCLH)}$	SCL clock high time	6*t_{PCLK}	-	6*t_{PCLK}	-	μs
$t_{su\ (SDA)}$	SDA establishment time	2*t_{PCLK}	-	2*t_{PCLK}	-	ns
$t_{h\ (SDA)}$ (3)	SDA data retention time	0	-	0	875	ns
$t_{r\ (SDA)}$ $t_{r\ (SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f\ (SDA)}$ $t_{f\ (SCL)}$ (4)	SDA and SCL fall time	-	300	-	300	ns
$t_{h\ (STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	μs
$t_{su\ (STA)}$	Repeated start condition establishment time	6*t_{PCLK}	-	6*t_{PCLK}	-	μs
$t_{su\ (STO)}$	Stop condition establishment time	6*t_{PCLK}	-	6*t_{PCLK}	-	μs
$t_{w\ (STO:STA)}$	Time from stop condition to start condition (Bus Free)	5*t_{PCLK}	-	5*t_{PCLK}	-	μs
C_b	Capacitive load of each bus	-	400	-	400	pF

1) Guaranteed by design, not tested in production.

2) To reach the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 3MHz. To reach the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 12MHz.

3) If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the start condition needs to be met.

4) In order to cross the undefined area of the falling edge of SCL, a hold time of at least 300nS on the SDA signal must be guaranteed inside the MCU.

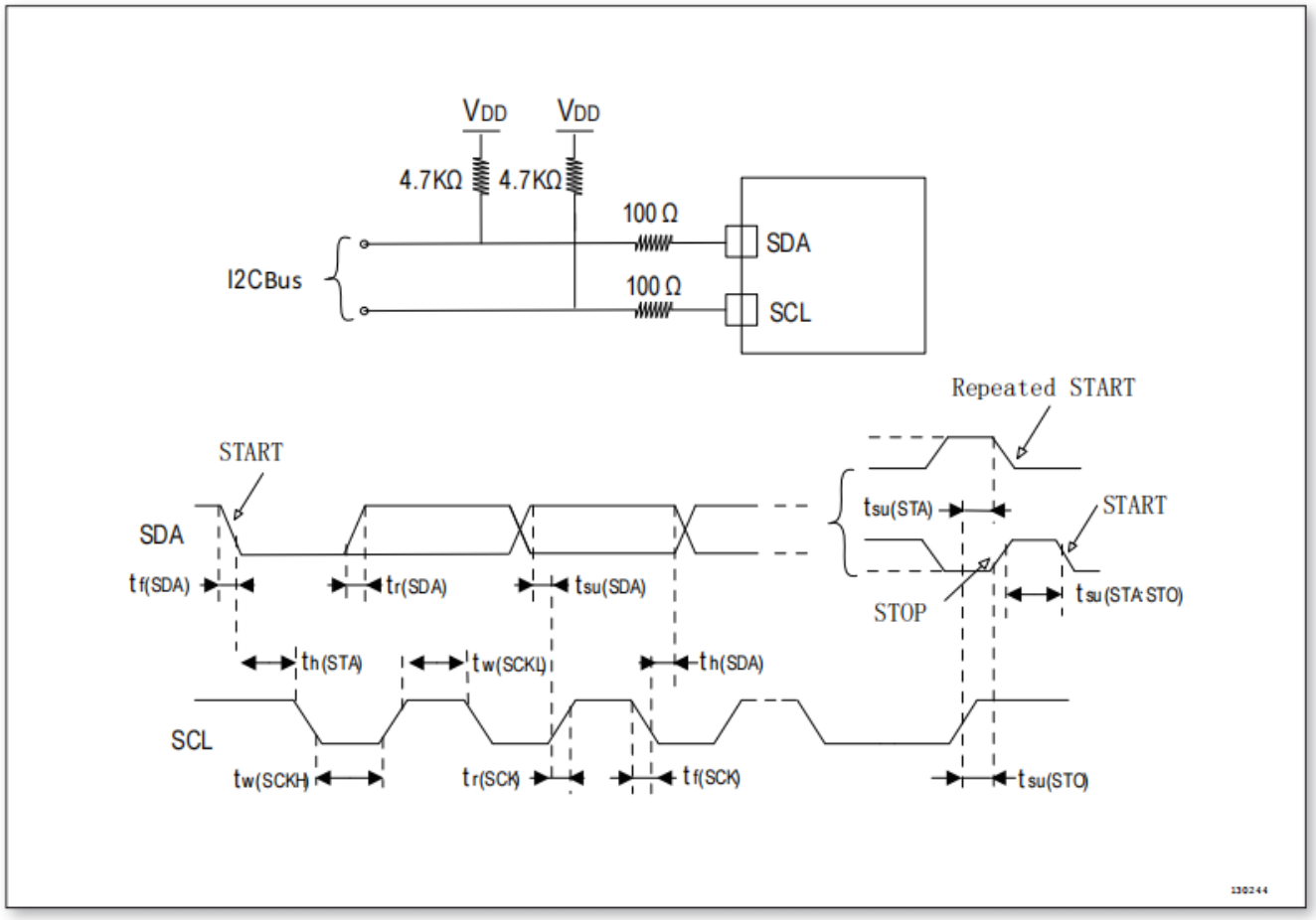

Figure 20 I2C bus AC waveform and measurement circuit (1)

1) The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

SPI interface characteristics

Unless otherwise specified, the parameters listed in Table 32 are measured when ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage meet the condition in Table 11.

For details on the characteristics of input/output multiplex function pins (NSS, SCK, MOSI, MISO), see section 4.3.10.

Table 33 SPI interface characteristics

Symbol	Parameter	Condition	Minimum value (2)	Maximum value (3)	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	24	MHz
		Slave mode		12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C= 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C= 15pF	-	6	nS
$t_{su(NSS)}$ (1)	NSS establishment time	Slave mode	1Tpclk	-	nS
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	1Tpclk	-	nS
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)}/2$ - 6	$t_{c(SCK)}/2$ - 6	nS
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)}/2$ - 6	$t_{c(SCK)}/2$ - 6	nS

Symbol	Parameter	Condition	Minimum value (2)	Maximum value (3)	Unit
$t_{su\ (MI)}$ (1)	Data input establishment time	Main mode, f_{PCLK} = 48MHz, prescaler coefficient = 2, fast-speed mode	12	-	nS
$t_{su\ (SI)}$ (1)		Slave mode	5	-	nS
$t_{h\ (MI)}$ (1)	Data input hold time	Main mode, f_{PCLK} = 48MHz, prescaler coefficient = 2, fast-speed mode	0	-	nS
$t_{h\ (SI)}$ (1)		Slave mode	6	-	nS
$t_{a\ (SO)}$ (1) (2)	Data output valid time	Slave mode (after enabling edge) Not fast-speed mode	-	34	nS
		Slave mode (after enabling edge) Fast-speed mode	-	13	nS
$t_{v\ (MO)}$ (1)	Data output valid time	Master mode (after enabling edge)	-0.6	-	nS

1) Drawn from comprehensive evaluation.

2) Minimum value indicates the drive output minimum time, and maximum value indicates the maximum time to obtain data correctly.

3) Minimum value represents the minimum time to close output, and maximum value represents the maximum time to put the data line in the high impedance state.

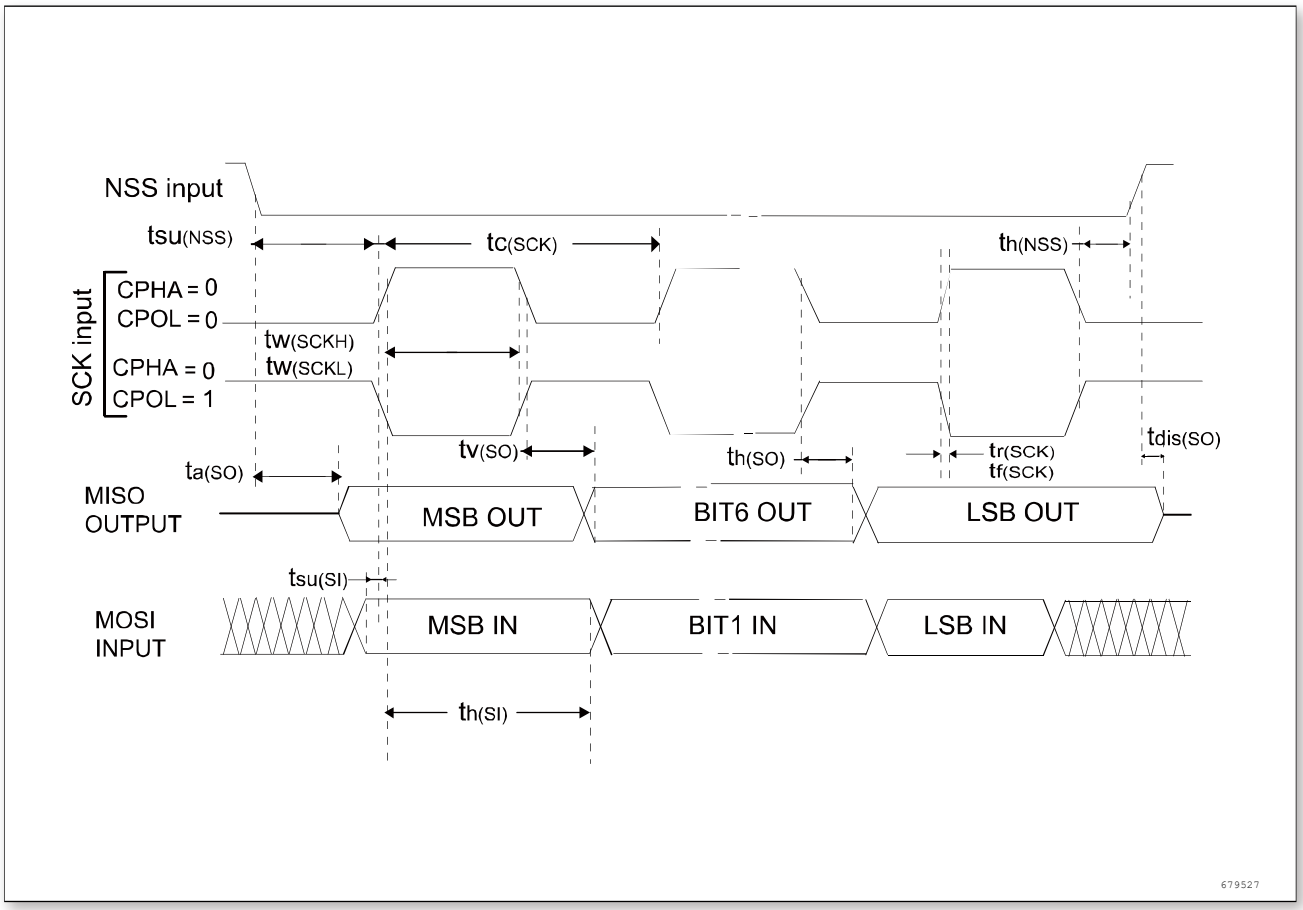

Figure 21 SPI waveform-slave mode and CPHA = 0, SPI_CCTL.CPHASEL=1

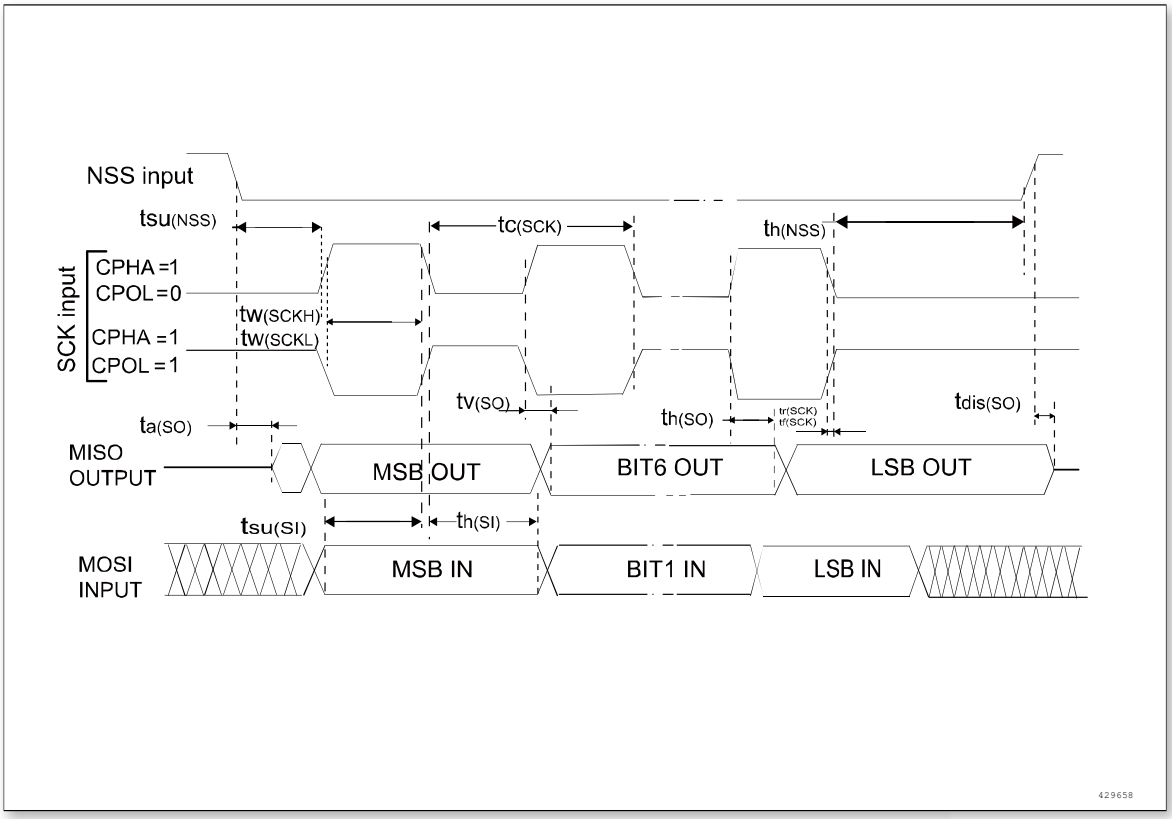

Figure 22 SPI waveform-slave mode and CPHA = 1 (1), SPI_CCTL.CPHASEL=1

1) Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

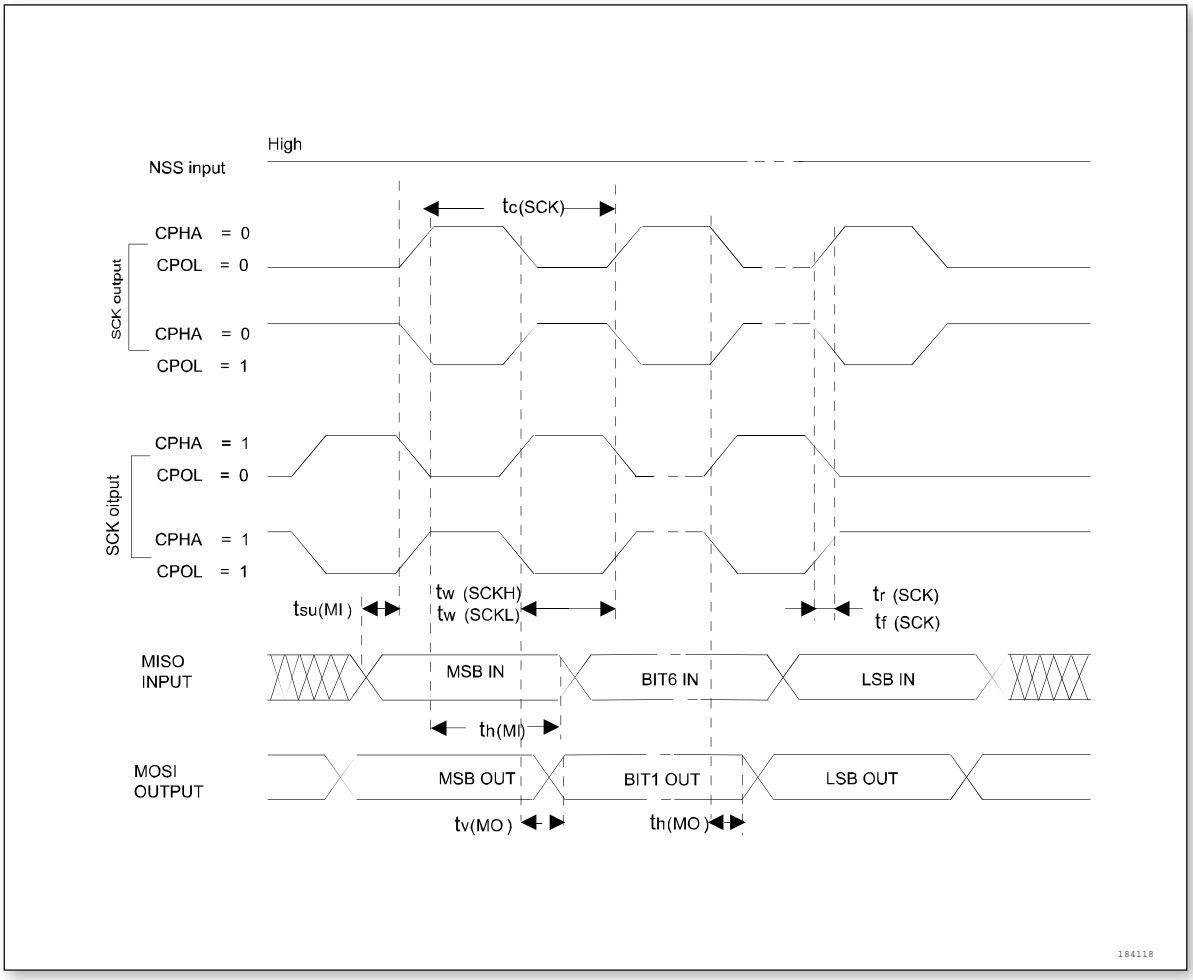

Figure 23 SPI waveform-master mode and SPI_CCTL.CPHASEL=1

1) Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.14 12 bit ADC Characteristics

Unless otherwise specified, the parameters in the following table are measured at ambient temperature, fPCLK1 frequency and VDD supply voltage meet the condition of Table 11.

Table 34 ADC characteristics (1)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
VDD	Supply voltage	-	2.5	-	5.5	V
f_{ADC} (3)	ADC clock frequency	-	-	-	16	MHz
f_S (3)	Sampling rate	-	-	-	1	MHz
f_{TRIG}	External trigger frequency (3)	fADC = 16MHz	-	-	941	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	VDD	V
R_{AIN}	External input impedance	-	See formula 1 and the following table			kΩ
R_{ADC}	Sampling switch resistance	-	-	-	1.5	kΩ

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	-	10	pF
t_S	Sampling time	fADC = 16MHz	0.156	-	15.031	μS
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (Including sampling time)	fADC = 16MHz	1	-	15.875	μS
		-	15 ~ 253 (sampling tS + stepwise approximation to 12.5)			$1/f_{ADC}$

1) Guaranteed by comprehensive evaluation, not tested in production

2) Guaranteed by design, not tested in production.

3) For external trigger, a delay of $1/f_{ADC}$ must be added to the delay.

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

Formula 1

Table 35 Maximum R_{AIN} when f_{ADC}=15MHz (1)

T_S (cycle)	t_S (μS)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1) Guaranteed by design, not tested in production.

Table 36 ADC accuracy (1) (2)

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
Resoluion	Resolution		12	-	Bit
ET	Composite error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	+2/-7	-	LSB
EO	Offset error		4.5	-	
EG	Gain error		-2	-	
ED	Differential linearity error		3/-0.8	-	
EL	Integral linearity error		+4.5/-3.5	-	

1) Correlation between ADC accuracy and reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, because this will significantly reduce the accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$, it will not affect the ADC accuracy.

2) Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: the maximum deviation between the actual and ideal transmission curves.

EO = Offset error: the deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: the deviation between the last ideal conversion and the last actual conversion.

ED = Differential linearity error: the maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: the maximum deviation between any actual conversion and the endpoint correlation line.

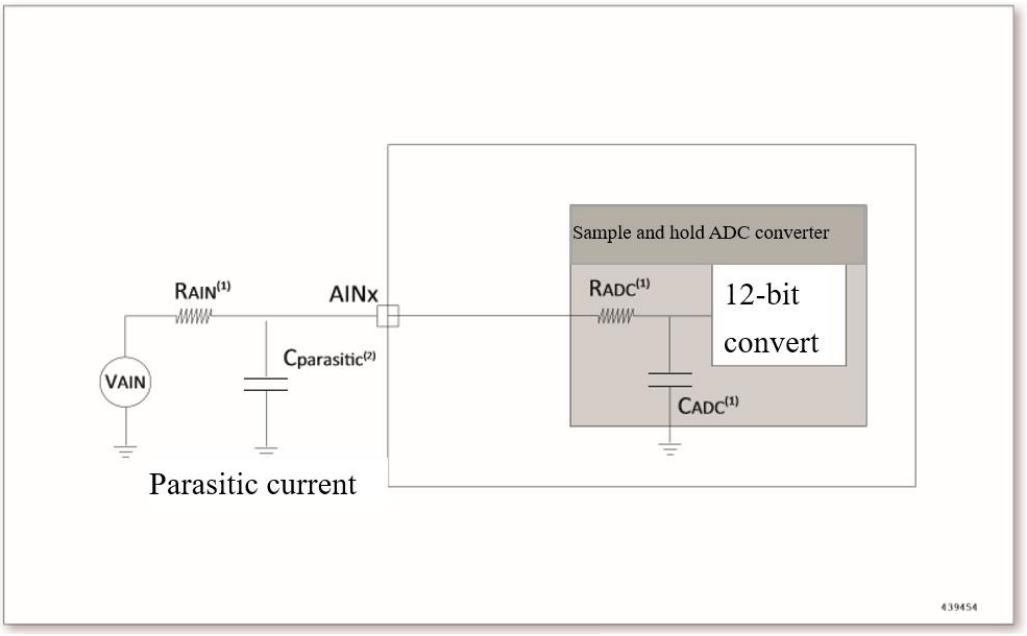

Figure 24 Typical connection diagram using ADC

1) Refer to Table 34 for the values of R_{AIN}, R_{DAC} and C_{ADC}.
2) Cparasitic means the parasitic capacitance (about 7pF) on the PCB (related to soldering and PCB layout quality) and pad. A larger Cparasitic value will reduce the conversion accuracy. The solution is to reduce f_{ADC}.

PCB design recommendations

The power supply decoupling must be connected according to the diagram below. The 10 nF capacitor in the diagram must be ceramic capacitors, which should be placed as close as possible to the MCU chip.

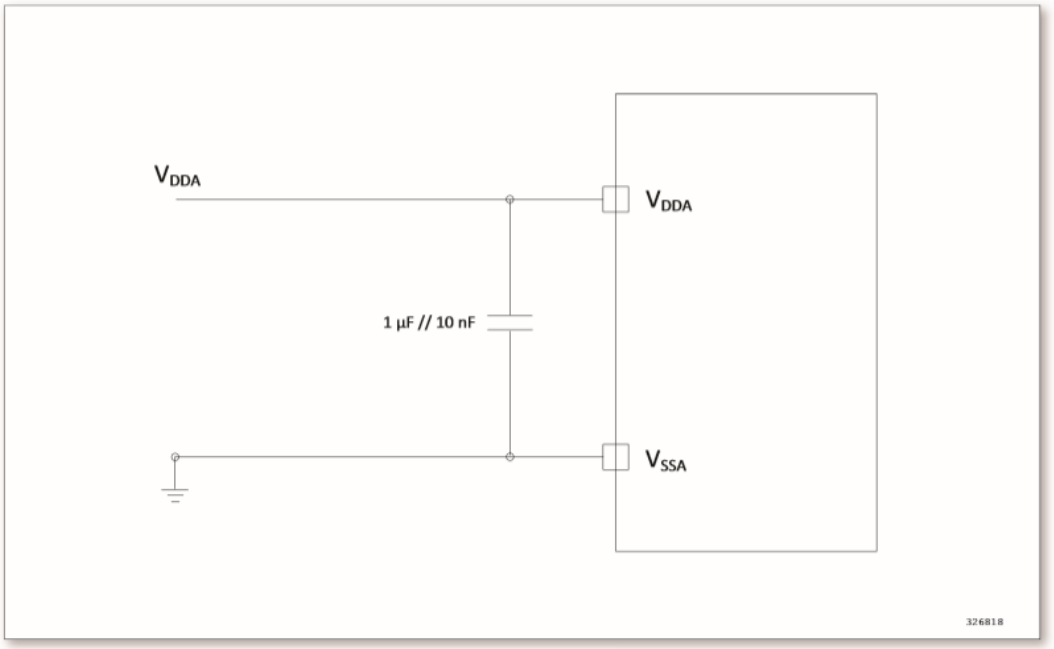

Figure 25 Decoupling circuit of power supply and reference power supply

5 Package Characteristics

5.1 Package TSSOP20

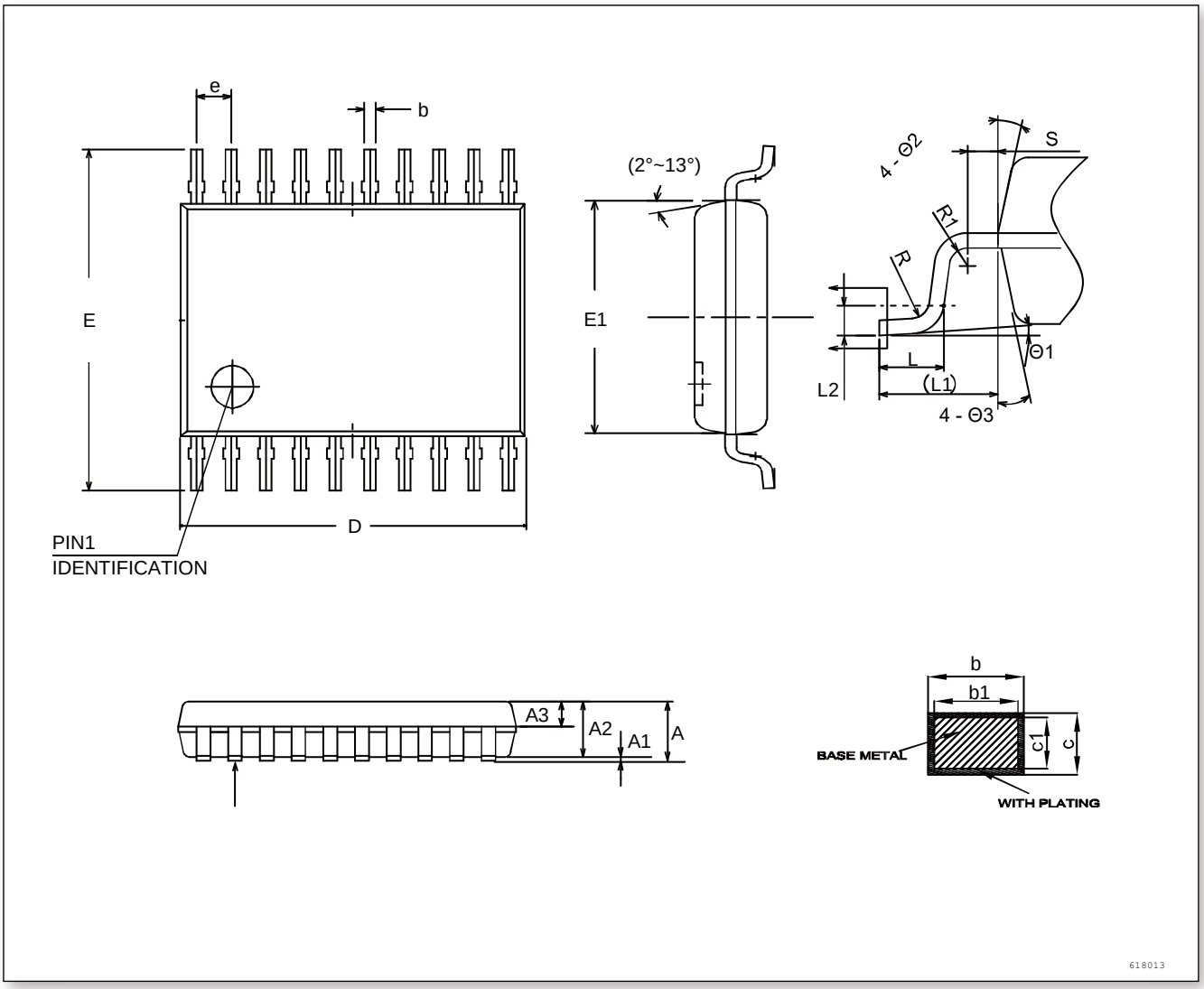

Figure 26 TSSOP20, 20-pin low profile rectangular flat package

1) The Diagram is not drawn to scale.
2) The size is in mm.

Table 37 TSSOP20 dimension description

Lable	mm		
	Minimum value	Typical value	Maximum value
A	-	-	1.20
A1	0.05	-	0.15
A2	-	-	1.05
A3	0.34	-	0.54
b	0.20	-	0.28
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.60
E	6.20	6.40	6.60
E1	-	4.35	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0°	-	8°

5.2 Package SOP8

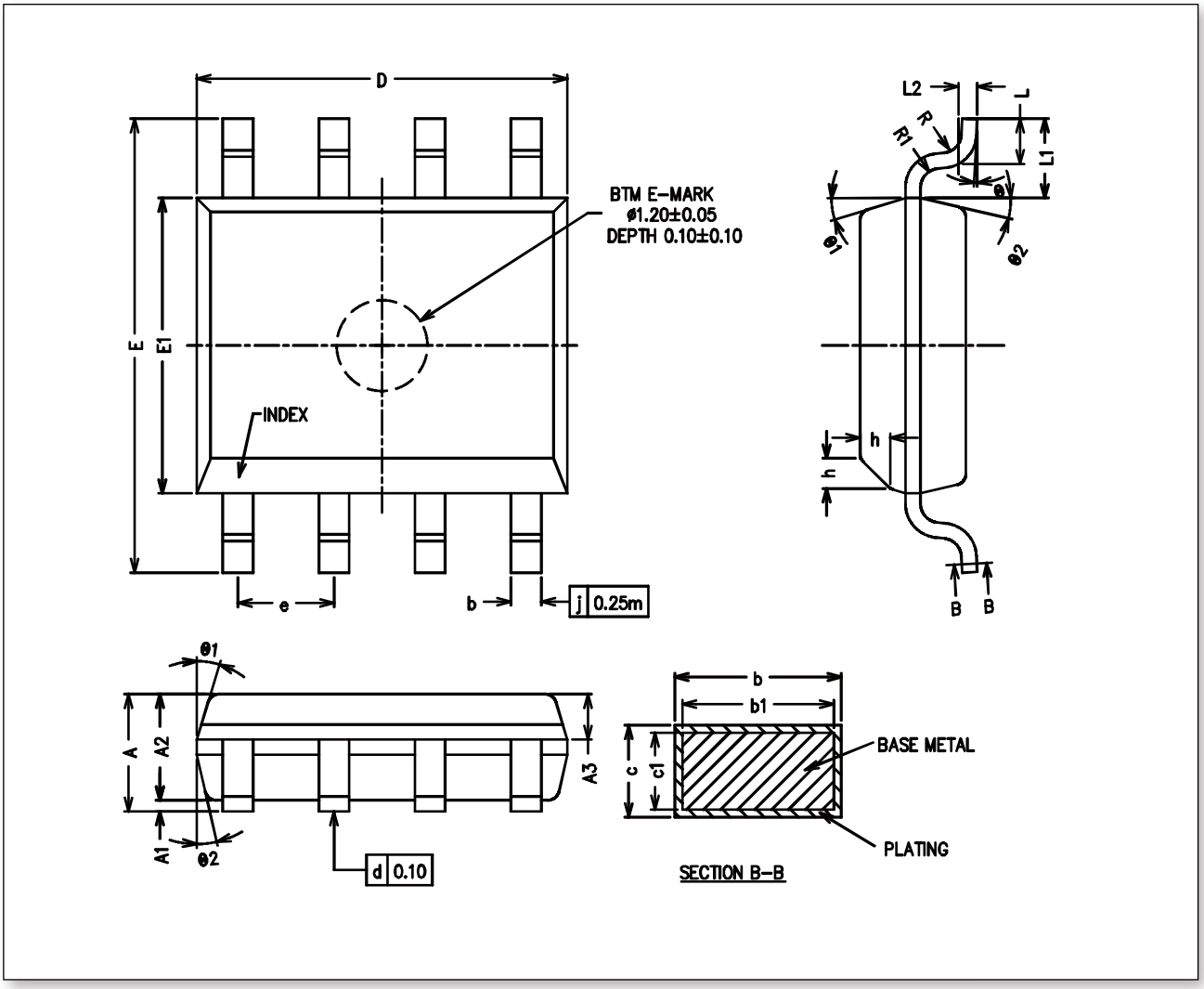

Figure 27 SOP8, 8-pin small outline package

1) The Diagram is not drawn to scale.
2) The size is in mm.

Table 38 SOP8 size description

Lable	mm		
	Minimum value	Typical value	Maximum value
A	1.35	1.55	1.75
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	-	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	-	-
R1	0.07	-	-
θ	0°	-	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

5.3 Package QFN20

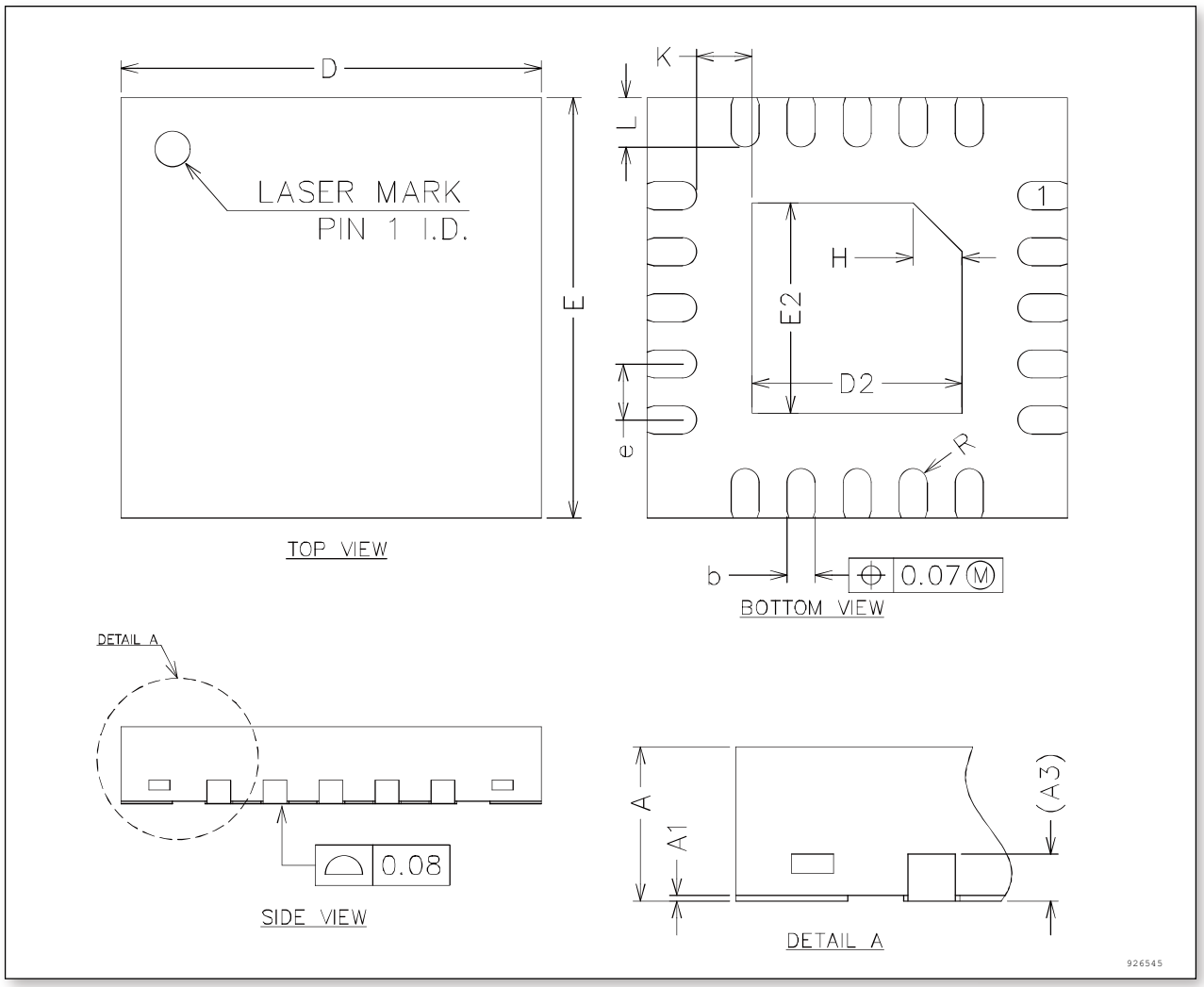

Figure 28 QFN20, 20-pin square flat cordless package exterior

1) The Diagram is not drawn to scale.
2) The size is in mm.

Table 39 QFN20 size description

Label	mm		
	Minimum value	Typical value	Maximum value
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.152REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H	0.35REF		
K	0.40REF		
L	0.25	0.35	0.45
R	0.075		
N	Pin number = 20		

6 Model Naming Rule

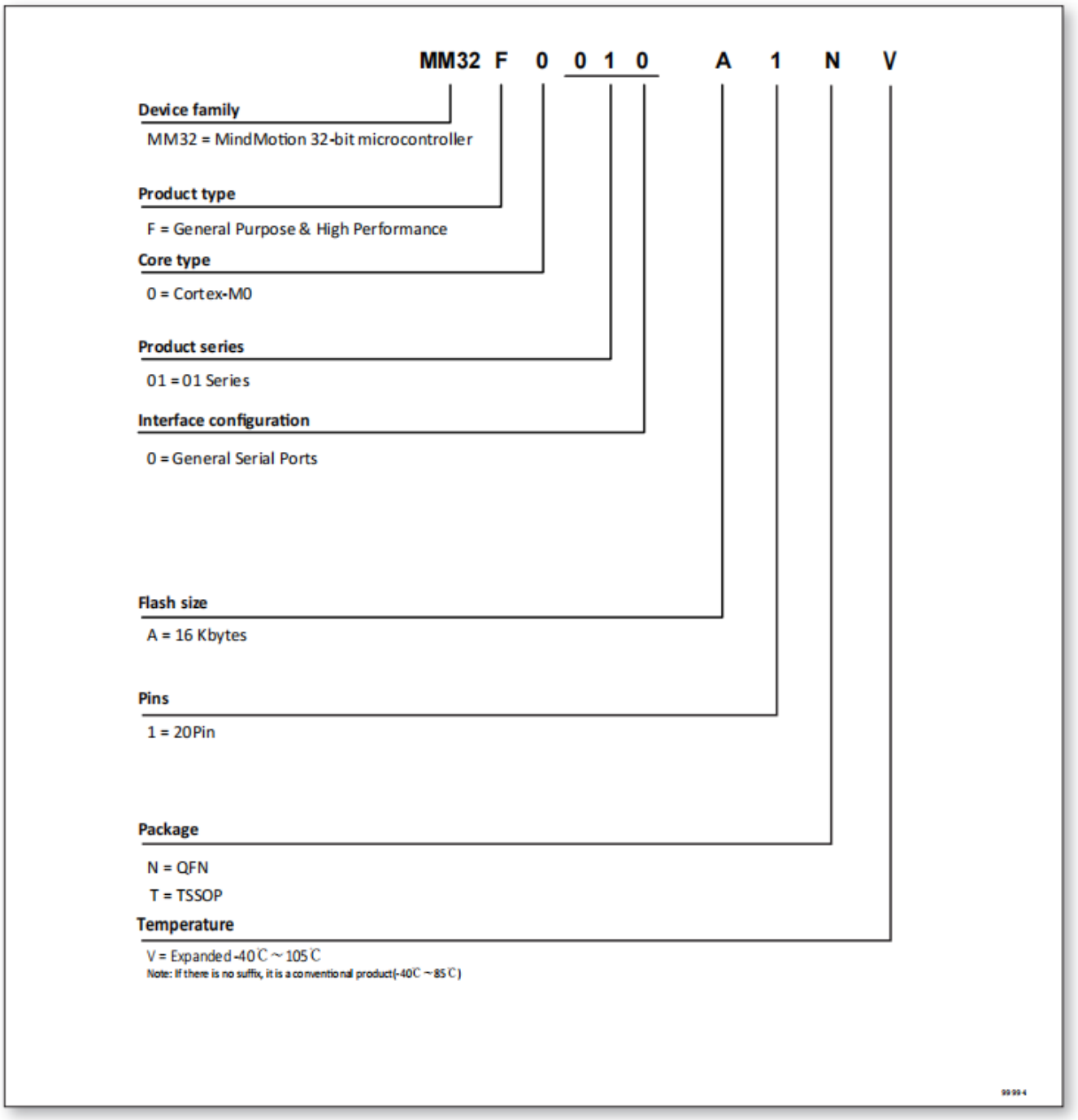

Figure 29 MM32 model naming

7 Abbreviations

ADC	Analog Digital Converter
CRC	Cyclic Redundancy Check
EXTI	External Interrupt Event Controller
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FLASH	Flash Memory
GPIO	General-Purpose Input/Output
HSE	External High Speed Clock
HSI	Internal High Speed Clock
I2C	Inter-Integrated Circuit
IWDG	Independent Watchdog
LP	Low Power
LSI	Internal Low Speed Clock
NVIC	Nested Vectored Interrupt Controller
PWR	Power Control
POR	Power On Reset
PDR	Power Down Reset
PVD	Programmable Voltage Detector
RCC	Reset Clock Controller
SRAM	Static Random Access Memory
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug Interface
SysTick	System Tick Timer
TIM	Timer
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

8 Revision History

Table 40 Revision history

Date	Version	Content
2023/09/08	Rev 1.14	1. Added Output voltage static characteristics (3)
2023/04/18	Rev 1.12	1. Updated Figure 11 Scheme of power supply
2022/03/28	Rev 1.11	1. Added $R_{JA\text{-}QFN20}$ information 2. Added the maximum value of low power mode
2022/03/03	Rev 1.10	1. Updated marking information
2022/01/25	Rev 1.09	1. Updated the maximum value of voltage characteristics 2. Added nRST
2021/11/23	Rev 1.08	1. Updated marking information
2021/07/22	Rev 1.07	1. Updated TSSOP20 package information
2021/07/05	Rev 1.05	1. Updated system block diagram 2. Updated ESD characteristics table 3. Upated working condition table during power-on and power-down
2021/04/08	Rev 1.04	1. Added SOP8 package information
2021/01/14	Rev 1.03	1. Modified parameters of electrical characteristics
2020/10/19	Rev 1.02	1. Modified parameters of electrical characteristics 2. Modified model naming figure
2020/09/08	Rev 1.01	1. Modified specifications
2020/07/02	Rev 1.00	1. Formal version