Data Sheet

MM32F0130

Arm® Cortex®-M0 based 32-bit Microcontrollers

Revision: 2.24

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1 Introduction

1.1 Overview

The MM32F0130 microcontrollers are based on Arm® Cortex®-M0 core. These devices have a maximum clocked frequency of 72MHz, built-in 64KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, two analog comparators, one 16-bit advanced timer, one 16-bit and one 32-bit general purpose timers and three 16-bit basic timers, as well as communication interfaces including one I2C, two SPI, two UART, one USB interface and one CAN interface.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) includes the industrial tier -40°C to 85°C and the extended industrial tier -40°C to 105°C (Suffix V). Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Motor drive and application control
- Medical and hand-hold devices
- PC game peripherals and GPS platforms
- Industrial applications: programmable logic controllers (PLC), frequency converters, printers and scanners
- Alarm systems, video intercom systems, heating, ventilation and air conditioning systems

This product series is available in LQFP64, LQFP48, LQFP32, QFN32 and QFN28 packages.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M0.
  - Frequency up to 72MHz.
- Memory
  - Up to 64KB embedded Flash storage.
  - Up to 16KB SRAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.

  - Power-on and Power-down reset (POR/PDR), Brown-out reset (BOR), Programmable voltage detector (PVD).
  - POR reset voltage is as low as 1.7V.
  - PVD voltage threshold can be as low as 1.8V.
  - 2 to 24MHz high speed crystal oscillator.
  - Embedded 48 MHz high speed oscillator with factory calibration
  - Internal 40KHz low speed oscillator
  - PLL supports CPU operating at a frequency of up to 72MHz
  - External 32.768KHz low speed oscillator
- Low power
  - Multiple low power modes, including sleep, stop and standby
- One 12-bit analog-to-digital converter (ADC), 1μs conversion time, up to 10 external input channels
  - Conversion range: 0 ~ V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
- Two comparators
- One DMA controller with 5 channels
  - Supported peripheries include Timer, UART, I2C, SPI, USB, and ADC
- Up to 56 quick I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
- Total 10 timers:
  - One 16-bit and 4-channel advanced control timer providing 4-channel PWM output, with dead zone generation and emergency stop functions
  - One 16-bit general timer and one 32-bit general timer with up to 4 input captures/output compare used for IR control decoding
  - Two 16-bit basic timer with 1 input capture/output compare channel and 1 group of complementary output, dead zone generation, emergency stop, and modulator gate circuit used for IR control
  - One 16-bit basic timer with 1 input capture/output compare channel
  - Two watchdog timers (free IWDG and window WWDG)
  - One Systick timer: 24-bit down counter
  - One RTC real-time clock
- Debug mode
  - Serial wire debug (SWD) port
- Up to 7 digital peripheral interfaces
  - Two UART interfaces

  - One I2C interfaces
  - Two SPI interfaces
  - One CAN interface
  - One USB device interface
- 96-bit unique ID (UID) of the chip
- Adopts LQFP64, LQFP48, LQFP32, QFN32 and QFN28 packages

2 Specification

2.1 Model list

2.1.1 Ordering information

Table 2-1 Ordering information

Part numbers / Features		MM32F0131C7P/ MM32F0132C7P/ MM32F0133C7P	MM32F0131C6P/ MM32F0132C6P/ MM32F0133C6P	MM32F0131C4P/ MM32F0132C4P/ MM32F0133C4P	MM32F0131C4Q/ MM32F0132C4Q/ MM32F0133C4Q	MM32F0131C3N
CPU frequency		72 MHz				
Flash - KB		64	64	64	64	64
SRAM - KB		16	16	16	16	16
Timers	16-bit GP	1	1	1	1	1
	32-bit GP	1	1	1	1	1
	Basic	3	3	3	3	3
	Advanced	1	1	1	1	1
Communication interfaces	UART	2	2	2	2	2
	I2C	1	1	1	1	1
	SPI	2	2	1	1	1
	USB	-/1/1	-/1/1	-/1/1	-/1/1	-
	CAN	-/-/1	-/-/1	-/-/1	-/-/1	-
GPIO		56	39	25	27	23
12-bit ADC	Modules	1	1	1	1	1
	Channels	10	10	10	10	10
Comparators		2				
RTC		√				
Supply voltage		2.0V ~ 5.5V				
Package		LQFP64	LQFP48	LQFP32	QFN32	QFN28

2.1.2 Marking information

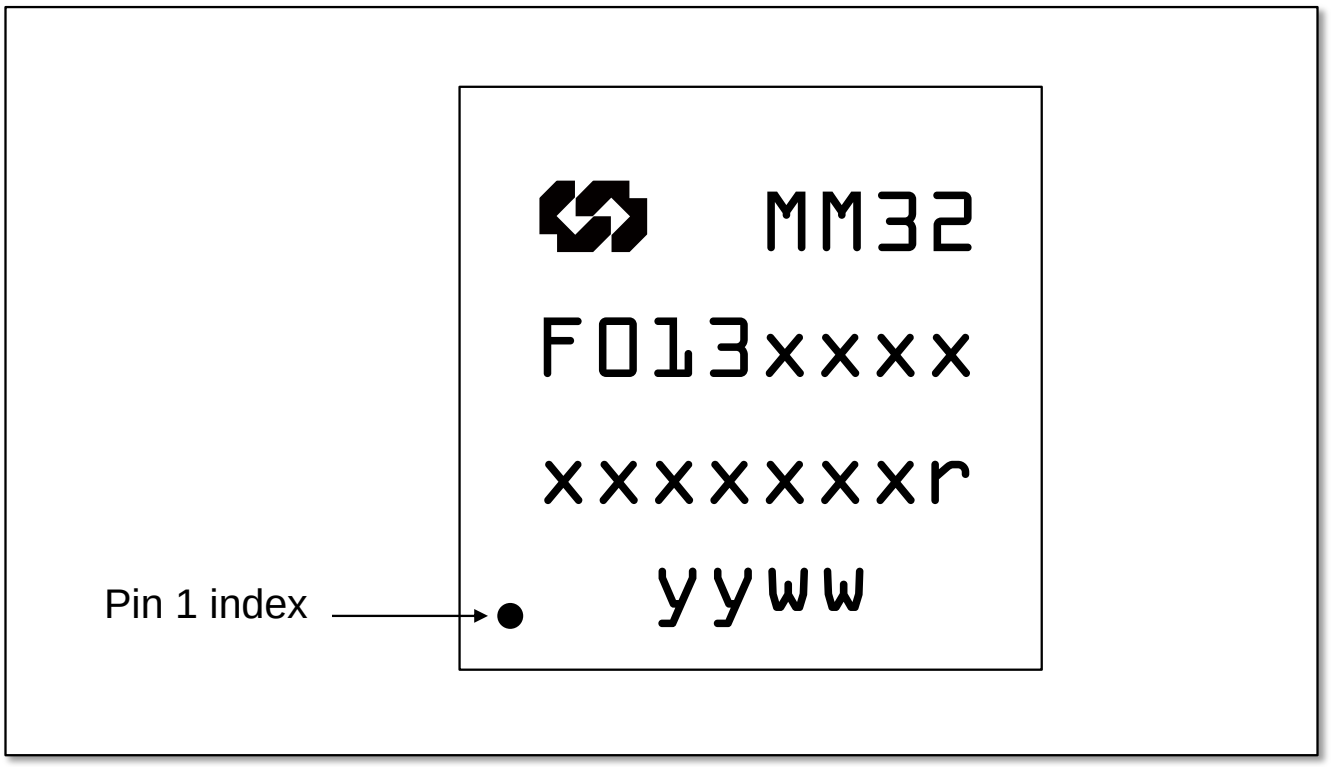

Figure 2-1 LQFP and QFN package marketing

LQFP and QFN package have the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F013xxxx
  - Second part of product name.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision. For engineering samples, the prefix 2 digital of the Trace code is labelled as “ES”.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.1.3 Block diagram

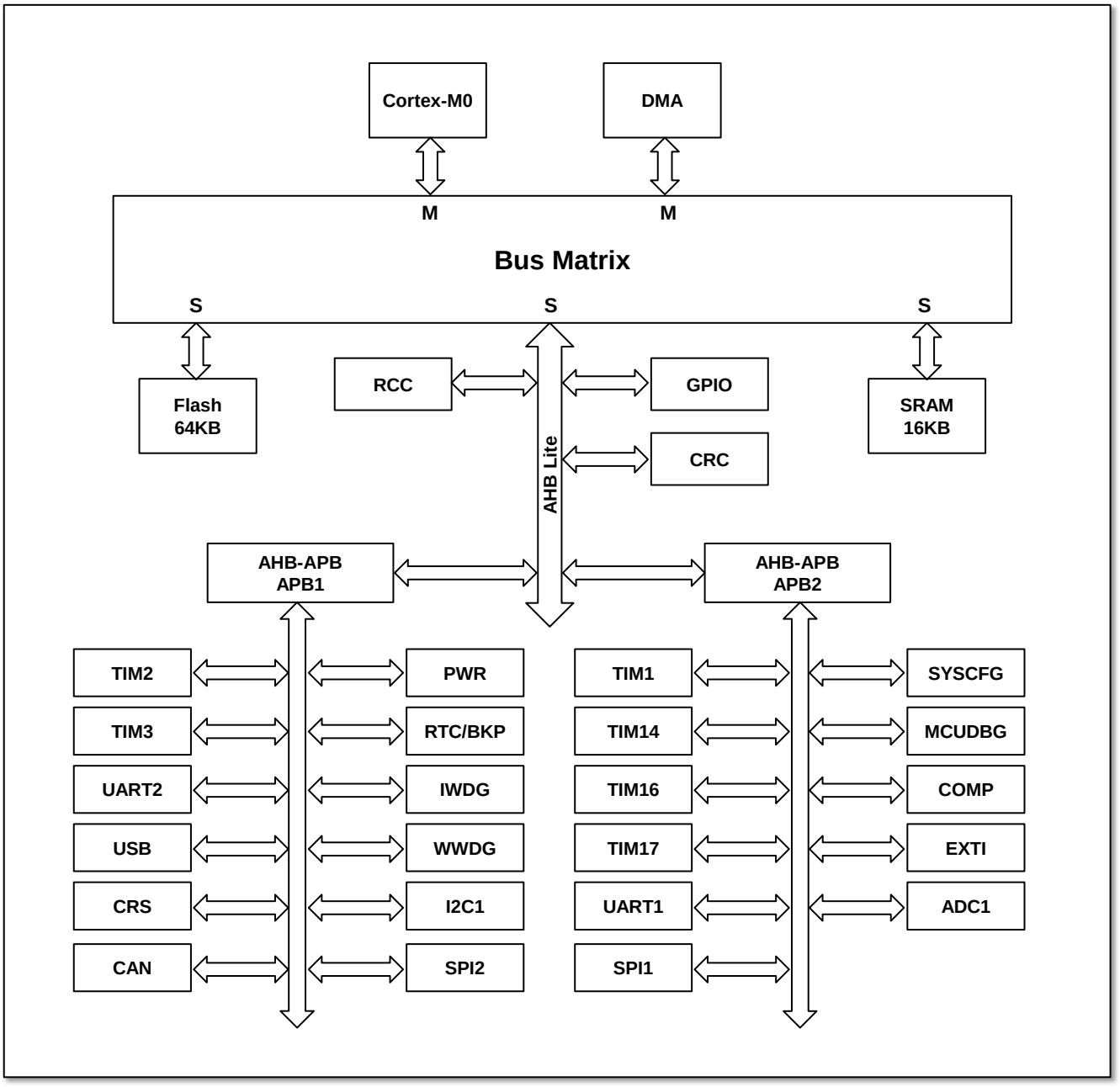

Figure 2-2 System block diagram

2.2 Functional description

2.2.1 Core introduction

The Arm® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The Arm® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded Arm core, this product is compatible with all the tools and software for Arm-based products.

2.2.2 Memory map

Table 2-2 Memory map

Bus	Address	Size	Peripherals
FLASH	0x0000 0000–0x0000 FFFF	64 KB	Main flash memory/system memory or SRAM configuration inseparable from BOOT
	0x0001 0000–0x07FF FFFF	~ 128 MB	Reserved
	0x0800 0000–0x0800 FFFF	64 KB	Main Flash memory
	0x0801 0000–0x1FFD FFFF	~ 383 MB	Reserved
	0x1FFE 0000–0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200–0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000–0x1FFE 1BFF	3 KB	Reserved
	0x1FFE 1C00–0x1FFF F3FF	~ 256 MB	Reserved
	0x1FFF F400–0x1FFF F7FF	1 KB	System memory
	0x1FFF F800–0x1FFF F80F	16 B	Option bytes
	0x1FFF F810–0x1FFF FFFF	~2 KB	Reserved
SRAM	0x2000 0000–0x2000 3FFF	16 KB	SRAM
	0x2000 4000–0x2FFF FFFF	~ 255 MB	Reserved
APB1	0x4000 0000–0x4000 03FF	1 KB	TIM2
	0x4000 0400–0x4000 07FF	1 KB	TIM3
	0x4000 0800–0x4000 0BFF	8 KB	Reserved
	0x4000 2800–0x4000 2BFF	1 KB	RTC/BKP
	0x4000 2C00–0x4000 2FFF	1 KB	WWDG
	0x4000 3000–0x4000 33FF	1 KB	IWDG
	0x4000 3400–0x4000 37FF	1 KB	Reserved
	0x4000 3800–0x4000 3BFF	1 KB	SPI2
	0x4000 4000–0x4000 43FF	1 KB	Reserved
	0x4000 4400–0x4000 47FF	1 KB	UART2
	0x4000 4800–0x4000 4BFF	3 KB	Reserved

Bus	Address	Size	Peripherals
	0x4000 5400–0x4000 57FF	1 KB	I2C1
	0x4000 5800–0x4000 5BFF	1 KB	Reserved
	0x4000 5C00–0x4000 5FFF	1 KB	USB
	0x4000 6000–0x4000 63FF	1 KB	Reserved
	0x4000 6400–0x4000 67FF	1 KB	CAN
	0x4000 6800–0x4000 6BFF	1 KB	Reserved
	0x4000 6C00–0x4000 6FFF	1 KB	CRS
	0x4000 7000–0x4000 73FF	1 KB	PWR
	0x4000 7400–0x4000 FFFF	35 KB	Reserved
APB2	0x4001 0000–0x4001 03FF	1 KB	SYSCFG
	0x4001 0400–0x4001 07FF	1 KB	EXTI
	0x4001 0800–0x4001 23FF	7 KB	Reserved
	0x4001 2400–0x4001 27FF	1 KB	ADC1
	0x4001 2800–0x4001 2BFF	1 KB	Reserved
	0x4001 2C00–0x4001 2FFF	1 KB	TIM1
	0x4001 3000–0x4001 33FF	1 KB	SPI1
	0x4001 3400–0x4001 37FF	1 KB	DBGMCU
	0x4001 3800–0x4001 3BFF	1 KB	UART1
	0x4001 3C00–0x4001 3FFF	1 KB	COMP
	0x4001 4000–0x4001 43FF	1 KB	TIM14
	0x4001 4400–0x4001 47FF	1 KB	TIM16
	0x4001 4800–0x4001 4BFF	1 KB	TIM17
	0x4001 4C00–0x4001 7FFF	13 KB	Reserved
AHB	0x4002 0000–0x4002 03FF	1 KB	DMA
	0x4002 0400–0x4002 0FFF	3 KB	Reserved
	0x4002 1000–0x4002 13FF	1 KB	RCC
	0x4002 1400–0x4002 1FFF	3 KB	Reserved
	0x4002 2000–0x4002 23FF	1 KB	Flash Interface
	0x4002 2400–0x4002 2FFF	3 KB	Reserved
	0x4002 3000–0x4002 33FF	1 KB	CRC
	0x4002 3400–0x4002 FFFF	47 KB	Reserved
	0x4003 0000–0x4003 03FF	1 KB	Reserved
	0x4003 0400–0x47FF FFFF	~ 127 MB	Reserved
	0x4800 0000–0x4800 03FF	1 KB	GPIOA
	0x4800 0400–0x4800 07FF	1 KB	GPIOB
	0x4800 0800–0x4800 0BFF	1 KB	GPIOC
	0x4800 0C00–0x4800 0FFF	1 KB	GPIOD
	0x4800 1000–0x5FFF FFFF	~ 384 MB	Reserved

2.2.3 Embedded Flash

Up to 64K bytes of embedded Flash memory available for storing programs and data.

2.2.4 Embedded SRAM

Up to 16K bytes of embedded SRAM.

2.2.5 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to generate a CRC code from one 32-bit data word using a fixed polynomial generator. Among many applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of EN/IEC60335-1, they offer a means of verifying the Flash memory errors. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Nested Vectored Interrupt Controller (NVIC)

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

2.2.8 Clock and boot

Select the system clock after the chip starts. After reset, first use the internal 8 MHz oscillator as the system clock by default, and then select the external 4 ~ 24 MHz clock

source. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. And the associated interrupt monitoring switch, if enabled, will also generate corresponding interrupt request.

Multiple prescalers permit to configure the clock of AHB bus and high-speed APB (APB1 and APB2) bus. The maximum frequency of the AHB and the high-speed APB is 72MHz. Please refer to the clock tree of the clock system in Figure 2-3.

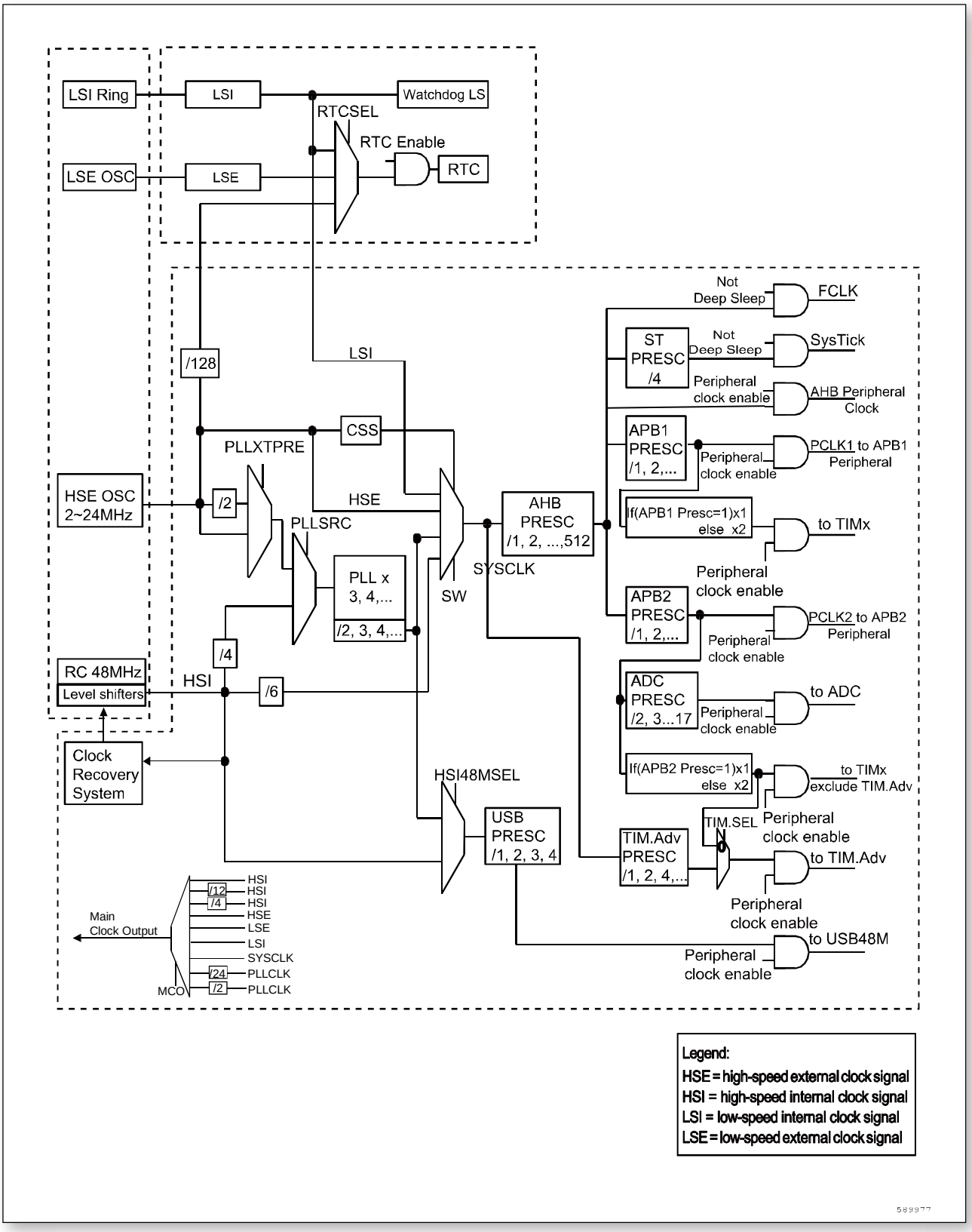

Figure 2-3 Clock tree

2.2.9 Boot modes

At startup, BOOT0 pin and BOOT option bit are used to select one of three boot options:

- Boot from on-chip Flash memory
- Boot from system memory
- Boot from on-chip SRAM

The Bootloader is located in system memory. It is used to reprogram the Flash memory by UART1 after startup from the system memory area.

2.2.10 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} pins.
- V_{DDA} = 2.0V ~ 5.5V (1): ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

1. Note: only when VDDA = 2.5V ~ 5.5V, the analog performance is guaranteed to be consistent with this Data Sheet.

2.2.11 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

2.2.12 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

2.2.13 Low power mode

The device supports low power mode to achieve the best compromise among low-power consumption, short startup time, and multiple wake-up events.

Sleep mode

In sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode permits to achieve the lowest power consumption while keeping the

SRAM and register contents intact. In the Stop mode, the HSI oscillator and HSE crystal oscillator are switched off. The microcontroller can wake up from the Stop mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The Standby mode is used to achieve the lowest power consumption. In the Standby mode, the voltage regulator is switched off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V section are disconnected. PLL, HSI and HSE oscillators are turned off and can be woken up by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. They can also be woken up and reset by the watchdog timer. The contents of SRAM and registers will be lost. Only the backup register and Standby circuit sustain power supply.

2.2.14 DMA

The flexible 5 channel general-purpose DMA can manage data transfer from memory to memory, device to memory, and memory to device; the DMA controller supports the management of ring buffer, avoiding interrupts generated by controller in transferring data to the end of the buffer.

Each channel is connected to fixed hardware DMA requests, and software trigger is also supported on each channel; the transfer length, source address and target address can be independently configured by the software.

DMA can be used for main peripherals such as UART, I2C, SPI, ADC, USB and general/basic/advanced control timer TIMx.

2.2.15 Real-time clock (RTC)

The real-time clock is an independent timer, which provides a set of continuously running counters. It can provide a real calendar function with corresponding software configuration. The current time and date of the system can be reset by modifying the value of the counter. The RTC module and clock configuration system (RCC_BDCR register) are in the backup area, namely, RTC setting and time remain unchanged after the system reset or the wake-up of the Standby mode.

2.2.16 Backup register

The backup register is composed of 20 16-bit registers used to store user application data. They are not reset by a system or power reset, or when the system wakes up from Standby mode.

2.2.17 Timer and watchdog (TIM & WDG)

The device includes one advanced control timer, two general-purpose timers, three basic timers, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general-purpose and basic timers:

Table 2-3 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
Basic	TIM14	16-bit	Up	Any integer between 1 and 65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes

Advanced control timer (TIM1)

Advanced-control timer is composed of one 16-bit counter, 4 capture/compare channels and three-phase complementary PWM generator. It has complementary PWM outputs with programmable inserted dead-times and can also be used as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center- aligned modes)
- One-pulse mode output

When it is configured as a 16-bit universal timer, it has the same function as a TIM2 timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In the debug mode, the counter can be frozen while the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many features are shared with those of the general-purpose TIM timer, using the same architecture, so the advanced-control timer can work together with the TIM timer via the Timer Link feature for synchronization or event chaining.

General purpose timer (TIM2 / TIM3)

There are up to two synchronizable general-purpose timers (TIM2, TIM3) embedded in the device. The timer has one 16/32-bit automatic up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM or single-pulse mode output.

The timers can work together with the advanced control timer for synchronization or

event chaining. The counters can be frozen in debug mode. Any general-purpose timer can be used to produce PWM output. Each timer has an independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1 to 4 Hall sensors. Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

General purpose timer _32-bit

This timer has a 32-bit auto-load up/down counter, a 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output.

General purpose timer _16-bit

This timer has a 16-bit auto-load up/down counter, a 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output.

Basic timer (TIM14 / TIM16 / TIM17)

TIM14

The timer contains one 16-bit automatically reloadable count-up counter and one 16-bit prescaler. It has a single channel for input capture/output comparison, PWM or single pulse output. Its counter can be frozen in the debug mode.

TIM16 / TIM17

Both timers contain one 16-bit automatically reloadable count-up counter and one 16-bit prescaler. Both timers have a single channel for input capture/output comparison, PWM or single pulse output. They have complementary outputs with functions of dead zone generation and independent DMA request generation. In the debug mode, the timers are off.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40KHz internal clock oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used to either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog has a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the entire system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.18 UART interface

The UART interface supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be configured for 5 bit, 6 bit, 7 bit, 8 bit and 9 bit.

All UART interfaces can be served by the DMA.

2.2.19 I2C

The I2C interface can operate in the multi-master mode or slave mode and it supports the standard and fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

2.2.20 SPI

The SPI interface can be configured as 1-32 bits per frame in the slave or master mode.

All SPI interfaces are compatible with DMA.

2.2.21 USB

The product has an embedded device controller compatible with the full-speed USB and follows the full-speed USB device (12 Mbps) standard. The endpoint can be configured by the software. USB-exclusive 48MHz clock can be generated by internal PLL or internal clock source (HSI).

2.2.22 CAN

The CAN interface is compliant with 2.0A and 2.0B (active) specifications with a bit rate up to 1 Mbps. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifier.

2.2.23 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open drain), as input (with/without pull-up/pull-down) or as peripheral alternate function port. Most GPIO pins are shared with digital or analog alternate peripherals.

The peripheral function of the I/O pin can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.24 ADC

The device embeds a 12-bit analog-to-digital converter (ADC), with up to 10 external channels available for single, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs. ADC can be performed by DMA.

The analog watchdog allows the application to monitor one or all selected channels precisely. An interrupt occurs when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timer (TIMx) and advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize ADC conversion with the clock.

2.2.25 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel, which is used to convert the sensor output voltage into the digital value.

2.2.26 Analog comparator (COMP)

The device embeds two comparators that can work either standalone (all terminals are available on I/Os) or together with the timers. COMP can be used as follows:

- Trigger low-power mode wake-up event by the analog signal
- Adjust the analog signal
- Combine the PWM output from the timer, and form a cyclic current control circuit
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Reusable I/O pin
  - Internal comparison voltage CRV can be division voltage value of VDDA or internal reference voltage
- Programmable hysteresis voltage
- Programmable speed and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminal, which can trigger the following events:
  - Capture event
  - OCref_clr event (cyclic current control)
- Break event of rapidly turning off PWM

2.2.27 Serial debug interface (SWD)

The device embeds an Arm standard two-wire serial debug interface (SW-DP).

3 Pinout and assignment

3.1 Pinout diagram

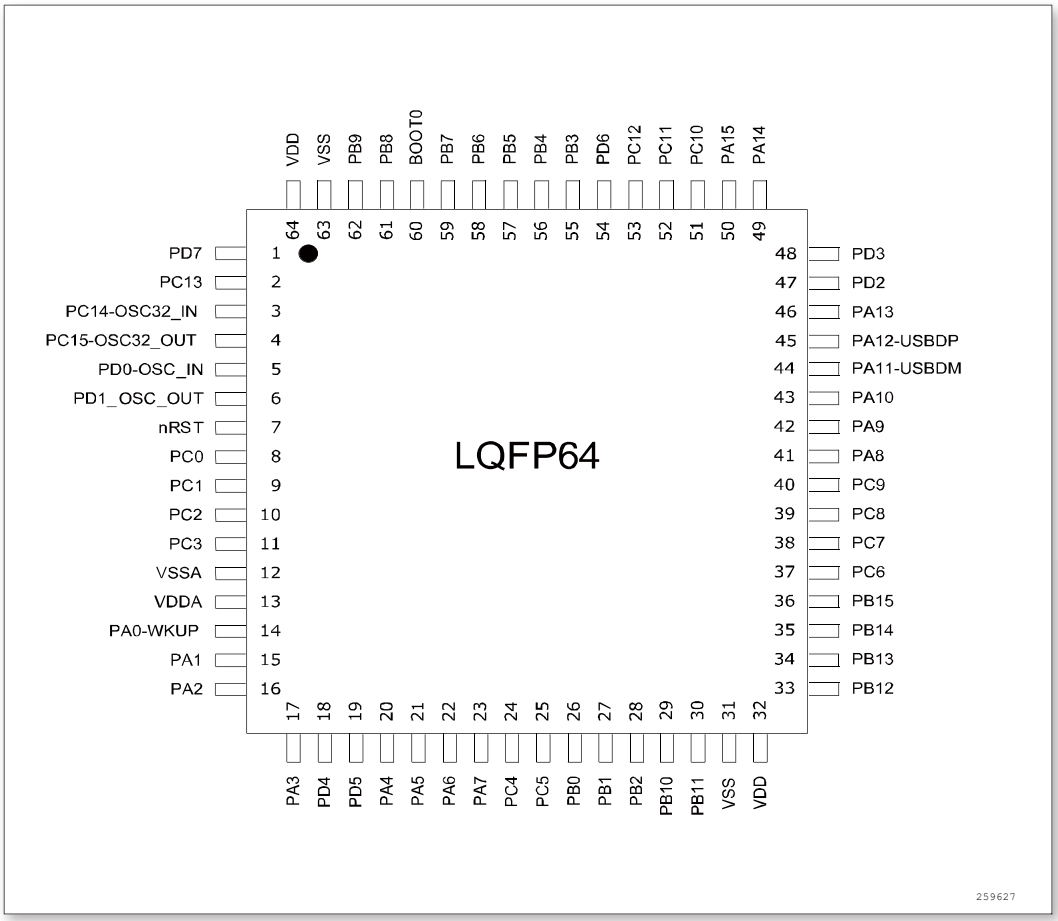

Figure 3-1 LQFP64 pinout diagram

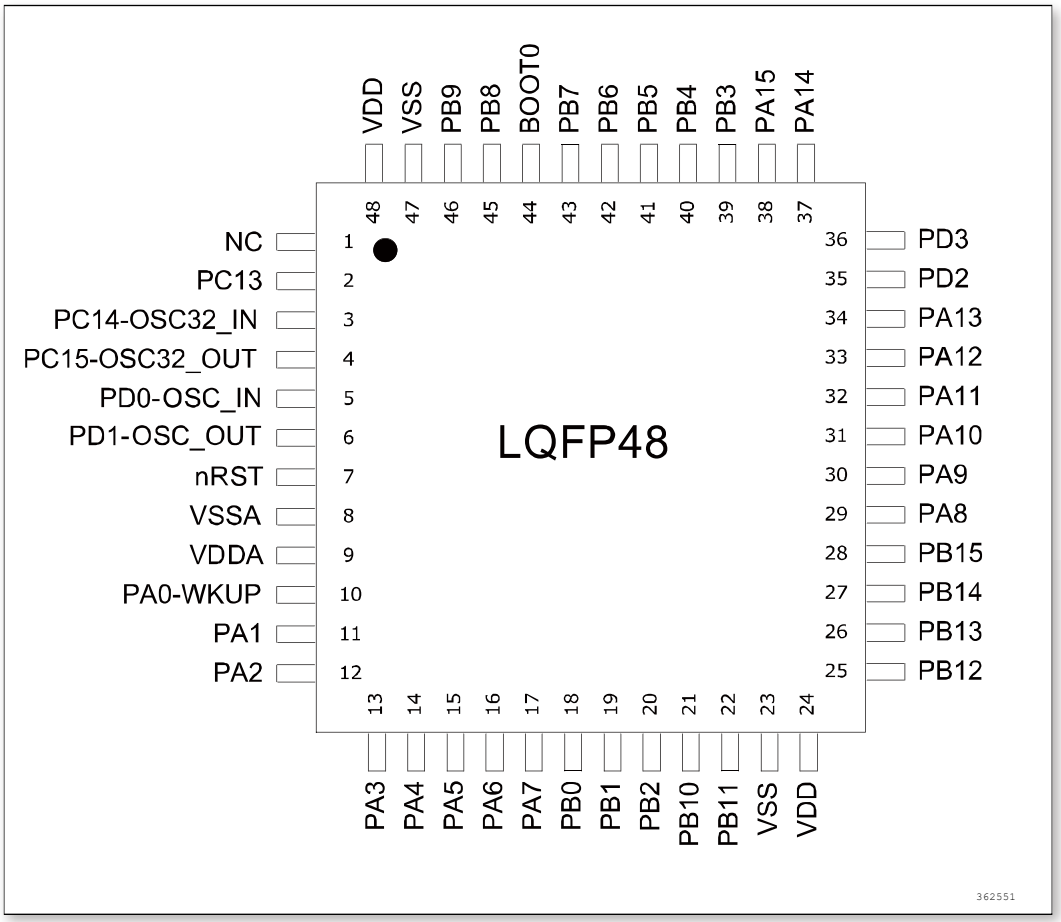

Figure 3-2 LQFP48 pinout diagram

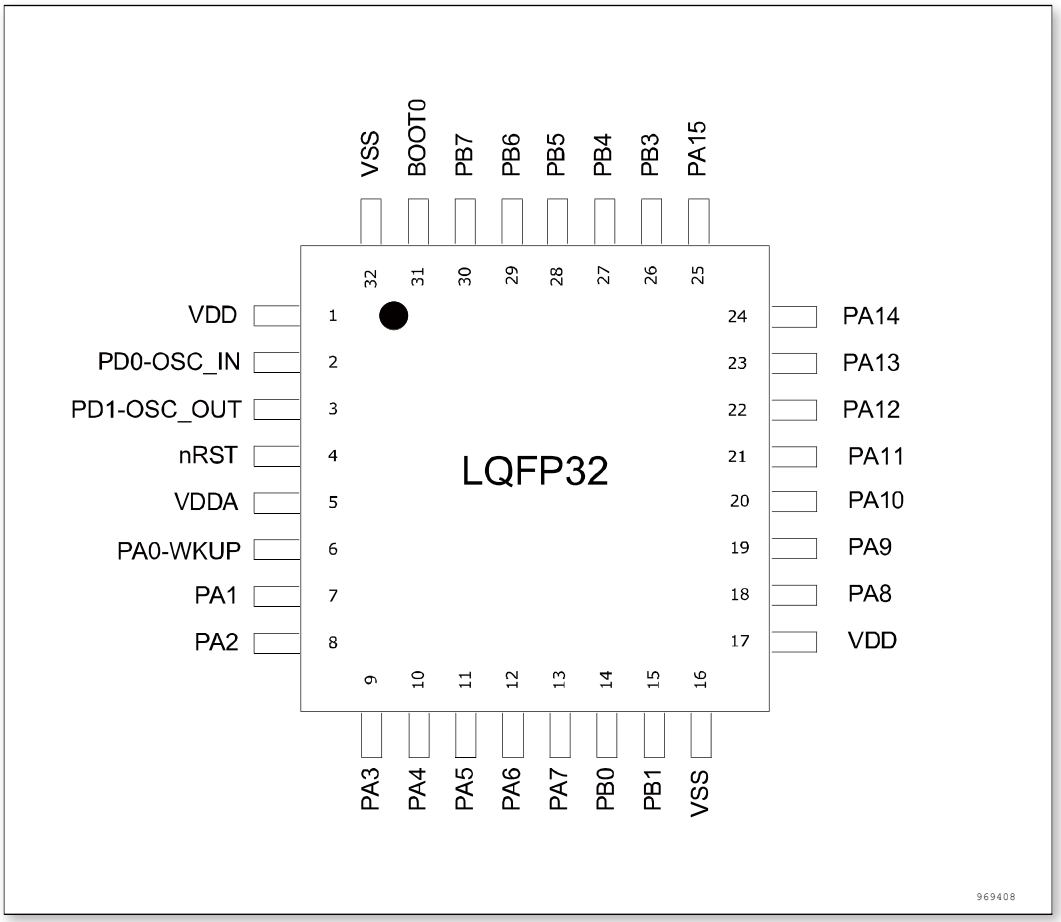

Figure 3-3 LQFP32 pinout diagram

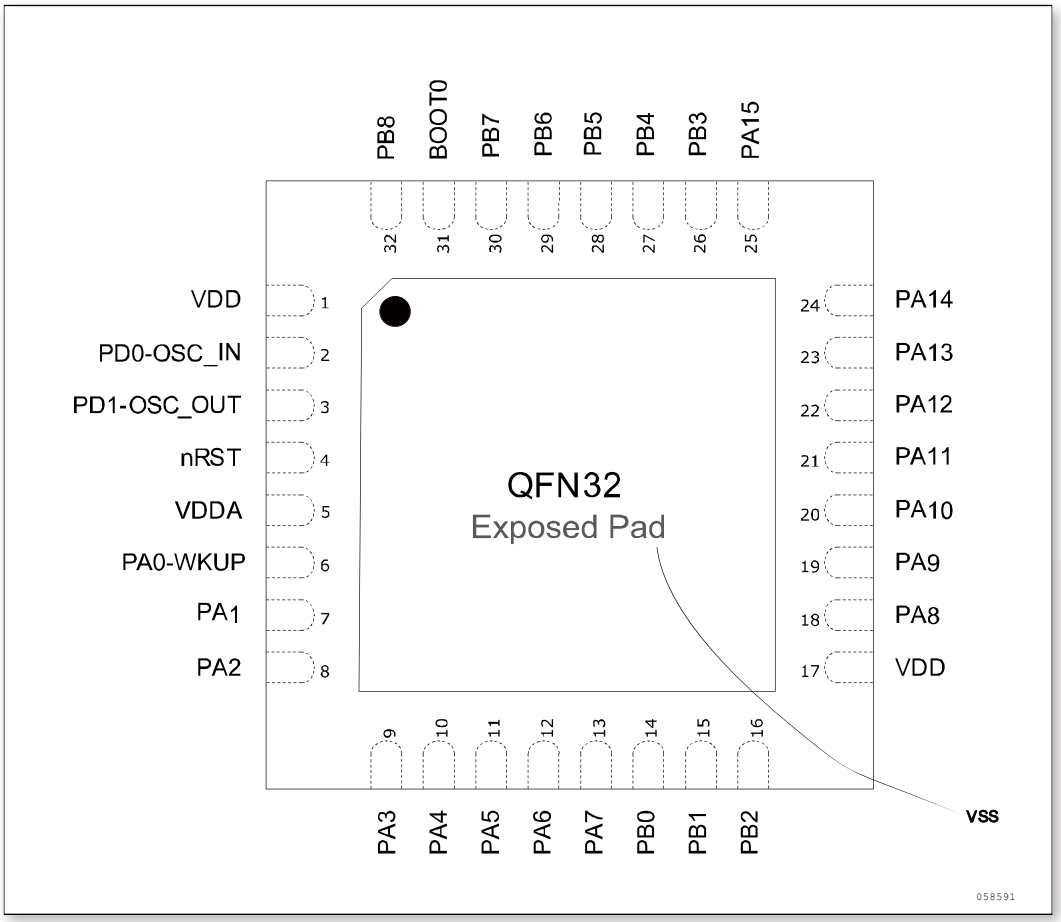

Figure 3-4 QFN32 pinout diagram

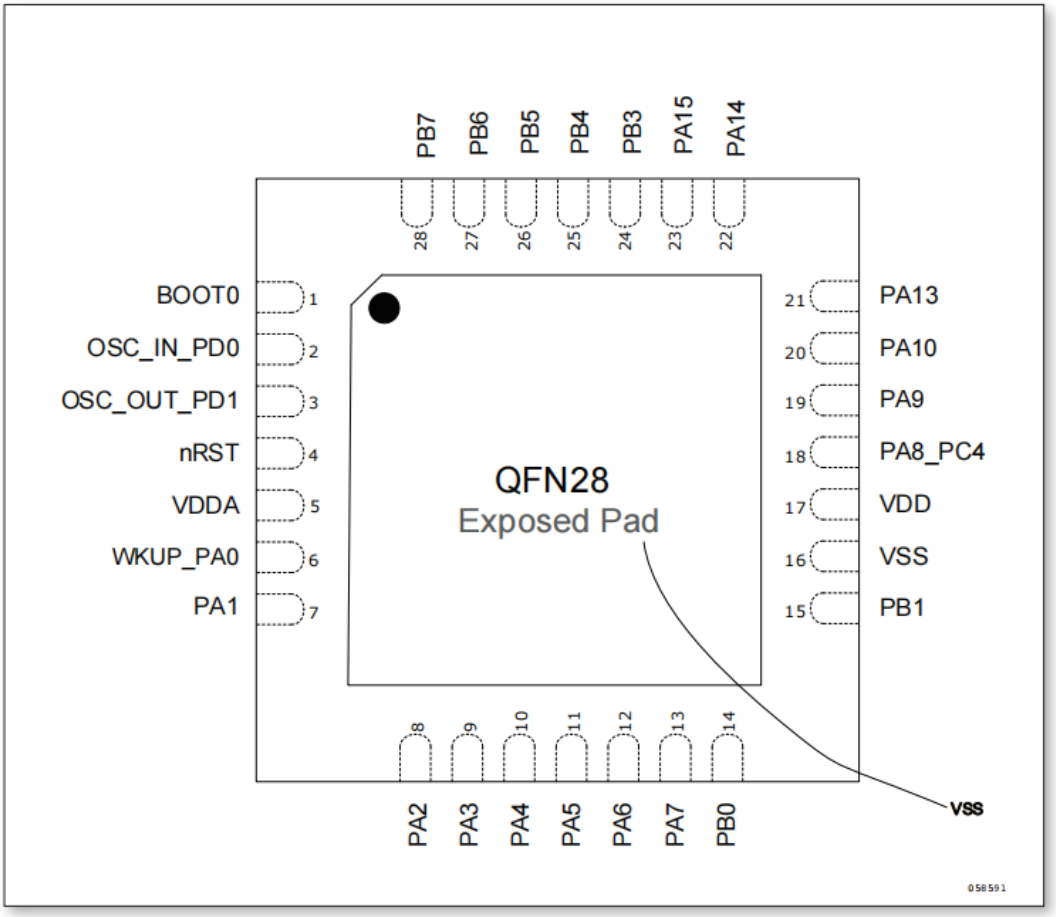

Figure 3-5 QFN28 pinout diagram

3.2 Pin assignment

Table 3-1 Pin assignment table

Pin ID					Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
LQFP64	LQFP48	LQFP32	QFN32	QFN28						
1	-	-	-	-	PD7	I/O	TC	PD7	TIM3_CH1 TIM17_CH1	-
2	2	-	-	-	PC13	I/O	TC	PC13	TIM2_CH1 TIM2_ETR	-
3	3	-	-	-	PC14 OSC32_IN	I/O	TC	PC14	TIM2_CH2	-
4	4	-	-	-	PC15 OSC32_OUT	I/O	TC	PC15	TIM2_CH3	-
5	5	2	2	2	PD0 OSC_IN	I/O	TC	PD0	I2C1_SDA TIM1_CH1N UART1_TX TIM1_CH2 SPI1_MOSI	-
6	6	3	3	3	PD1 OSC_OUT	I/O	TC	PD1	TIM1_BKIN I2C1_SCL TIM1_CH1 UART1_RX TIM1_CH2 SPI1_MISO SPI1_SCK	-
7	7	4	4	4	nRST	I/O	TC	nRST	-	-
8	-	-	-	-	PC0	I/O	TC	PC0	-	-
9	-	-	-	-	PC1	I/O	TC	PC1	-	-
10	-	-	-	-	PC2	I/O	TC	PC2	SPI2_MISO	-
11	-	-	-	-	PC3	I/O	TC	PC3	SPI2_MOSI	-
12	8	-	0	0	VSSA	S	-	VSSA	-	-
13	9	5	5	5	VDDA	S	-	VDDA	-	-
14	10	6	6	6	PA0 WKUP	I/O	TC	PA0	UART2_CTS TIM2_CH1 TIM2_ETR UART1_RX TIM14_CH1 COMP1_OUT	ADC1_VIN[0] COMP1_INP[0] COMP2_INP[0] COMP1_INM[2]
15	11	7	7	7	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2 TIM1_CH2 UART1_TX	ADC1_VIN[1] COMP1_INP[1] COMP2_INP[1]
16	12	8	8	8	PA2	I/O	TC	PA2	UART2_TX TIM2_CH3 TIM1_CH2N COMP2_OUT	ADC1_VIN[2] COMP1_INP[2] COMP2_INP[2] COMP2_INM[2]
17	13	9	9	9	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4 TIM1_CH3	ADC1_VIN[3] COMP1_INP[3] COMP2_INP[3]
18	-	-	-	-	PD4	I/O	TC	PD4	SPI1_MISO SPI1_MOSI	-
19	-	-	-	-	PD5	I/O	TC	PD5	SPI1_MOSI SPI1_MISO	-
20	14	10	10	10	PA4	I/O	TC	PA4	SPI1_NSS SPI1_SCK TIM1_CH3N TIM14_CH1 TIM1_BKIN	ADC1_VIN[4] COMP1_INM[0] COMP2_INM[0]

Pin ID					Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
LQFP64	LQFP48	LQFP32	QFN32	QFN28						
21	15	11	11	11	PA5	I/O	TC	PA5	SPI1_SCK SPI1_NSS TIM2_CH1 TIM2_ETR TIM1_CH3N	ADC1_VIN[5] COMP1_INM[1] COMP2_INM[1]
22	16	12	12	12	PA6	I/O	TC	PA6	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 TIM1_CH3 COMP1_OUT	ADC1_VIN[6]
23	17	13	13	13	PA7	I/O	TC	PA7	SPI1_MOSI TIM3_CH2 TIM1_CH1N TIM1_CH3N TIM14_CH1 TIM17_CH1 TIM1_CH2N COMP2_OUT	ADC1_VIN[7]
24	-	-	-	18	PC4	I/O	TC	PC4	UART2_TX TIM3_CH1 SPI1_MOSI	-
25	-	-	-	-	PC5	I/O	TC	PC5	UART2_RX TIM3_CH2 SPI1_MISO	-
26	18	14	14	14	PB0	I/O	TC	PB0	TIM3_CH3 TIM1_CH2N TIM1_CH1N TIM1_CH3	ADC1_VIN[8]
27	19	15	15	15	PB1	I/O	TC	PB1	TIM14_CH1 TIM3_CH4 TIM1_CH3N TIM1_CH2N TIM2_CH3 TIM1_CH2 TIM1_CH1N	ADC1_VIN[9]
28	20	-	16	-	PB2	I/O	TC	PB2	-	-
29	21	-	-	-	PB10	I/O	TC	PB10	I2C1_SCL TIM2_CH3 SPI2_SCK	-
30	22	-	-	-	PB11	I/O	TC	PB11	I2C1_SDA TIM2_CH4	-
31	23	16	0	16	VSS	S	-	VSS	-	-
32	24	17	17	17	VDD	S	-	VDD	-	-
33	25	-	-	-	PB12	I/O	TC	PB12	SPI2_NSS SPI2_SCK TIM1_BKIN SPI2_MOSI SPI2_MISO	-
34	26	-	-	-	PB13	I/O	TC	PB13	SPI2_SCK SPI2_MISO TIM1_CH1N SPI2_NSS SPI2_MOSI I2C1_SCL TIM17_CH1 TIM1_CH3N	-
35	27	-	-	-	PB14	I/O	TC	PB14	SPI2_MISO SPI2_MOSI TIM1_CH2N SPI2_SCK	-

Pin ID					Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
LQFP64	LQFP48	LQFP32	QFN32	QFN28						
									SPI2_NSS I2C1_SDA TIM1_CH3 TIM1_CH1	
36	28	-	-	-	PB15	I/O	TC	PB15	SPI2_MOSI SPI2_NSS TIM1_CH3N SPI2_MISO SPI2_SCK TIM1_CH2N TIM1_CH2	-
37	-	-	-	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM3_CH3 SPI1_NSS	-
38	-	-	-	-	PC7	I/O	TC	PC7	TIM3_CH2 TIM2_CH1 TIM2_ETR SPI1_SCK	-
39	-	-	-	-	PC8	I/O	TC	PC8	TIM3_CH3 TIM2_CH2	-
40	-	-	-	-	PC9	I/O	TC	PC9	TIM3_CH4 TIM2_CH3	-
41	29	18	18	18	PA8	I/O	TC	PA8	MCO TIM1_CH1 TIM1_CH2 TIM1_CH3	-
42	30	19	19	19	PA9	I/O	TC	PA9	UART1_TX TIM1_CH2 UART1_RX I2C1_SCL MCO TIM1_CH1N	-
43	31	20	20	20	PA10	I/O	TC	PA10	TIM17_BKIN UART1_RX TIM1_CH3 UART1_TX I2C1_SDA TIM1_CH1 TIM16_CH1	-
44	32	21	21	-	PA11	I/O	TC	PA11	UART1_CTS TIM1_CH4 TIM1_CH3 CAN1_RX I2C1_SCL TIM1_BKIN COMP1_OUT	USB_DM
45	33	22	22	-	PA12	I/O	TC	PA12	UART1_RTS TIM1_ETR TIM1_CH3N CAN1_TX I2C1_SDA TIM1_CH2 COMP2_OUT	USB_DP
46	34	23	23	21	PA13	I/O	TC	PA13	SWDIO UART1_TX	-
47	35	-	-	-	PD2	I/O	TC	PD2	I2C1_SCL SPI1_NSS	-
48	36	-	-	-	PD3	I/O	TC	PD3	I2C1_SDA SPI1_SCK SPI1_MISO	-
49	37	24	24	22	PA14	I/O	TC	PA14	SWDCLK UART2_TX UART1_RX	-

Pin ID					Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
LQFP64	LQFP48	LQFP32	QFN32	QFN28						
50	38	25	25	23	PA15	I/O	TC	PA15	SPI1_NSS UART2_RX TIM2_CH1 TIM2_ETR SPI2_SCK SPI2_MOSI SPI2_MISO TIM1_CH1N TIM1_CH3N	-
51	-	-	-	-	PC10	I/O	TC	PC10	UART1_TX SPI2_MISO SPI2_SCK SPI2_NSS SPI2_MOSI COMP2_OUT	-
52	-	-	-	-	PC11	I/O	TC	PC11	UART1_RX SPI2_MOSI SPI2_NSS SPI2_SCK SPI2_MISO	-
53	-	-	-	-	PC12	I/O	TC	PC12	UART1_TX SPI2_SCK SPI2_MISO SPI2_MOSI SPI2_NSS	-
54	-	-	-	-	PD6	I/O	TC	PD6	TIM3_ETR TIM1_CH3N TIM1_CH1 TIM1_CH1N	-
55	39	26	26	24	PB3	I/O	TC	PB3	SPI1_SCK TIM2_CH2 TIM1_CH1 TIM1_CH2N TIM1_CH3	-
56	40	27	27	25	PB4	I/O	TC	PB4	SPI1_MISO TIM3_CH1 TIM1_CH2 TIM17_BKIN TIM1_CH3N TIM1_CH2N	-
57	41	28	28	26	PB5	I/O	TC	PB5	SPI1_MOSI TIM3_CH2 TIM16_BKIN TIM1_CH1 TIM1_CH2	-
58	42	29	29	27	PB6	I/O	TC	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM1_CH2N TIM1_CH2 TIM1_CH1N	-
59	43	30	30	28	PB7	I/O	TC	PB7	UART1_RX I2C1_SDA TIM17_CH1N TIM1_CH3 TIM1_CH1	-
60	44	31	31	1	BOOT0	I	-	BOOT0	-	-
61	45	-	32	-	PB8	I/O	TC	PB8	UART1_RX I2C1_SCL TIM16_CH1 TIM1_CH1	-

Pin ID					Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
LQFP64	LQFP48	LQFP32	QFN32	QFN28						
									CAN1_RX TIM3_CH2	
62	46	-	-	-	PB9	I/O	TC	PB9	UART1_TX I2C1_SDA TIM17_CH1 CAN1_TX SPI2_NSS TIM3_CH3	-
63	47	32	0	0	VSS	S	-	VSS	-	-
64	48	1	1	-	VDD	S	-	VDD	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state
2. TC: standard IO, input signal level should not exceed V_{DD}

3.3 Pin multiplexing

Table 3-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1 TIM2_ETR	-	UART1_RX	-	TIM14_CH1	COMP1_OU
PA1	-	UART2_RTS	TIM2_CH2	TIM1_CH2	UART1_TX	-	-	-
PA2	-	UART2_TX	TIM2_CH3	TIM1_CH2N	-	-	-	COMP2_OU
PA3	-	UART2_RX	TIM2_CH4	TIM1_CH3	-	-	-	-
PA4	SPI1_NSS	SPI1_SCK	-	TIM1_CH3N	TIM14_CH1	TIM1_BKIN	-	-
PA5	SPI1_SCK	SPI1_NSS	TIM2_CH1 TIM2_ETR	-	-	-	TIM1_CH3N	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	TIM1_CH3	COMP1_OU
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	TIM1_CH3N	TIM14_CH1	TIM17_CH1	TIM1_CH2N	COMP2_OU
PA8	MCO	-	TIM1_CH1	-	-	-	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	TIM1_CH1	TIM16_CH1	-
PA11	-	UART1_CTS	TIM1_CH4	TIM1_CH3	CAN1_RX	I2C1_SCL	TIM1_BKIN	COMP1_OU
PA12	-	UART1_RTS	TIM1_ETR	TIM1_CH3N	CAN1_TX	I2C1_SDA	TIM1_CH2	COMP2_OU
PA13	SWDIO	-	-	UART1_TX	-	-	-	-
PA14	SWDCLK	UART2_TX	-	UART1_RX	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1 TIM2_ETR	SPI2_SCK	SPI2_MOSI	SPI2_MISO	TIM1_CH1N	TIM1_CH3N

Table 3-3 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH2N	TIM2_CH3	TIM1_CH2	TIM1_CH1N	-
PB3	SPI1_SCK	-	TIM2_CH2	-	TIM1_CH1	-	TIM1_CH2N	TIM1_CH3
PB4	SPI1_MISO	TIM3_CH1	-	-	TIM1_CH2	TIM17_BKIN	TIM1_CH3N	TIM1_CH2N
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	TIM1_CH1	TIM1_CH2
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM1_CH2N	-	TIM1_CH2	TIM1_CH1N
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM1_CH3	TIM1_CH1
PB8	UART1_RX	I2C1_SCL	TIM16_CH1	TIM1_CH1	CAN1_RX	-	TIM3_CH2	-
PB9	UART1_TX	I2C1_SDA	TIM17_CH1	-	CAN1_TX	SPI2_NSS	TIM3_CH3	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM17_CH1	TIM1_CH3N
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	TIM1_CH3	TIM1_CH1
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	-	TIM1_CH2N	TIM1_CH2

Table 3-4 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC2	-	SPI2_MISO	-	-	-	-	-	-
PC3	-	SPI2_MOSI	-	-	-	-	-	-
PC4	-	-	-	UART2_TX	-	TIM3_CH1	SPI1_MOSI	-
PC5	-	-	-	UART2_RX	-	TIM3_CH2	SPI1_MISO	-
PC6	-	TIM3_CH1	-	-	-	TIM3_CH3	SPI1_NSS	-
PC7	-	TIM3_CH2	-	-	-	TIM2_CH1 TIM2_ETR	SPI1_SCK	-
PC8	-	TIM3_CH3	-	-	-	TIM2_CH2	-	-
PC9	-	TIM3_CH4	-	-	-	TIM2_CH3	-	-
PC10	UART1_TX	-	-	SPI2_MISO	SPI2_SCK	SPI2_NSS	SPI2_MOSI	COMP2_OU
PC11	UART1_RX	-	-	SPI2_MOSI	SPI2_NSS	SPI2_SCK	SPI2_MISO	-
PC12	UART1_TX	-	-	SPI2_SCK	SPI2_MISO	SPI2_MOSI	SPI2_NSS	-
PC13	-	-	-	-	-	-	TIM2_CH1 TIM2_ETR	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 3-5 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	TIM1_CH1N	UART1_TX	TIM1_CH2	SPI1_MOSI	SPI1_MOSI	-
PD1	TIM1_BKIN	I2C1_SCL	TIM1_CH1	UART1_RX	TIM1_CH2	SPI1_MISO	SPI1_SCK	-
PD2	-	I2C1_SCL	-	-	-	SPI1_NSS	SPI1_NSS	-
PD3	-	I2C1_SDA	-	-	-	SPI1_SCK	SPI1_MISO	-
PD4	SPI1_MISO	SPI1_MOSI	-	-	-	-	-	-
PD5	SPI1_MOSI	SPI1_MISO	-	-	-	-	-	-
PD6	-	TIM3_ETR	-	TIM1_CH3N	-	TIM1_CH1	TIM1_CH1N	-
PD7	-	-	-	-	-	TIM3_CH1	TIM17_CH1	-

4 Electrical characteristics

4.1 Test condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Typical Value

Unless otherwise specified, typical data are based on T_A = 25℃ and V_{DD} = 3.3V. These data are only used for design guidance and have not been tested.

4.1.2 Typical Curve

Unless otherwise specified, the typical curve is only used for design guidance and has not been tested.

4.1.3 Load Capacitance

The load condition during the measurement of pin parameters is shown in the figure below.

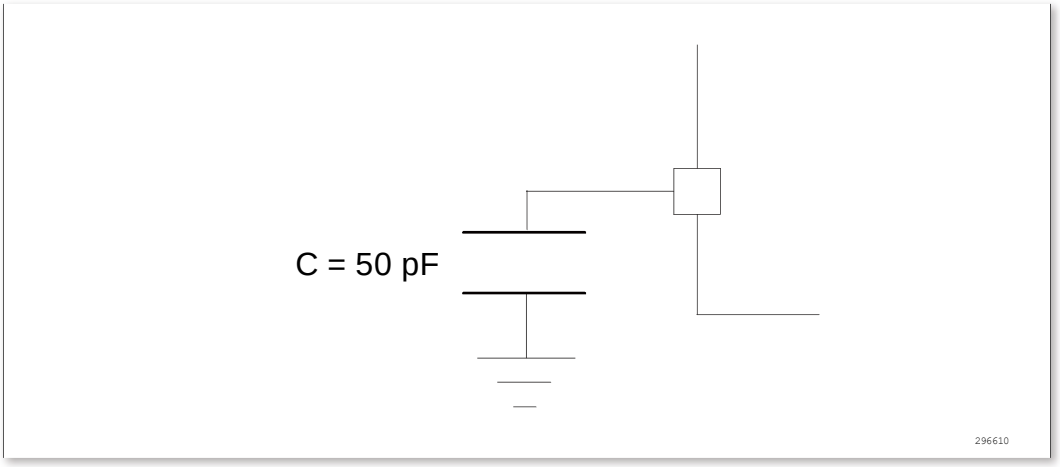

Figure 4-1 Pin loading conditions

4.1.4 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

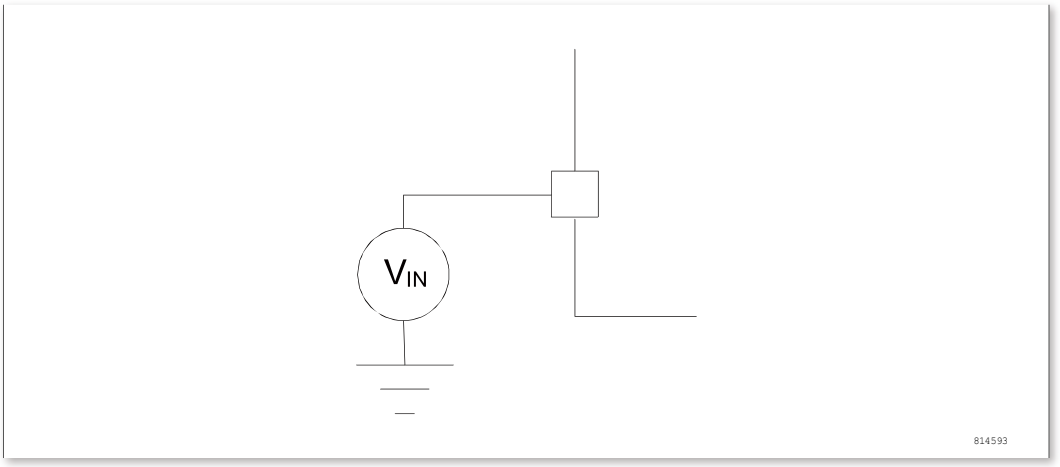

Figure 4-2 Pin input voltage

4.1.5 Power supply scheme

The power supply scheme is shown in the figure below.

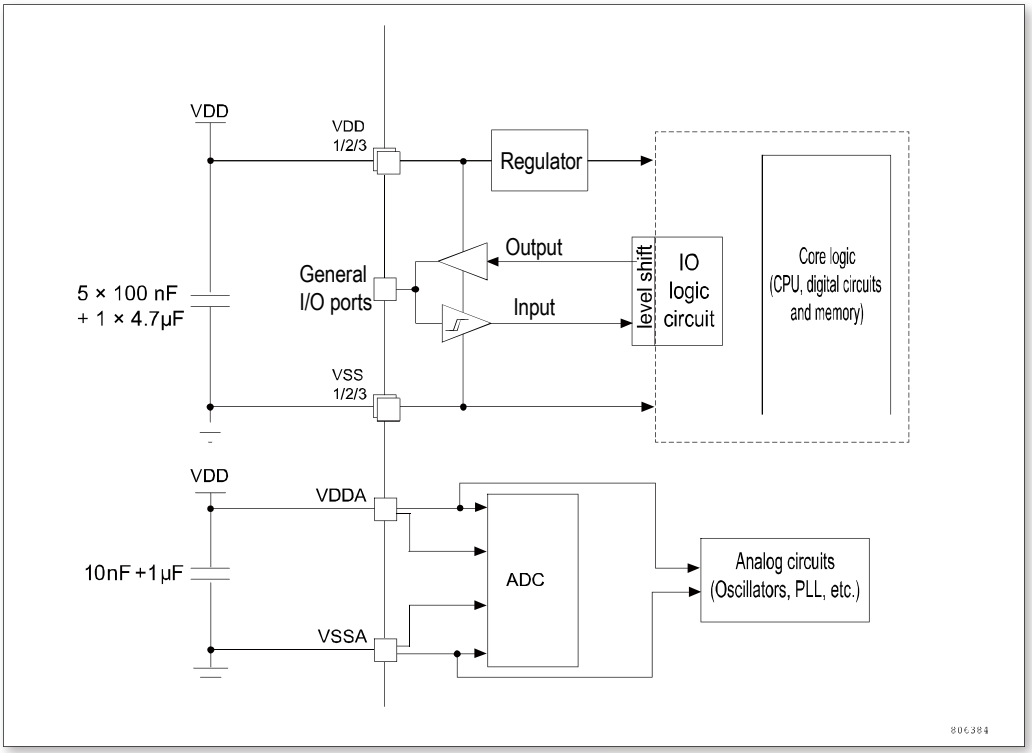

Figure 4-3 Power scheme

4.1.6 Current consumption measurement

The current consumption measurement on a pin is shown in the figure below

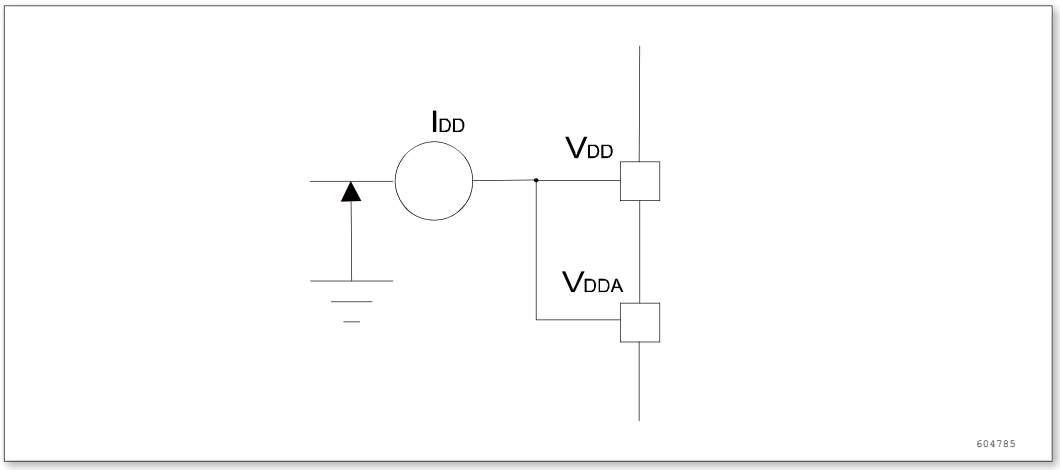

Figure 4-4 Current consumption measurement scheme

4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in (Table 4-1 and Table 4-2) may cause permanent damage to the device. These are stress maximum ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Description	Min.	Max.	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	-0.3	5.8	V
V_{IN}	Input voltage on other pins (2)	V_{SS}-0.3	V_{DD}+0.3	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to the table below for the maximum allowed injected current values.

Table 4-2 Current characteristics

Symbol	Description	Max.	Unit
I_{VDD}	Total current into sum of all V_{DD}/V_{DDA} power lines (source)(1)	120	mA
I_{VSS}	Total current out of sum V_{SS}/V_{SSA} ground lines (sink)(1)	-120	
I_{IO}	Output current sunk by any I/O and control pins	25	
	Output current sunk by any I/O and control pins	-25	
$I_{INJ\ (PIN)}$(2)(3)	Injected current on NRST pin	±5	
	Injected current on OSC_IN pin of HSE	±5	
$\sum I_{INJ\ (PIN)}$(4)	Total injected current on other pins(4)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/pulled between two consecutive power supply pins

referring to high pin count LQFP packages.

3. The negative injected current will interfere with the analog performance of the device.

4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency		0	72MHz	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Digital operating voltage		2.0	5.5	V
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD}(1)	2.5	5.5	V
	Analog circuit operating voltage (Performance is not guaranteed)		2.0	2.5	
P_D	Temperature: T_A = 85℃(2)				mW
T_A	Ambient temperature	Maximum power dissipation	-40	85	℃
		Low power dissipation (2)	-40	105	
T_J	Junction temperature		-40	105	℃

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.

2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.

4.3.2 Operating conditions at power-up/power-down

The parameters given in table below are derived from tests performed under the general operating conditions.

Table 4-4 Operating conditions at power-up/power-down (1)

Symbol	Condition	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise speed	T_A = 25℃	1	∞	μs/V
	V_{DD} rise speed		500	∞	

1. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

4.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions listed in Table 4-3.

Table 4-5 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Embedded reset and power control block characteristics	PLS[3:0]=0000 (rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (falling edge)	-	1.7	-	
		PLS[3:0]=0001 (rising edge)	-	2.1	-	
		PLS[3:0]=0001 (falling edge)	-	2.0	-	
		PLS[3:0]=0010 (rising edge)	-	2.4	-	
		PLS[3:0]=0010 (falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	
		PLS[3:0]=0100 (falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)	-	3.3	-	
		PLS[3:0]=0101 (falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	
		PLS[3:0]=0111 (falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	
		PLS[3:0]=1000 (falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	
		PLS[3:0]=1001 (falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (falling edge)	-	4.7	-	
$V_{POR/PDR}$	Power on reset threshold	Flip point	-	1.65	-	V
$T_{RSTTEMPO}$	Reset duration	-	-	2.7	-	ms

1. Guaranteed by design, not tested in production.

Note: Reset duration is measured from the power-on moment to the moment the first instruction is read by the user's application code.

4.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed code.

The current consumption readings in all running modes given in this section are under the execution of a set of simple codes.

Maximum Current Consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state at 0~24 MHz; 1 wait state at 24~48 MHz; 2 wait states at 48 ~ 72 MHz).
- The instruction prefetch function is enabled. When the peripherals are enabled: $f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 4-6 Typical and maximum current consumption in Stop and Standby mode (1)(2)

Symbol	Parameter	Conditions	Typical			Maximum	Unit
			-40℃	25℃	85℃	25℃	
I_{DD}	Supply current in stop mode	PWR->CR[0] is set as 1	1.5	5.2	55.9	9	μA
	Supply current in standby mode	LSI and IWDG are on	1.3	1.6	6.0	-	
		IWDG is off	0.5	0.5	5.1	1	

1. Drawn from comprehensive evaluation, not tested in production. The IO status is analog input.
2. The maximum value is tested in case of the power supply voltage = 3.3V.

Typical Current Consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state at 0~24 MHz; 1 wait state at 24~48 MHz; 2 wait states at 48 ~ 72 MHz).
- The instruction prefetch function is enabled. When the peripherals are enabled: $f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 4-7 Maximum Current Consumption in Operating Mode, with Data Processing Code Running from Internal Flash Memory (1)(2)(3)(4)(5)

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled			Typical value All peripherals disabled			Unit
				-40℃	25℃	85℃	-40℃	25℃	85℃	
I_{DD}	Supply current in Run mode	Internal clock	72MHz	21.70	22.10	22.40	10.40	10.20	10.40	mA
			48MHz	15.70	16.00	16.30	8.37	8.07	8.24	
			24MHz	9.50	9.70	9.91	5.29	4.95	5.09	

Symbol	Parameter	Condition	f_{HCLK}(Hz)	Typical value All peripherals enabled			Typical value All peripherals disabled			Unit
				-40℃	25℃	85℃	-40℃	25℃	85℃	
			8MHz	5.19	5.30	5.42	3.10	2.67	2.75	
			4MHz	4.13	4.22	4.32	2.58	2.13	2.21	
			2MHz	3.62	3.69	3.78	2.32	1.86	1.93	
			1MHz	3.36	3.43	3.51	2.21	1.73	1.79	
			500K	3.23	3.29	3.38	2.14	1.67	1.73	
			125K	3.13	3.20	3.28	2.09	1.62	1.68	

1. All I/O pins are in input mode; V_{DD} or V_{SS} is a static value (no load).
2. All peripherals are disabled, unless otherwise specified.
3. The flash access time conforms to the configuration in the user manual.
4. The values are measured when the supply voltage is 3.3V.
5. It's obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division.

Table 4-8 Maximum Current Consumption in Sleep Mode, with Data Processing Code Running from Internal Flash Memory (1)(2)(3)(4)(5)

Symbol	Parameter	Condition	f_{HCLK}	Typical value All peripherals enabled			Typical value All peripherals disabled			Unit
				-40℃	25℃	85℃	-40℃	25℃	85℃	
I_{DD}	Supply current in sleep mode	Internal clock	72MHz	17.50	17.90	18.20	6.29	5.96	6.07	mA
			48MHz	12.10	12.30	12.50	4.72	4.33	4.42	
			24MHz	7.64	7.79	7.94	3.46	3.04	3.11	
			8MHz	4.58	4.66	4.77	2.48	2.03	2.09	
			4MHz	3.83	3.90	4.00	2.28	1.82	1.87	
			2MHz	3.47	3.53	3.62	2.17	1.71	1.76	
			1MHz	3.28	3.35	3.43	2.11	1.65	1.71	
			500K	3.19	3.26	3.34	2.10	1.63	1.68	
			125K	3.13	3.19	3.27	2.08	1.61	1.66	

1. All I/O pins are in input mode; V_{DD} or V_{SS} is a static value (no load).
2. All peripherals are disabled, unless otherwise specified.
3. The flash access time conforms to the configuration in the user manual.
4. The values are measured when the supply voltage is 3.3V.
5. It's obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division.

Current Consumption of Built-in Peripherals

The built-in peripheral current consumption is presented in Table 4-9, The MCU is placed under the following working conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The given value is calculated by measuring current consumptions
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient temperature and VDD supply voltage conditions are listed in Table 4-3.

Table 4-9 Built-in peripheral current consumption (1)

Built-in Peripheral		Typical Power Consumption at 25℃	Unit	Built-in Peripheral		Typical Power Consumption at 25℃	Unit
AHB	GPIOD	0.12	mA	APB2	TIM14	0.35	mA
	GPIOC	0.13			TIM16	0.38	
	GPIOB	0.12			TIM17	0.43	
	GPIOA	0.15		APB1	WWDG	0.09	
	CRC	0.20			SPI2	1.03	
	DMA	0.36			UART2	0.77	
APB2	DBG	0.04			I2C1	1.19	
	ADC1	0.28			TIM2	0.97	
	TIM1	1.28			TIM3	0.70	
	SPI1	0.97			PWR	0.23	
	COMP	0.20			CRS	0.13	
	SYSCFG	0.09			CAN	1.64	
	UART1	0.78			USB	3.32	

1. f_{HCLK} = 72Mhz; HSI is used as PLL clock source.

4.3.5 External clock source characteristics

High-speed external user clock generated from an external oscillator source

The parameters of characteristics given in the following table are measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 4-10 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock frequency (1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w\ (HSE)}$	OSC_IN high or low time (1)	-	15	-	-	ns
$C_{in\ (HSE)}$	OSC_IN input capacitive reactance (1)	-	-	5	-	pF
DuCy (HSE)	Duty cycle	-	-	50	-	%

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from external oscillator source

The parameters of characteristics given in the following table are measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 4-11 Low-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User external clock frequency (1)	-	16	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w\ (LSE)}$	OSC_IN high or low time (1)	-	450	-	-	ns
$t_{r\ (LSE)}$	OSC_IN rise time (1)	-	-	-	50	ns
$t_{f\ (LSE)}$	OSC_IN fall time (1)	-	-	-	50	ns
$C_{in\ (LSE)}$	OSC_IN input capacitive reactance (1)	-	-	-	10	pF
$DuCy_{\ (LSE)}$	Duty cycle	-	-	50	-	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-1	-	1	μA

1. Guaranteed by design, not tested in production.

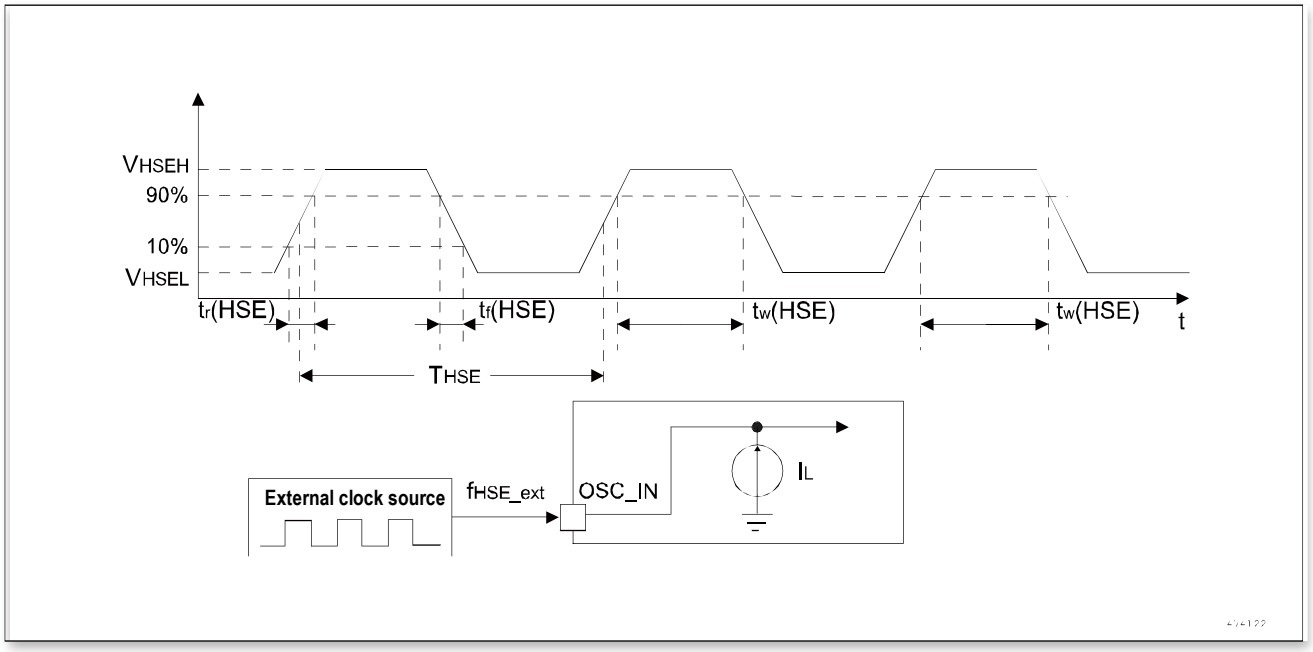

Figure 4-5 High-speed external user clock alternate current timing diagram

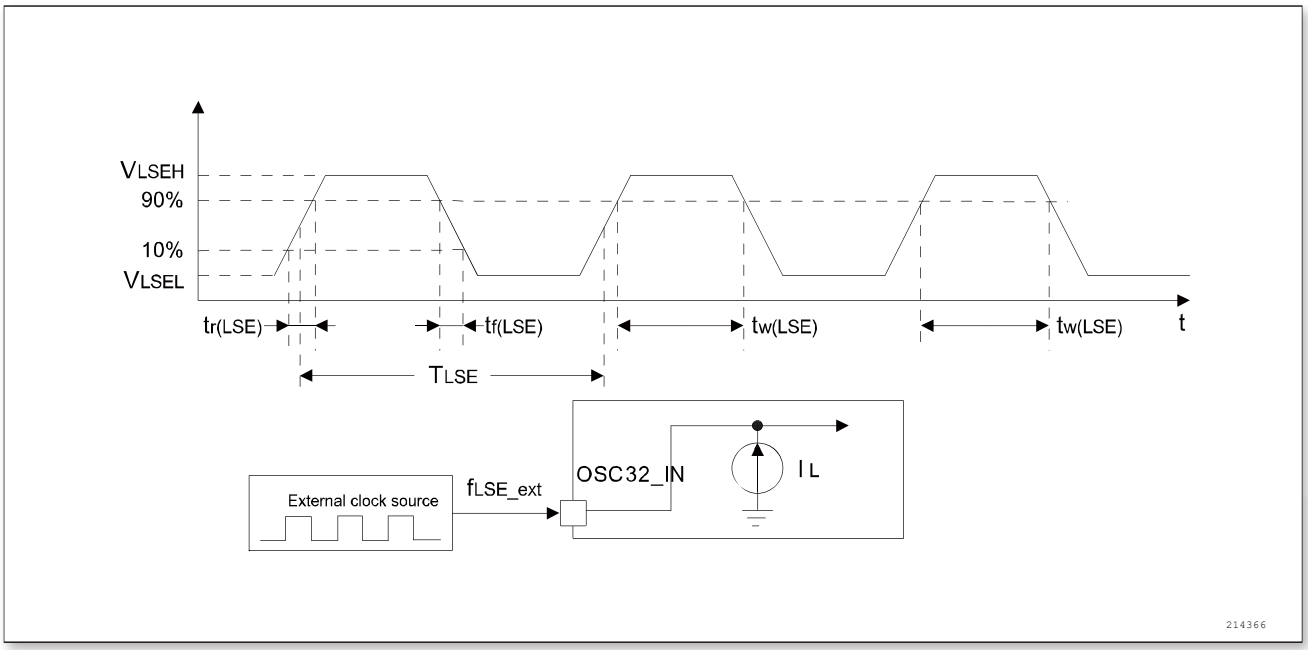

Figure 4-6 Low-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be generated by an oscillator composed of a 2 to 24MHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator parameters (frequency, package, accuracy, etc.).

Table 4-12 HSE 2 ~ 24MHz oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	2V<V_{DD}<3.6V	2	8	12	MHz
		3.0V<V_{DD}<5.5V	8	16	24	MHz
R_F	Feedback resistance (4)	-	-	510	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2}(3) is 16pF)	f_{OSC_IN} =24M V_{DD}=3V	-	-	60	Ω
		f_{OSC_IN} =12M V_{DD}=2V	-	-	150	Ω
I_2	HSE drive current	f_{OSC_IN} =24M ESR=30 V_{DD} = 3.3V, C_{L1} C_{L2}(3) is 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Startup	-	9	-	mA/V
$t_{SU\ (HSE)}$(5)	Startup time	V_{DD} is stable	-	3	-	mS

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Drawn from comprehensive evaluation.

3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typical value) designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10pF can be used as a rough estimate of the combined pin and board capacitance) when choosing choosing C_{L1} and C_{L2}.

4. The relatively low R_F resistance value can provide protection and avoid problems occurred when operating in a humid environment. Changes have been made to leakage and bias conditions generated in this environment. However, if the MCU is used in harsh humid conditions, such parameters need to be considered in designing.

5. $t_{SU(HSE)}$ is the startup time, measured from the moment it is enabled HSE by software to a stablized 8 MHz is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

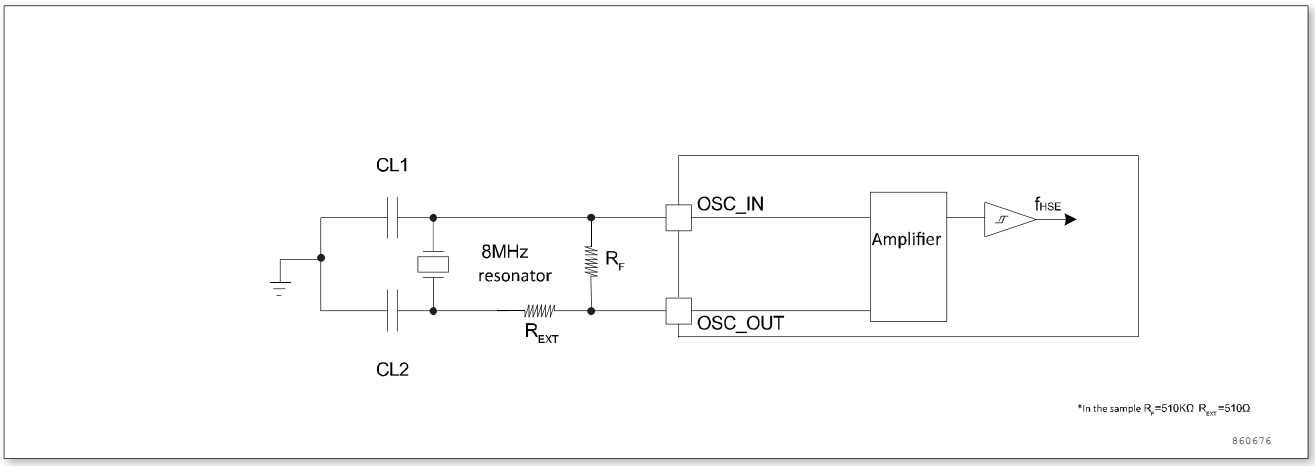

Figure 4-7 Typical application with an 8MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.). (note: the crystal oscillator is the passive crystal oscillator we usually refer to)

Note: For C_{L1} and C_{L2}, it is recommended to use a high quality 5pF ~ 15pF ceramic capacitor and a conformance crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically gives the load capacitance parameters

in serial combination of C_{L1} and C_{L2}. The load capacitor C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} pin capacitor and PCB board or PCB-related capacitor, and its typical value is in 2pF ~7pF. Warning: To avoid surpassing the maximum value (15pf) of C_{L1} and C_{L2}, it is highly recommended to use a resonator with load capacitor $C_L \leqslant$ 7PF. The resonator with load capacitor 12.5pF cannot be used. For example, if a resonator with load capacitor C_L = 6pF is selected and C_{stray} = 2pF, $C_{L1} = C_{L2}$= 8pF.

Table 4-13 LSE oscillator characteristics (f_{LSE}=32.768KHz)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
g_m	Oscillator transconductance	-	-	78	-	μA/V
$t_{SU\ (LSE)}$(2)	Startup time	R_S = 30kΩ	-	3	-	s

1. Drawn from comprehensive evaluation.
2. $t_{SU(LSE)}$ is the startup time, measured from the moment it is enabled LSE by software to a stablized 32.768KHz is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

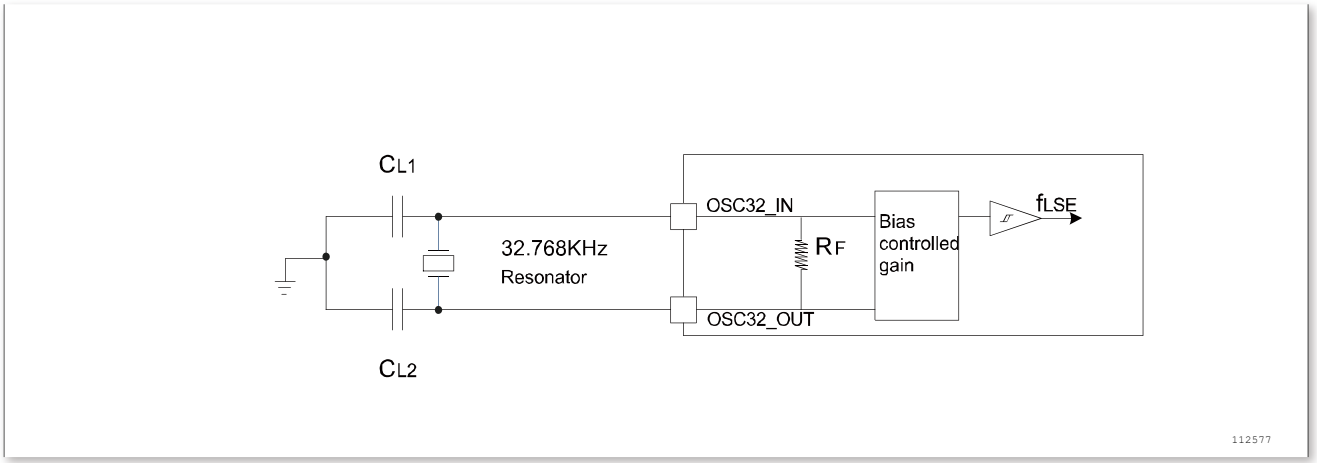

Figure 4-8 Typical application with a 32.768KHz crystal

4.3.6 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and supply voltage conforming to the general operating conditions.

High-speed internal (HSI) oscillator

Table 4-14 HSI oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
ACC_{HSI}	HSI oscillator accuracy	T_A = 25°C	-1	-	+1	%
		T_A = -40°C ~ 105°C	-3.5	-	+3.5	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{SU\ (HSI)}$	HSI oscillator startup time	-	-	12	16	μs
$I_{DD\ (HSI)}$	HSI oscillator power consumption	-	-	328	-	μA

1. V_{DD} = 3.3V, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 4-15 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}(2)	Frequency	-	-	40	-	KHz
$t_{SU\ (LSI)}$(3)	LSI oscillator startup time	-	-	-	85	μs
$I_{DD\ (LSI)}$(3)	LSI oscillator power consumption	-	-	1	1.4	μA

1. V_{DD} = 3.3V, T_A = -40℃~ 85℃, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

Wake-up time from low-power mode

The wake-up time listed in the following table is measured during the wake-up phase of the Internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times are measured when ambient temperature and supply voltage meet the general operating condition.

Table 4-16 Low-power mode wake-up timings

Symbol	Parameter	Condition	Max. Value	Unit
$t_{WUSLEEP}$(1)	Wake up from sleep mode	HSI is the system clock	2.7	μs
t_{WUSTOP}(1)	Wake up from Stop mode (voltage regulator in operation)	HSI is the system clock	5.5	μs
t_{WUSTOP}(1)	Wake up from Stop mode (voltage regulator in low power mode)	HSI is the system clock	7.7	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x00	498	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x01	430	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x02	390	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x03	318	μs

1. The wake-up time measurement starts from the wake-up event to the point at which the user application code reads the first instruction.

4.3.7 PLL Characteristics

The characteristic parameter listed in the following table is measured when ambient temperature and power supply voltage meet with the general operating condition.

Table 4-17 PLL characteristics (1)

Symbol	Parameter	Min Value	Typical Value	Max Value	Unit	Symbol
f_{PLL_IN}	PLL input clock (2)	-	4	-	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	-	40	-	200	MHz
t_{LOCK}	PLL lock time	-	-	-	100	μs

1. Guaranteed by design, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock frequency compatible with the range defined by f_{PLL_OUT}.

4.3.8 Memory Characteristics

Table 4-18 Flash characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	8-bit programming time	-	6	-	7.5	μs
t_{ERASE}	Page erasing time	-	4	-	5	ms
t_{ME}	Mass erasing time	-	20	-	40	ms
I_{DD}	Supply current	Reading mode	-	4	-	mA
		Writing mode	-	-	7	mA
		Erasing mode	-	-	2	mA
V_{prog}	Programming voltage	-	-	1.5	-	V

Table 4-19 Flash memory endurance and data retention period (1)(2)

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
N_{END}	Endurance		20	-	-	Thousand times
T_{RET}	Data retention period	T_A = 25℃	100	-	-	Year

1. Drawn from comprehensive evaluation, not tested in production.

4.3.9 EMC Characteristics

Susceptibility testing is carried out by sampling during product comprehensive evaluation.

Designing hardened software to avoid noise problems

EMC evaluation and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and qualification tests

in relation with the EMC.

Software recommendations

The software flowchart must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or the crystal oscillator pins for 1 second.

To complete these trials, a voltage can be applied directly on the chip, over the range of application requirements. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.3.10 Functional EMS (electrical sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive then a negative pulse separated by 1 second) are applied to the all pins of each sample. The sample size depends on the number of supply pins on the chip (3 parts X (n + 1) supply pins). This test conforms to the JEDEC JS-001-2017/002-2018 standard.

Static latchup

Two complementary static latchup tests are required on six samples to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin. These tests are compliant with the EIA/JESD78E IC latchup standard.

Table 4-20 EMS characteristics

Symbol	Parameter	Conditions	Max.	Unit
$V_{ESD\ (HBM)}$	Electrostatic discharge voltage (mannequin)	TA = 25℃, conforming to ESDA/JEDEC JS-001-2017	±6000	V
$V_{ESD\ (CDM)}$	Electrostatic discharge voltage (charging device model)	TA = 25℃, conforming to ESDA/JEDEC JS-002-2018	±1000	V
I_{LU}	Electrostatic latchup (Latchup current)	TA = 25℃, conforming to JESD78E	±100	mA

4.3.11 GPIO port general input/output characteristics

General Input/Output Characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests performed under the conditions summarized in Table 4-3. All I/O ports are CMOS-compliant.

Table 4-21 I/O static characteristics

Symbol	Parmeter	Conditions	Min	Typ.	Max.	Unit
VIL	Input low level voltage	2.5V< VDD < 5.5V			0.3*VDD	V
VIH	Input high level voltage	2.5V< VDD < 5.5V	0.7*VDD			V
Vhy	I/O pin Schmidt trigger voltage hysteresis (1)	2.5V< VDD < 5.5V		0.1*VDD		V
IIkg	Input leakage current (2)	2.5V< VDD < 5.5V	-1		1	uA
RPU	Weak pull-up equivalent resistance (3)	2.5V< VDD < 5.5V	10		50	kΩ
RPD	Weak pull-down equivalent resistance (3)	2.5V< VDD < 5.5V	10		100	kΩ
CIO	I/O pin capacitor	2.5V< VDD < 5.5V			10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. In case of a negative current back flow in the adjacent pin, the leakage current may be higher than the maximum value.
3. Pull-up and pull-down resistance is poly resistance.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA current.

In user application, the number of I/O pin must ensure that the drive current must be limited to respect the absolute maximum rating specified in Section 4.2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum running current of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents absorbed and sunk by all the I/O pins on V_{SS}, plus the maximum running current of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Table 4-22 Output voltage characteristics (1)

SPEED[1:0]	Symbol	Parmeter	Conditions	Min.	Typ.	Max.	Unit
11	VOL	Output low level	|IIO| = 6mA VDD=3.3V			0.60	V
	VOH	Output high level		2.80			V
	VOL	Output low level	|IIO| = 8mA VDD=3.3V			0.60	V
	VOH	Output high level		2.60			V
	VOL	Output low level	|IIO| = 20mA VDD=3.3V			1.20	V
	VOH	Output high level		1.60			V

SPEED[1:0]	Symbol	Parmeter	Conditions	Min.	Typ.	Max.	Unit
10	VOL	Output low level	|IIO| = 6mA VDD=3.3V			0.40	V
	VOH	Output high level		2.80			V
	VOL	Output low level	|IIO| = 8mA VDD=3.3V			0.40	V
	VOH	Output high level		2.80			V
	VOL	Output low level	|IIO| = 20mA VDD=3.3V			0.80	V
	VOH	Output high level		2.40			V
01	VOL	Output low level	|IIO| = 6mA VDD=3.3V			0.40	V
	VOH	Output high level		2.80			V
	VOL	Output low level	|IIO| = 8mA VDD=3.3V			0.40	V
	VOH	Output high level		2.80			V
	VOL	Output low level	|IIO| = 20mA VDD=3.3V			0.60	V
	VOH	Output high level		2.40			V

1. Drawn from comprehensive evaluation, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 4-9 and Table 4-23, respectively.

Unless otherwise specified, the parameter listed in Table 4-23 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 4-3.

Table 4-23 Input/output AC characteristics (1)(2)

SPEED[1:0]	Symbol	Parmeter	Conditions	min	typcal	max	unit
11	tf	Output high to low level fall time	CL = 50pF VDD = 3.3V		6.2		ns
	tr	Output low to high level rise time			7.8		ns
10	tf	Output high to low level fall time			4.2		ns
	tr	Output low to high level rise time			3.9		ns
01	tf	Output high to low level fall time			3.6		ns
	tr	Output low to high level rise time			3.7		ns

1. The I/O port speed is configured through MODEx[1:0]. Refer to the Reference manual for a description of the GPIO port configuration register.
2. Guaranteed by design, not tested in production.

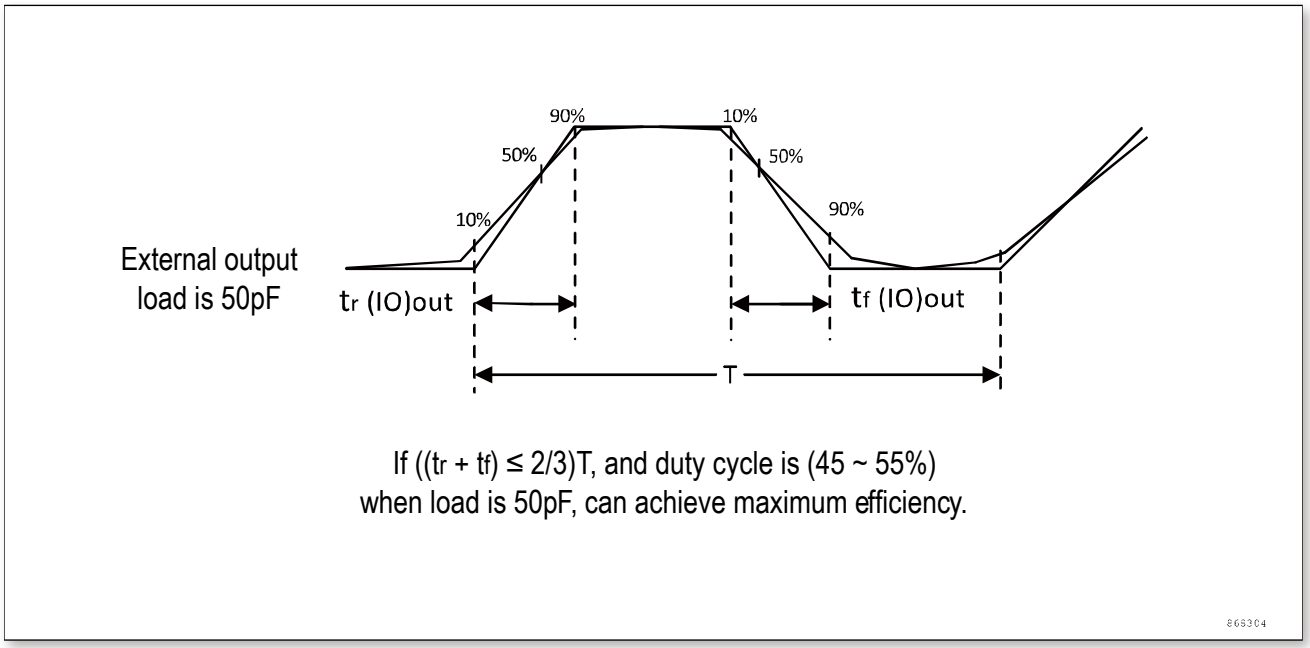

Figure 4-9 Input/output AC characteristics definition

4.3.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology, and it is connected to a permanent pull-up resistor, RPU. Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-24 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL\ (NRST)}$ (1)	NRST input low level voltage		-0.3	-	$0.3*V_{DD}$	V
$V_{IH\ (NRST)}$ (1)	NRST input high level voltage		$0.7*V_{DD}$	-	V_{DD}	V
$V_{hys\ (NRST)}$	NRST Schmitt trigger voltage hysteresis		-	$0.1*V_{DD}$	-	V
R_{PU}	Weak pull-up equivalent resistor (1) (2)	$V_{IN} = V_{SS}$	10	28	90	kΩ
$V_{F\ (NRST)}$ (1)	NRST input filtered pulse	-	-	-	1000	ns
$V_{NF\ (NRST)}$ (1)	NRST input unfiltered pulse	-	4000	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

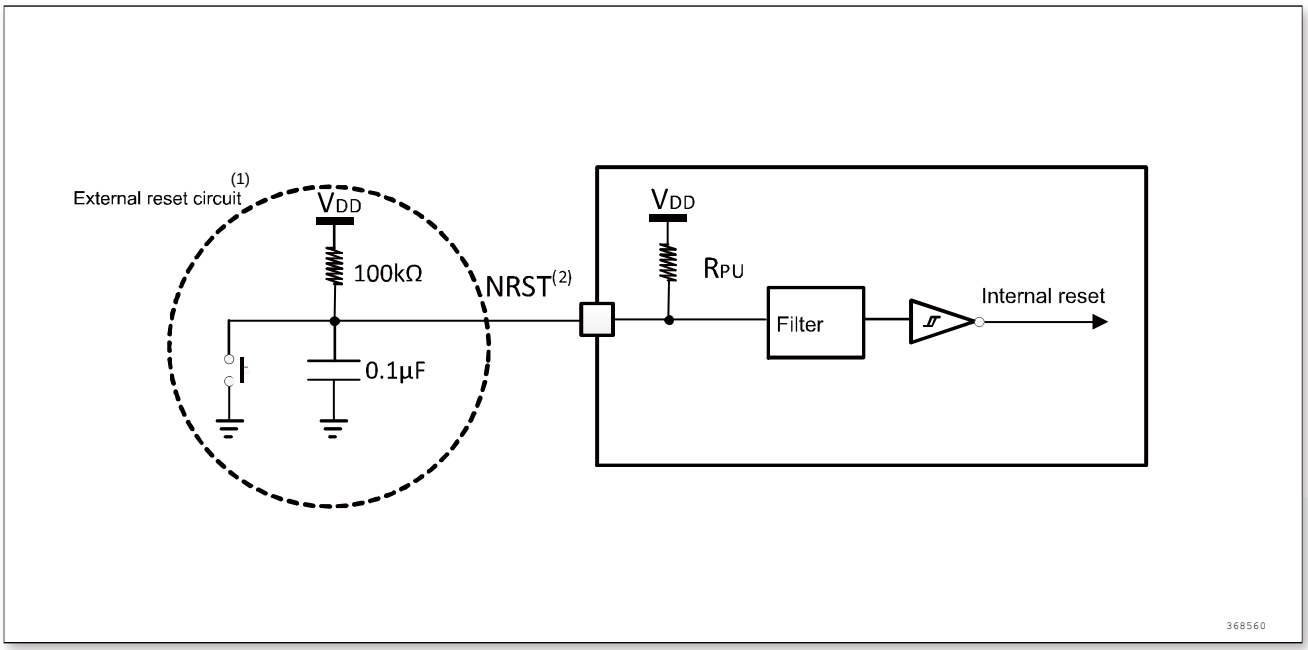

Figure 4-10 Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 4-24, otherwise the MCU cannot be reset.

4.3.13 TIM timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to Section 4.3.11 for details on the input/output alternate function pin (output compare, input capture, external clock, PWM input).

Table 4-25 TIMx(1) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res\ (TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.89	-	ns
f_{EXT}	CH1 to CH4 timer external clock frequency	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	
Res_{TIM}	Timer resolution	-	-	16	Bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.01389	910.2	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	-	59.65	s

4.3.14 Communication interface

I2C interface characteristics

Unless otherwise specified, the parameters given in the table below are derived from the tests performed under the ambient temperature, f_{PCLK1} frequency and VDD supply voltage conditions summarized in Table 4-3.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: the SDA and SCL are not "true" open-drain pins. When configured as open-drain, the PMOS tube connected between the pin and VDD is disabled, but is still present.

I2C interface characteristics are listed in the table below. Refer to section 4.3.11 for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 4-26 I2C interface characteristics

Symbol	Parameter	Standard I2C (1)(2)		Fast mode I2C (1)(2)		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	μs
$t_{w(SCLH)}$	SCL clock high time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	μs
$t_{su(SDA)}$	SDA setup time	$2*t_{PCLK}$	-	$2*t_{PCLK}$	-	ns
$t_{h(SDA)}$	SDA hold time	0(3)	-(4)	0(3)	-(4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{vd(DAT)}$(5)	Data valid time	-	$6*t_{PCLK}$ - 1(4)	-	$6*t_{PCLK}$ - 0.3(4)	μs
$t_{vd(ACK)}$(6)	Data valid acknowledge time	-	$6*t_{PCLK}$ - 1(4)	-	$6*t_{PCLK}$ - 0.3(4)	μs
$t_{h(STA)}$	Start condition hold time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	μs
$t_{su(STA)}$	Start condition setup time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	μs
$t_{su(STO)}$	Stop condition setup time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	μs
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	$5*t_{PCLK}$	-	$5*t_{PCLK}$	-	μs
C_b	Capacitive load of each bus	4.7	-	1.2	-	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. Ensure SCL drops below $0.3V_{DD}$ on falling edge before SDA crosses into the indeterminate range of $0.3V_{DD}$ to $0.7V_{DD}$.

   NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to $0.3V_{DD}$ should be used to insert a delay of the SDA transition with respect to SCL.
4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.

5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.

6. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

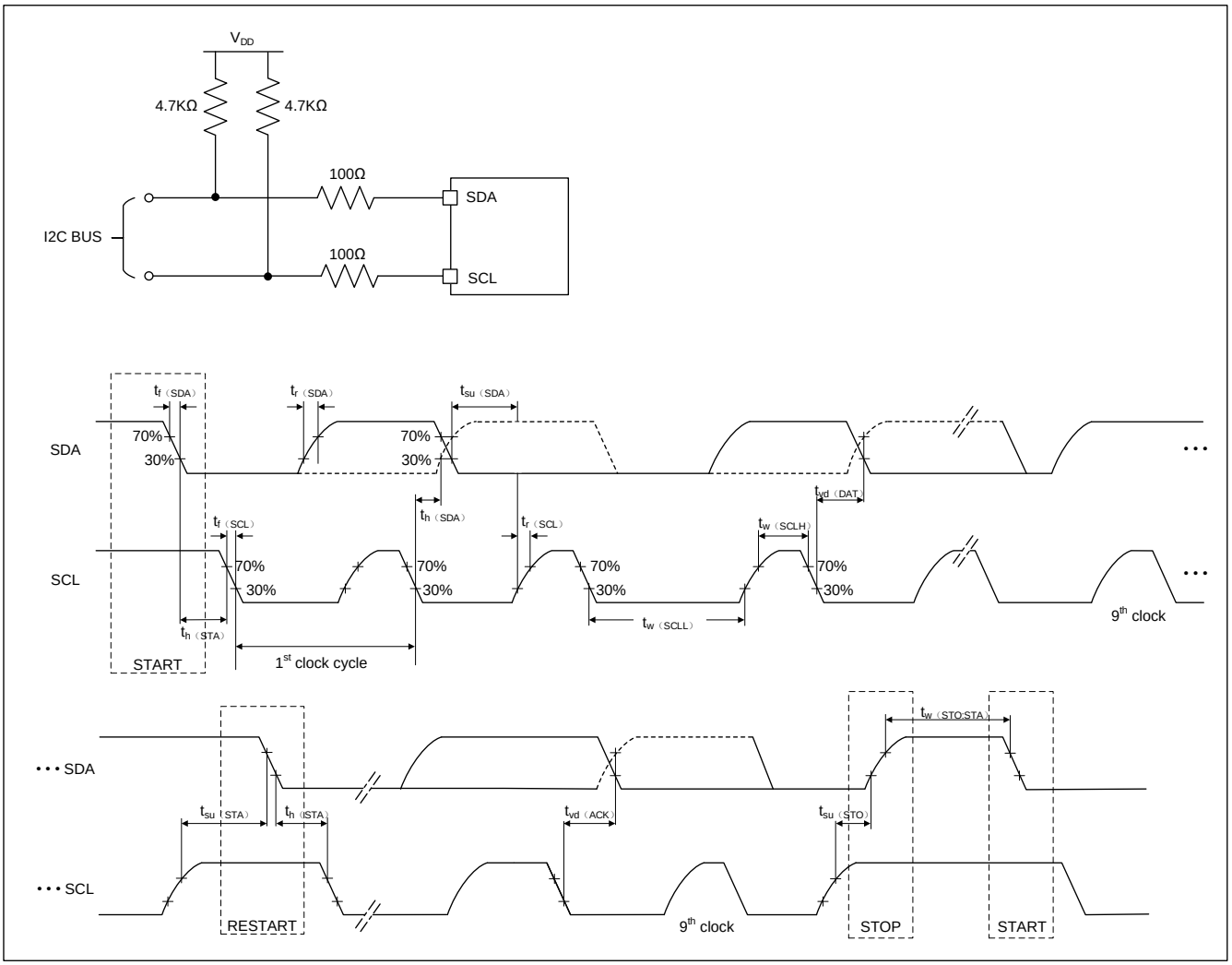

Figure 4-11 I2C bus AC waveform and measurement circuit (1)

1. Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 4.3.11 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 4-27 SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$f_{SCK}1/t_{c\ (SCK)}$	SPI clock frequency	Master mode	-	24	MHz
		Slave mode	-	12	
$t_{r\ (SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$t_{f\ (SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su\ (NSS)}^{(2)}$	NSS setup time	Slave mode	$1t_{PCLK}$	-	ns
$t_{h\ (NSS)}^{(2)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w\ (SCKH)}^{(2)}$	SCK high time	-	$t_{c\ (SCK)}/2-6$	$t_{c\ (SCK)}/2-6$	ns
$t_{w\ (SCKL)}^{(2)}$	SCK low time	-	$t_{c\ (SCK)}/2-6$	$t_{c\ (SCK)}/2-6$	ns
$t_{su\ (MI)}^{(2)}$	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	12	-	ns
$t_{su\ (SI)}^{(2)}$		Slave mode	5	-	ns
$t_{h\ (MI)}^{(2)}$	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	ns
$t_{h\ (SI)}^{(2)}$		Slave mode	6	-	ns
$t_{v\ (SO)}^{(1)(2)}$	Data output valid time	Slave mode (after enabling edge) non-highspeed mode	-	34	ns
$t_{h\ (SO)}^{(2)}$		Slave mode (after enabling edge) highspeed mode	-	13	ns
$t_{h\ (MO)}^{(2)}$	Data output valid time	Master mode (after enabling edge)	-0.6	2	ns

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

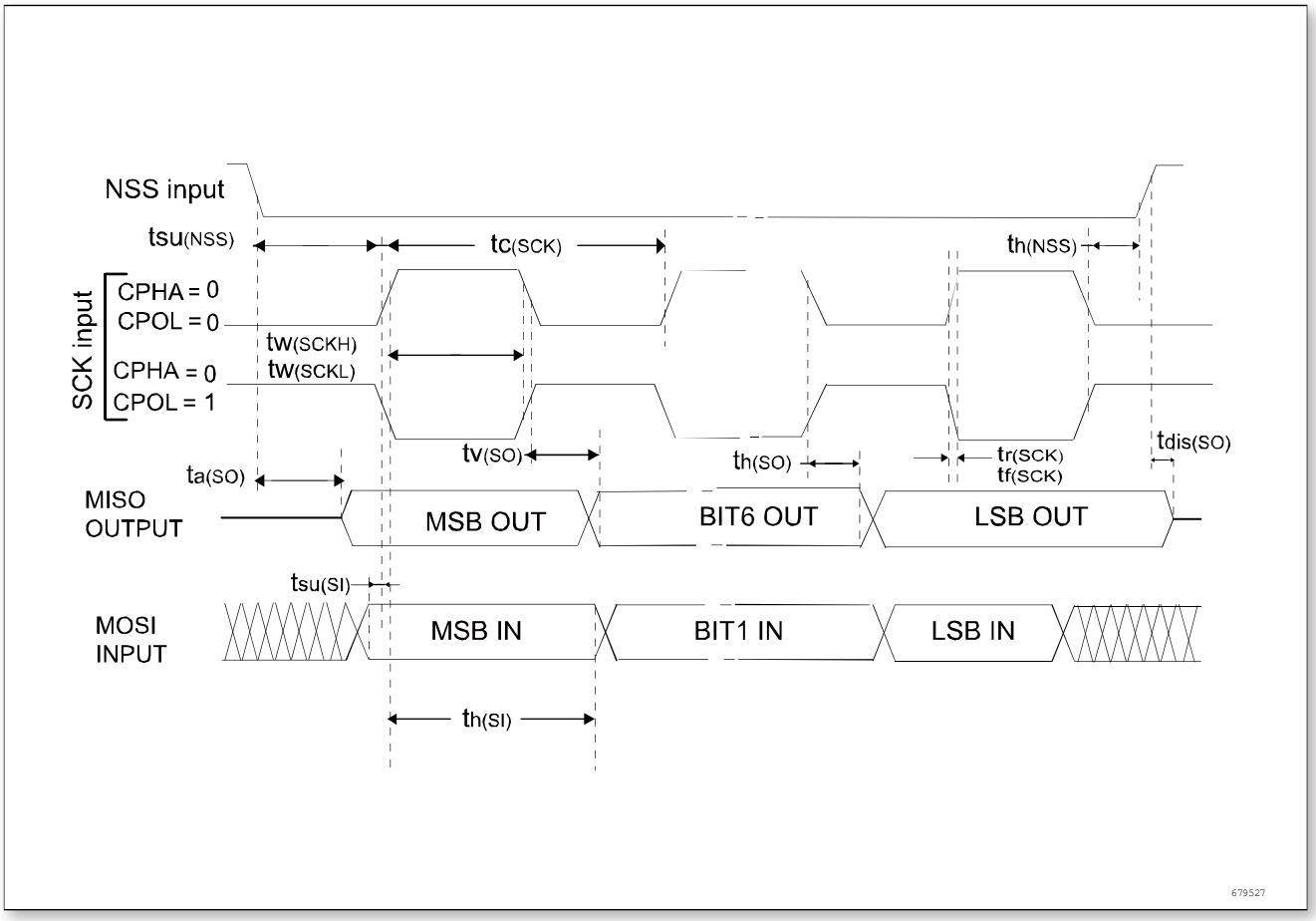

Figure 4-12 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

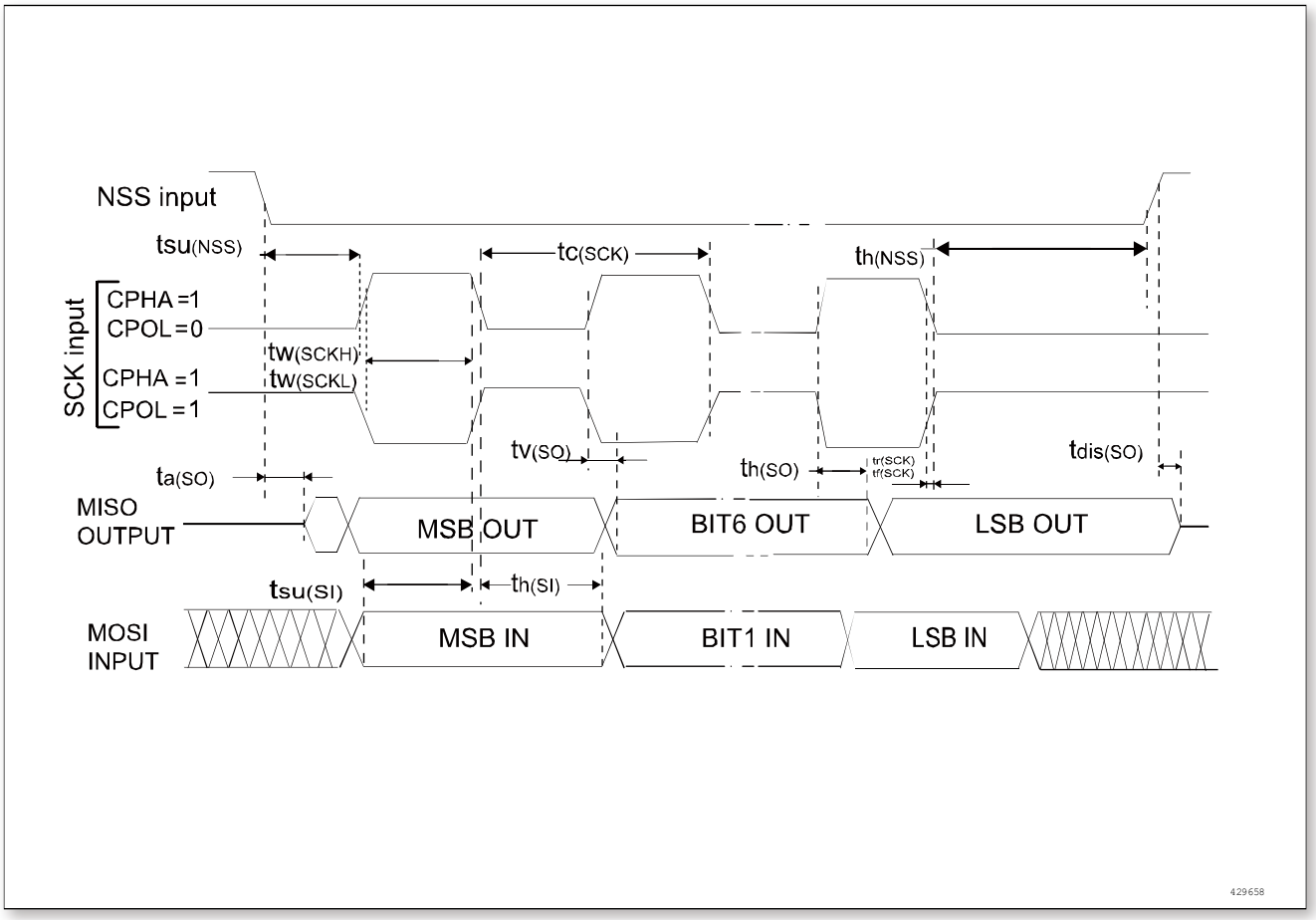

Figure 4-13 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

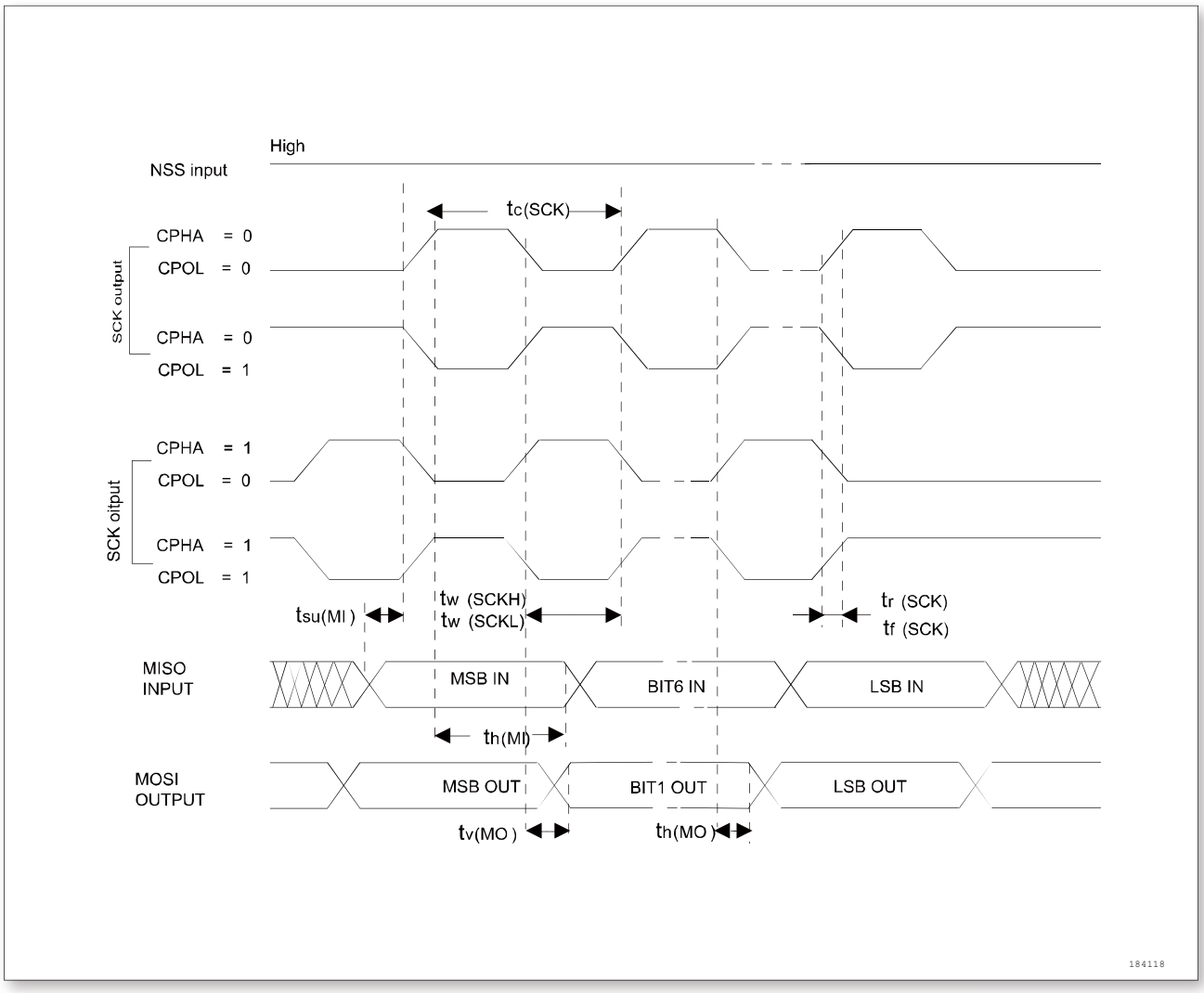

Figure 4-14 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB Characteristics

Table 4-28 USB DC Characteristics

Symbol	Parameter	Condition	Min.(1)	Max.(1)	Unit
V_{DD}	USB operating voltage (2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I (USBDP, USBDM)	0.2	-	
V_{CM}(4)	Range of differential common mode	Include V_{DI} range	0.8	2.5	
V_{SE}(4)	Single-end receiver threshold	-	1.3	2	
V_{OL}	Static output low level	1.5kΩ load resistor is connected to 3.6V(5)	-	0.3	V
V_{OH}	Static output high level	15kΩ load resistor is connected to V_{SS}(5)	2.8	3.6	

1. All voltage measurements shall be made on the ground wire of the device.
2. To be compatible with USB 2.0 full-speed electrical specification, the USBDP(D+) pin has

built in a 1.5 kΩ resistor which is connected to V_{DD}. No external resistor is required.

3. The normal USB function of the product can be guaranteed at 2.7V. Instead of that, electrical characteristics will degrade between 2.7V and 3.6V voltage.
4. Guaranteed by comprehensive evaluation, not tested in production.
5. R_L is the load attached to the USB drive.

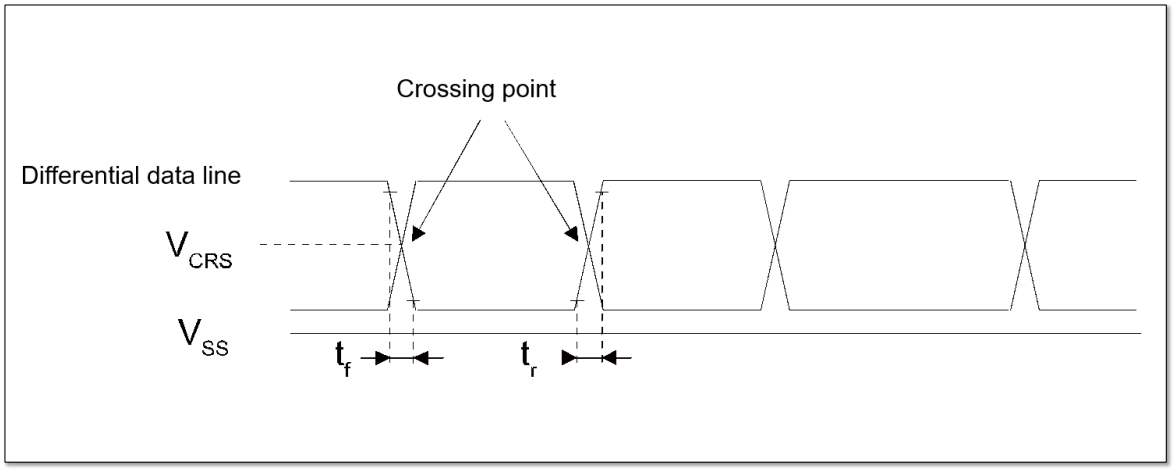

Figure 4-15 USB Timing: Definition of Data Signal Rise and Fall Times

4.3.15 CAN interface

Refer to Section 4.3.11 for the details on characteristics of input/output alternate function pin (CAN_TX and CAN_RX).

4.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters in the following table are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage specified in Table 4-3.

Table 4-29 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S(1)	Sampling rate	-	-	-	1	MHz
f_{TRIG}(1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	-	0	-	V_{DD}	V
R_{AIN}(1)	External input impedance	-	See equation 1 and Table 4-30			kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	-	10	pF
t_S(1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
		-	2.5	-	240.5	$1/f_{ADC}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CONV}(1)	Total conversion time (Including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (Sampling t_S + SAR conversion 12.5)			1/f_{ADC}

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product series, V_{REF+} is connected to V_{DDA}, V_{REF-} connected to V_{SSA} internally.

Equation 1

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula (equation 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB, where N = 12 (12-bit resolution).

Table 4-30 Maximum R_{AIN} under f_{ADC}=16MHz (1)

T_S(cycle)	t_S(us)	Maximum R_{AIN}(kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

Table 4-31 ADC accuracy - limited test conditions (1)(2)

Symbol	Parameter	Conditions	Typical	Unit	Symbol
Resolution	Resolution		12		BIT
ET	Composite error	f_{PCLK2} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 KΩ, V_{DDA} = 3.3V, T_A = 25°C	3.4/-2.3		LSB
EO	Offset error		-2.5		
EG	Gain error		3.7		
ED	Differential linearity error		1/-1		
EL	Integral linearity error		1.8/ -3		

1. Correlation between ADC accuracy and negative injection current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input pin. It is recommended to add a Schottky diode (pin to ground) to standard analog pins that may potentially inject negative current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Table 4-2, the ADC accuracy will not be affected.

2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: the maximum deviation between the actual and ideal transfer curves.

EO = Offset error: the deviation between the first actual transition and the first ideal one.

EG = Gain error: the deviation between the last ideal transition and the last actual one.

ED = Differential linearity error: the maximum deviation between the actual steps and the ideal ones.

EL = Integral linearity error: the maximum deviation between any actual transition and the endpoint correlation line.

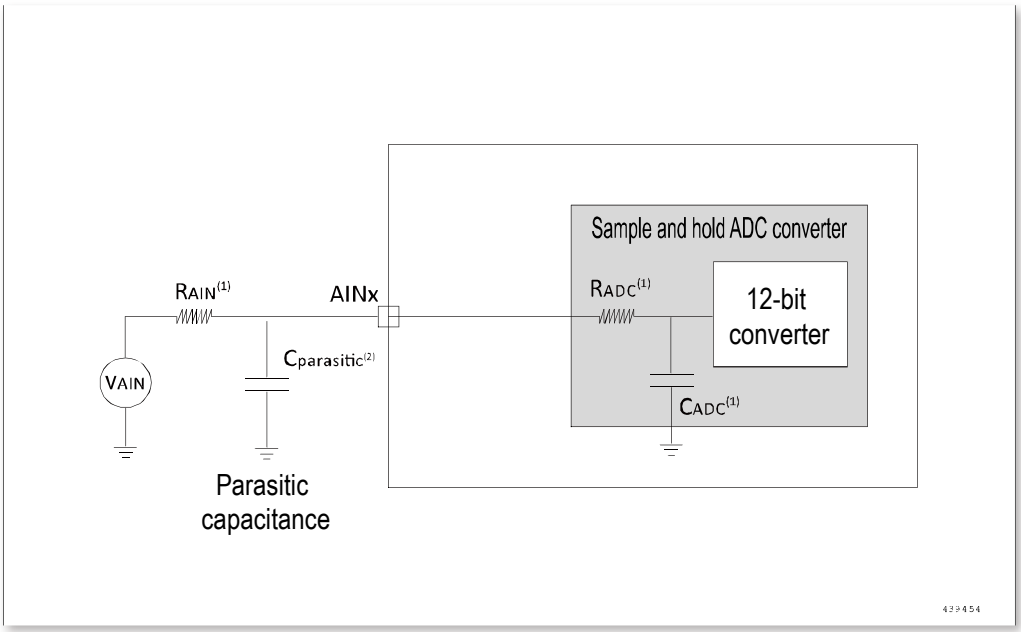

Figure 4-16 Typical connection diagram using ADC

1. Refer to Table 4-31 for the values of R_{AIN}, R_{ADC} and C_{ADC}.

2. $C_{parasitic}$ represents the parasitic capacitance (about 7pF) on the PCB (dependent on soldering and PCB layout quality) and the pad. A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design guidelines

Power supply decoupling should be performed as shown in the diagram below. The 10 nF capacitor should be ceramic and it should be placed as close as possible to the MCU chip.

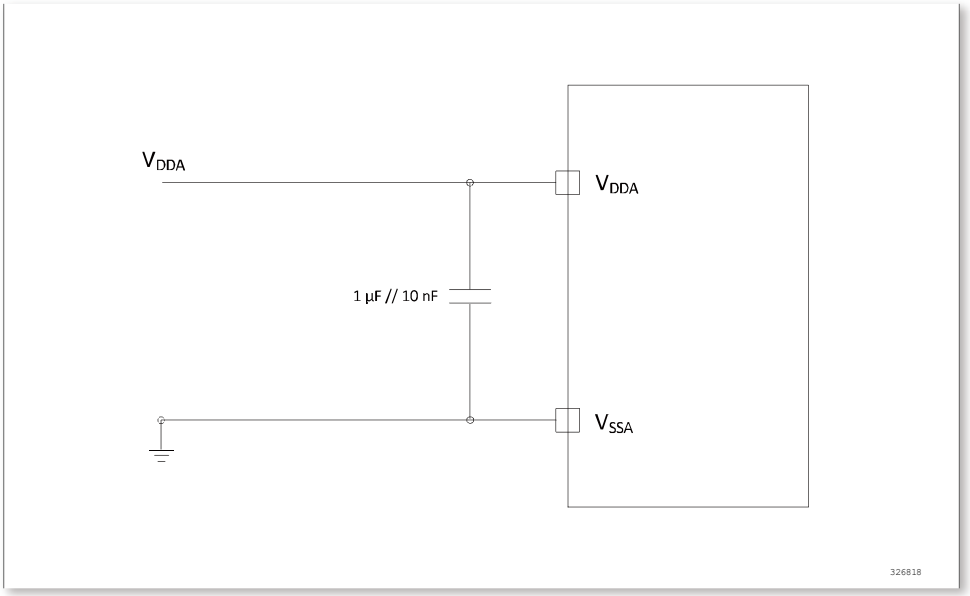

Figure 4-17 Decoupling circuit of power supply and reference power supply

4.3.17 Temperature sensor characteristics

Table 4-32 Temperature sensor characteristics (3)(4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L(1)	V_{SENSE} linearity with temperature		±5		℃
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/℃
V_{25}(1)	Voltage at 25℃	-	offset(5)	-	V
t_{start}(2)	Establishment time	-	-	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature	10	-	-	µs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by application through multiple circulations.
4. V_{DD} = 3.3V.
5. Temperature formula: TS_adc = 25 + (value * vdda – offset * 3300) / (4096 * Avg_slope), offset recorded in 0x1FFFF7F6 low 12-bit.

4.3.18 Comparator characteristics

Table 4-33 Comparator characteristics

Symbol	Parameter	Register configuration	Min.	Typ.	Max.	Unit
HYST	Hysteresis	00	-	0	-	mV
		01	-	15	-	mV
		10	-	30	-	mV
		11	-	90	-	mV

Symbol	Parameter	Register configuration	Min.	Typ.	Max.	Unit
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
		01	3.23	7.51	12.08	mV
		10	9.79	15	20.8	mV
		11	34.25	47.4	62.22	mV
DELAY	Propagation delay(1)	00	-	80	-	ns
		01	-	51	-	ns
		10	-	26	-	ns
		11	-	9	-	ns
I_q(2)	Average operating current	00	-	4.5	-	μA
		01	-	4.4	-	μA
		10	-	4.4	-	μA
		11	-	4.4	-	μA

1. Time difference between output flip 50% and input flip.
2. Mean value of the total consumption current, running current.

5 Package dimensions

5.1 Package LQFP64

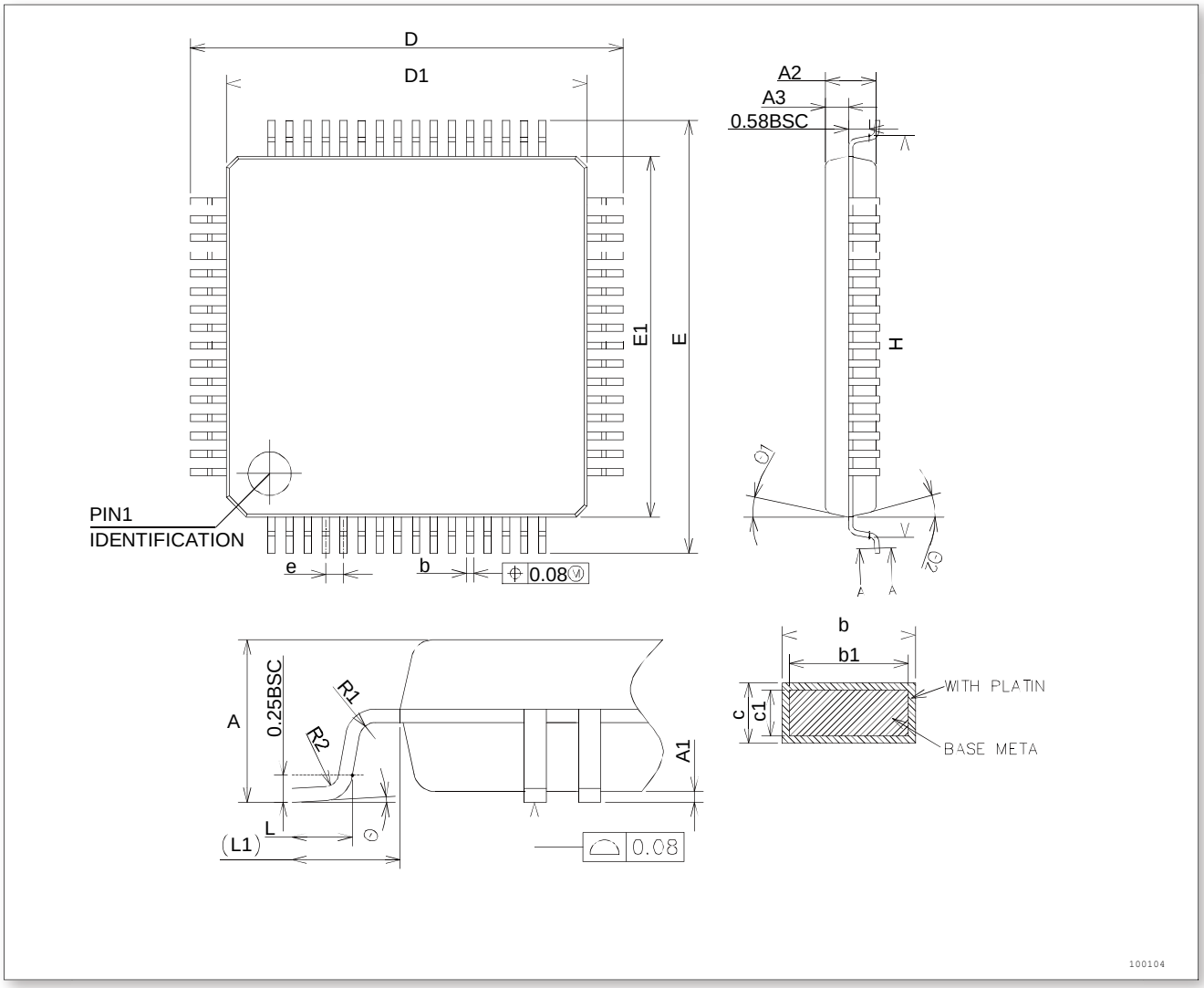

Figure 5-1 LQFP64, 64-pin low-profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-1 LQFP64 dimensions

Symbol	Millimeter		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0 ◦	3.5 ◦	7 ◦
θ1	11 ◦	12 ◦	13 ◦
θ2	11 ◦	12 ◦	13 ◦

5.2 Package LQFP48

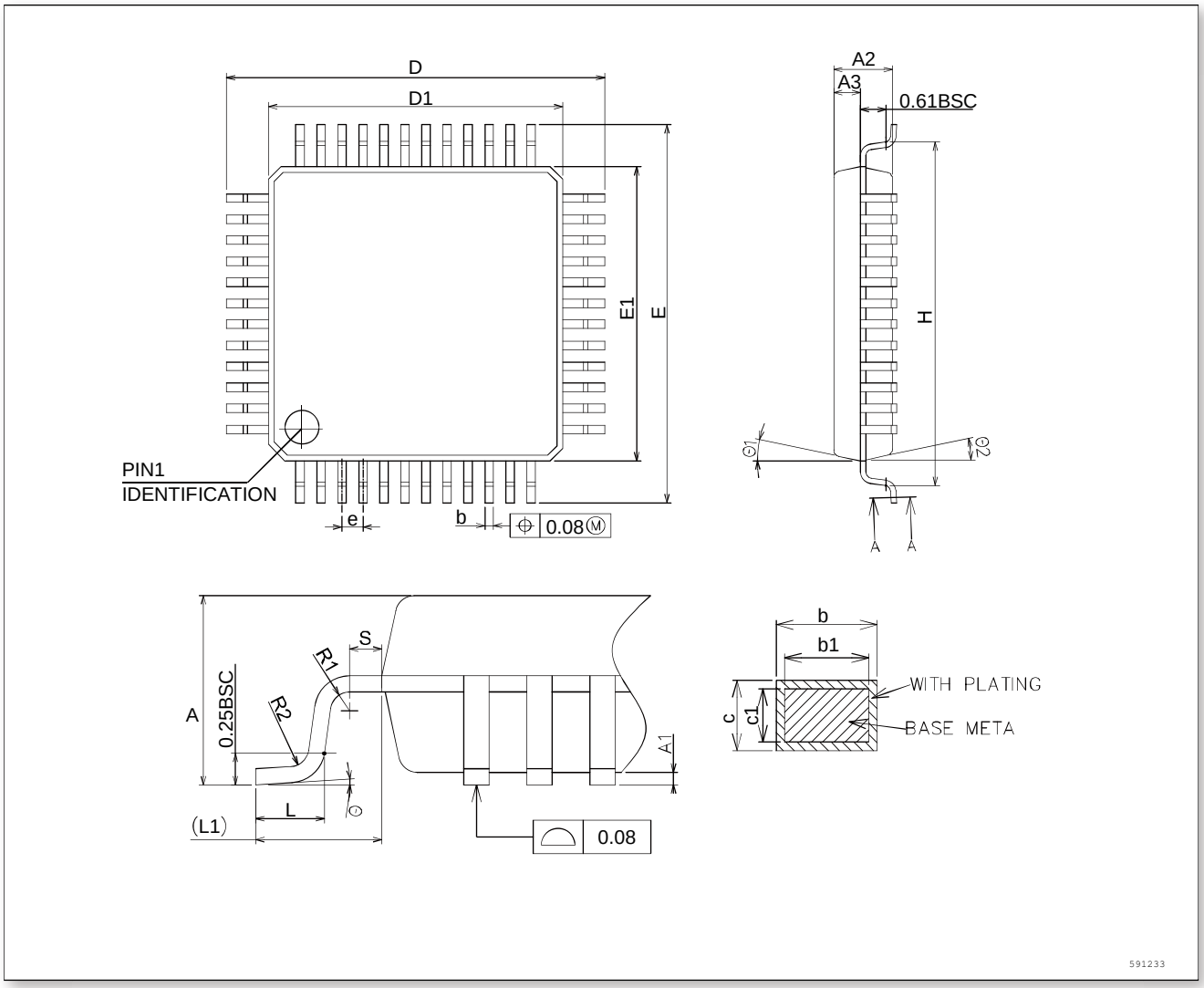

Figure 5-2 LQFP48, 48-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-2 LQFP48 dimensions

Symbol	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0 ◦	3.5 ◦	7 ◦
θ 1	11 ◦	12 ◦	13 ◦
θ 2	11 ◦	12 ◦	13 ◦

5.3 Package LQFP32

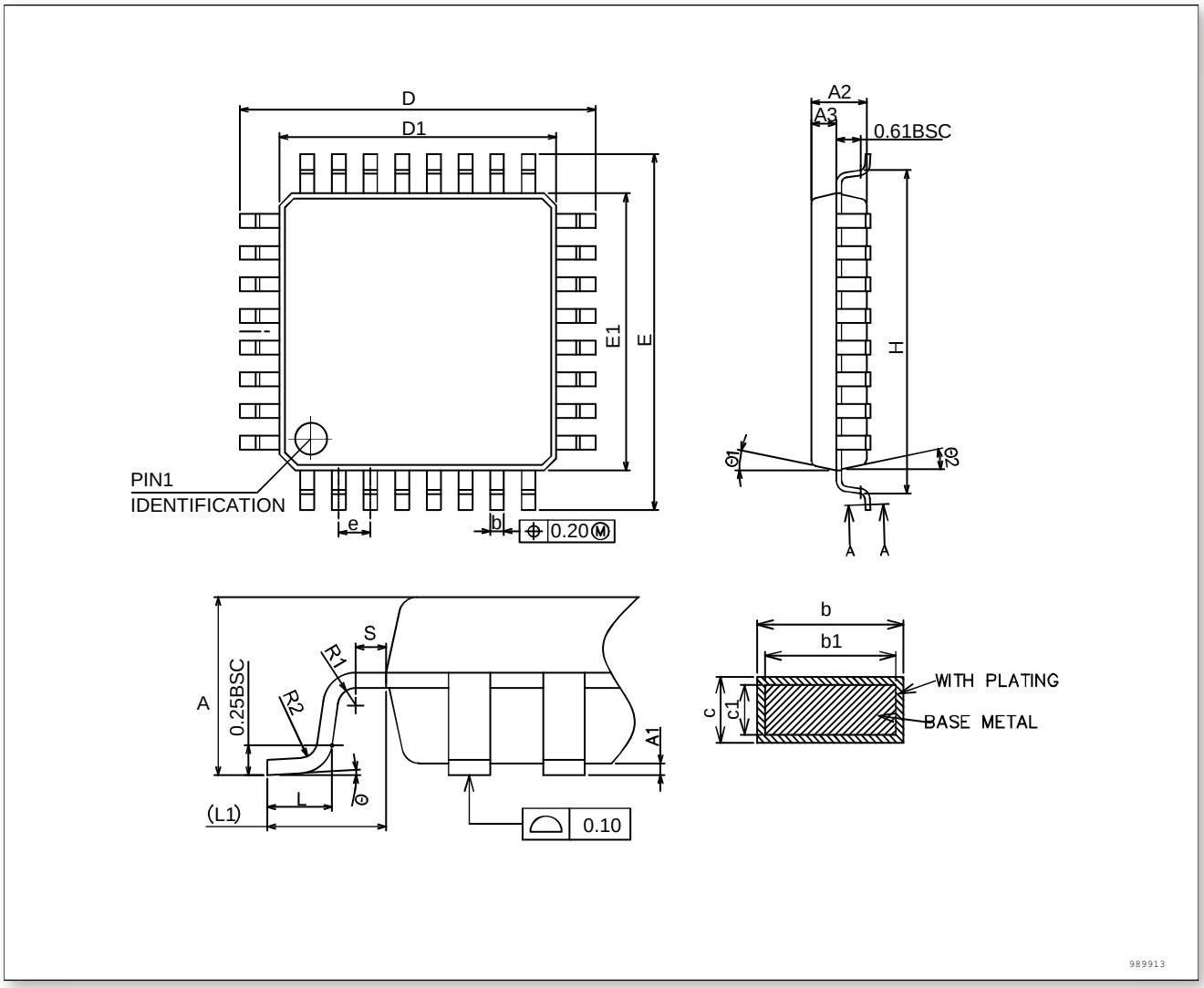

Figure 5-3 LQFP32, 32-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-3 LQFP32 dimensions

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0 ◦	3.5 ◦	7 ◦
θ1	11 ◦	12 ◦	13 ◦
θ2	11 ◦	12 ◦	13 ◦

5.4 Package QFN32

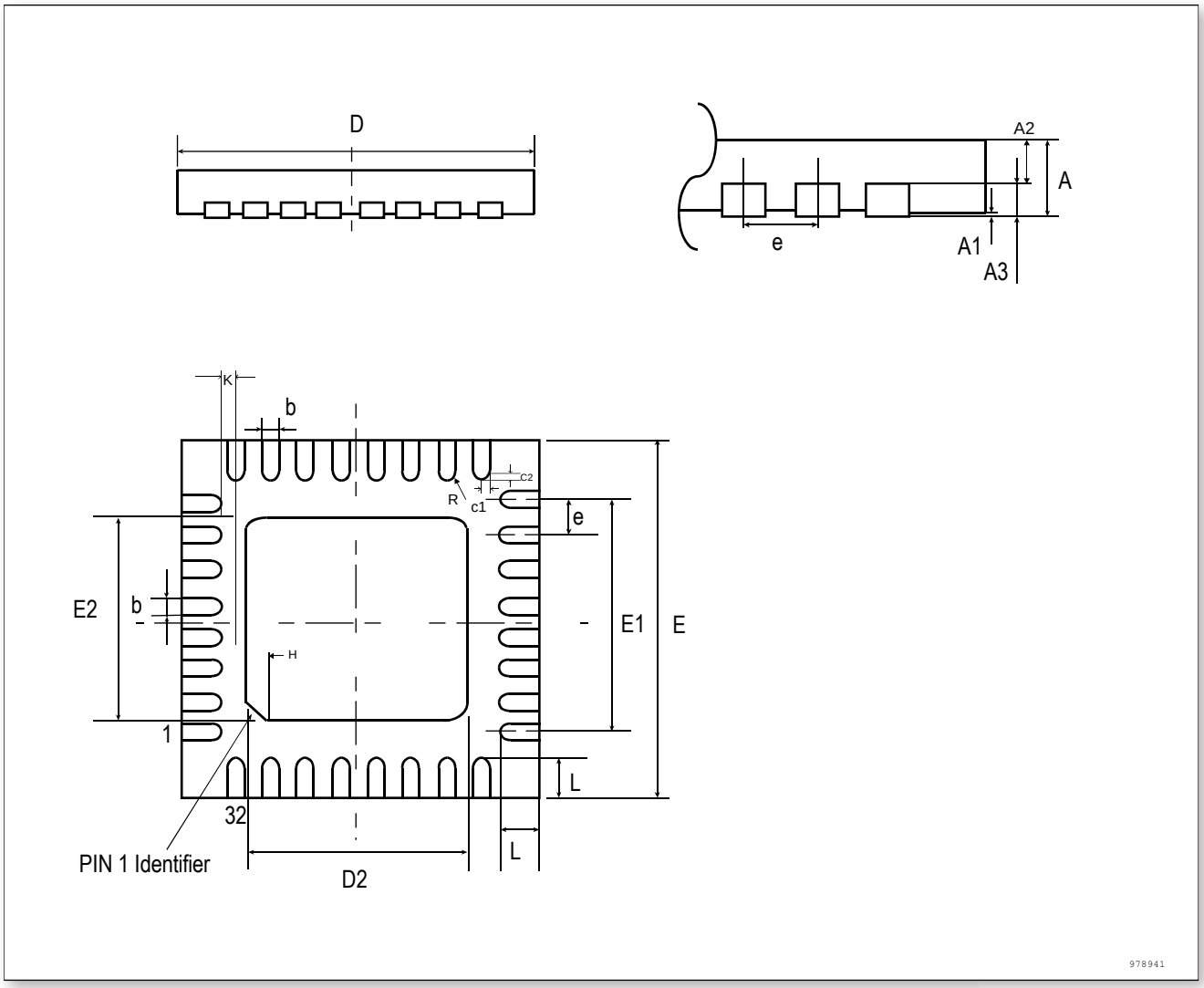

Figure 5-4 QFN32 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 5-4 QFN32 dimensions

ID	Millimeters		
	Minimum	Typical	Minimum
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e		0.5	
H	0.30REF		
K	0.35REF		
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-

5.5 Package QFN28

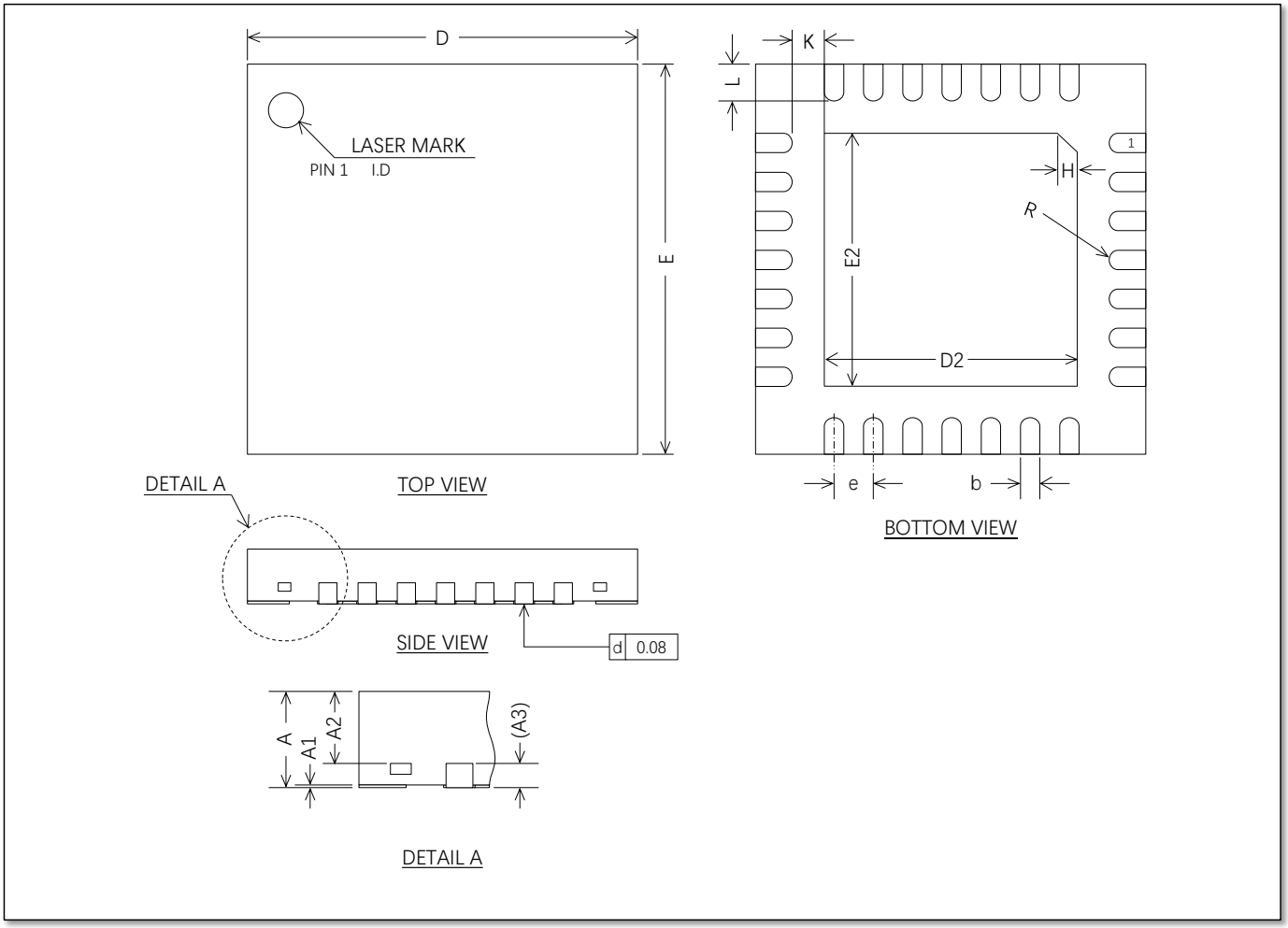

Figure 5-5 QFN28 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 5-5 QFN28 dimensions

ID	Millimeters		
	Minimum	Typical	Minimum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.30	0.40	0.50
H	0.35REF		
K	0.30REF		
L	0.35	0.40	0.45
R	0.075	-	-

6 Part identification

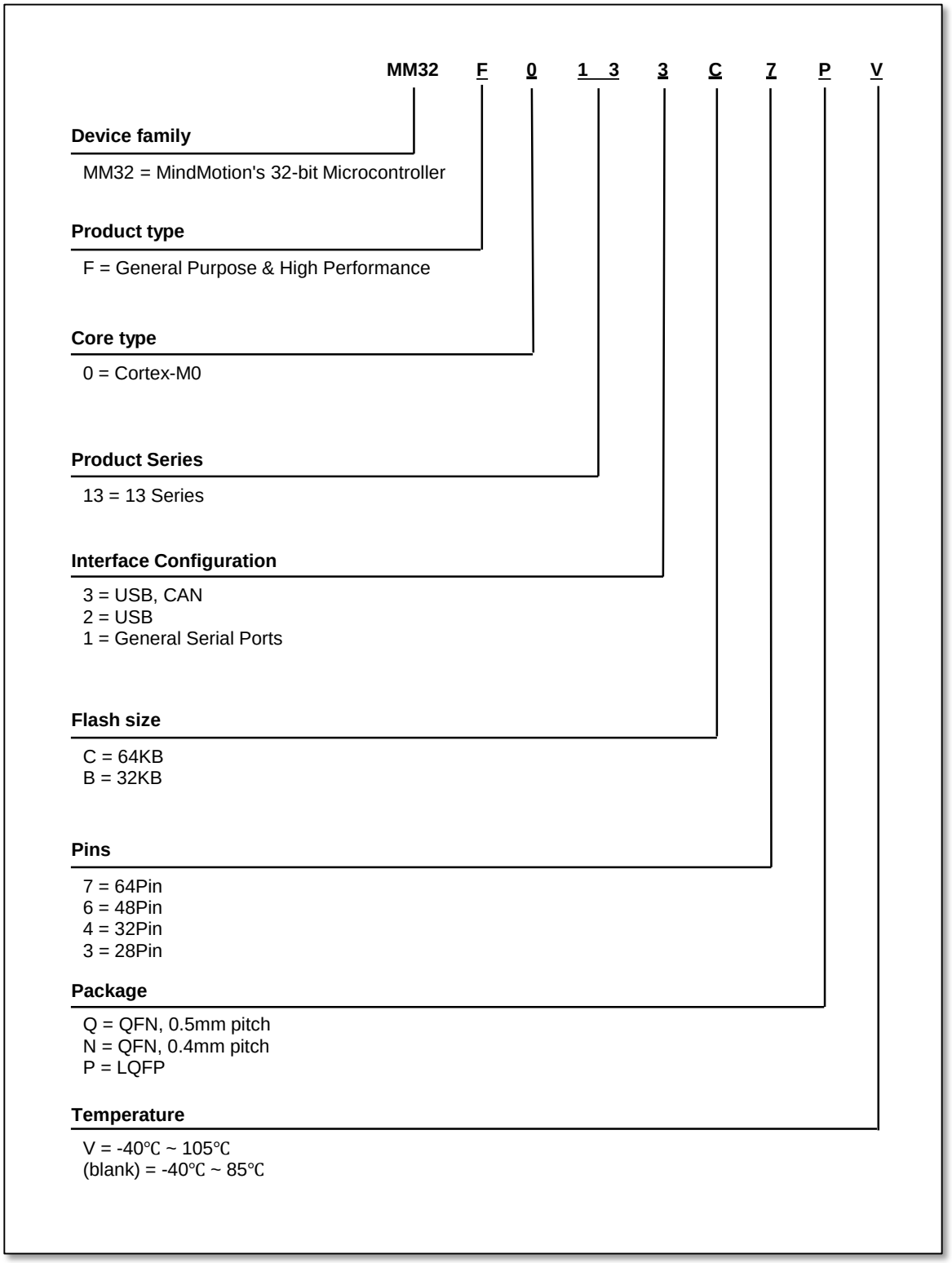

Figure 6-1 Part number naming rule

7 Abbreviation

ADC	Analog Digital Converter
BKP	Backup Register
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access Controller
EXTI	External Interrupt Event Controller
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FLASH	Flash Memory
GPIO	General-Purpose Input/Output
HSE	External High Speed Clock
HSI	Internal High Speed Clock
I2C	Inter-Integrated Circuit
IWDG	Independent Watchdog
LP	Low Power
LSI	Internal Low Speed Clock
NVIC	Nested Vectored Interrupt Controller
PWR	Power Control
POR	Power On Reset
PDR	Power Down Reset
PVD	Voltage Detector
RCC	Reset Clock Controller
RTC	Real-time Clock
SRAM	Static Random Access Memory
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug Interface
SysTick	System Tick Timer
Sleep	Sleep
Stop	Stop
Standby	Standby

TIM	Timer
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

8 Revision history

Table 8-1 Revision history

Date	Revision	Description
2023/3/20	Rev2.24	• Updated maximum power consumption of Stop mode
2022/06/07	Rev2.23	• Updated IO parameters
2022/05/17	Rev2.22	• Updated NRST & OSC application diagram • Added maximum value at room temperature in Stop and Standby mode
2022/01/20	Rev2.21	• Fixed the maximum value of voltage characteristics • Added new condition to HSI oscillator accuracy table
2021/12/30	Rev2.2	• Updated marking description • Updated ESD characteristics • Fixed I2C communication diagram wrong description • Updated V_{DDA} operating condition
2021/07/06	Rev2.01	• Updated PB port pin multiplexing • Updated ESD characteristics • Updated power-on and power-down operating conditions
2021/05/18	Rev2.00	• Added QFN28 package • Added package marking figures
2020/07/02	Rev1.00	Formal version