Data Sheet

MM32F0160

Arm® Cortex®-M0 based 32-bit Microcontrollers

Revision: 1.1

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1 Introduction

1.1 Overview

The MM32F0160 microcontrollers are based on Arm® Cortex®-M0 core. These devices have a maximum clocked frequency of 96MHz, built-in 128KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, two analog comparators, one 16-bit advanced timer, one 16-bit and one 32-bit general purpose timers, three 16-bit basic timers, one low power timer and one real-time clock (RTC) module, as well as communication interfaces including one I2C, one I3C slave, two SPI or I2S, four UART, one low power UART, one USB interface and one FlexCAN-FD interface.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) includes the industrial tier -40°C to 85°C and the extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Industrial IoT devices
- PC accessories
- Electronic door lock
- Medical and healthcare devices
- Handheld devices
- Gaming and entertainment

These devices are available in LQFP64, LQFP48, LQFP44, QFN32 and QFN28 packages.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M0.
  - Frequency up to 96MHz.
  - 32-bit hardware divider
- Memory
  - Up to 128KB embedded Flash storage.
  - Up to 16KB SRAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Programmable voltage detector

(PVD).

- 4 to 24MHz high speed crystal oscillator.
- 8MHz factory-trimmed high speed RC oscillator.
- Integrated PLL1 to generate system clock and support multiple prescaler rate to provide clock sources to bus matrix and peripherals.
- Integrated PLL2 to generate independent clock source for USB and FlexCAN-FD.
- 40KHz low speed oscillator.
- External 32.768KHz low speed oscillator (with LSE Bypass function).

- Low power
  - Multiple low power modes including Sleep mode, Stop mode, Deep Stop mode and Standby mode.
- One DMA controller with 7 channels to support peripherals including timers, ADC, UART, LPUART, I2C, I3C, SPI, and FlexCAN-FD.
- Total 10 timers:
  - One 16-bit 4-channel advanced timer (TIM1), each channel providing two PWM output including one complementary output, supports hardware dead-time insertion and emergency break when fault detected.
  - One 16-bit general purpose timer (TIM3) and one 32-bit general purpose timer (TIM2), with up to four input capture or output compare channels and can be used for infrared decode.
  - Three 16-bit basic timers (TIM14 / TIM16 / TIM17), with one input capture or output compare channel. TIM16 and TIM17 have one complementary output, support hardware dead-time insertion, emergency break when fault detected, and integrated modulator circuit for infrared control.
  - One 16-bit low power timer (LPTIM), able to wake up CPU in all low power modes except for Standby mode.
  - Two watchdog timers, including one independent watchdog (IWDG) and one window watchdog (WWDG).
  - One 24-bit Systick timer.
- One real-time clock (RTC) module
- Up to 57 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level is not higher than V_{DD}.
- Up to 11 communication interfaces:
  - Four UART.
  - One low power UART (LPUART).
  - One I2C.
  - One I3C slave.

  - Two SPI (support I2S mode).
  - One USB Device interface.
  - One FlexCAN-FD module supports CAN 2.0B and CAN-FD interface.
- One 12-bit Analog-to-Digital converter (ADC), support 1μs conversion duration, with up to 14 external inputs and 2 internal inputs
  - Conversion range: 0 to V_{DDA}.
  - Configurable sampling cycles and resolution.
  - On-chip temperature sensor.
  - On-chip voltage sensor.
- Two high speed analog comparators
- Embedded CRC engine
- 96bit unique chip ID (UID)
- Debug mode
  - Serial Wire Debug (SWD).
- Available in LQFP64, LQFP48, LQFP44, QFN32 and QFN28 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32 F0161 D3N *	MM32 F0164 D3N *	MM32 F0162 D4Q	MM32 F0163 D4Q(V)	MM32 F0162 DAP *	MM32 F0163 DAP *	MM32 F0162 D6P	MM32 F0163 D6P(V)	MM32 F0162 D7P	MM32 F0163 D7P(V)
CPU frequency		96 MHz									
Flash - KB		128	128	128	128	128	128	128	128	128	128
SRAM - KB		16	16	16	16	16	16	16	16	16	16
Timers	16-bit GP	1	1	1	1	1	1	1	1	1	1
	32-bit GP	1	1	1	1	1	1	1	1	1	1
	Basic	3	3	3	3	3	3	3	3	3	3
	Advanced	1	1	1	1	1	1	1	1	1	1
	Low power	1	1	1	1	1	1	1	1	1	1
RTC		√	√	√	√	√	√	√	√	√	√
Interfaces	UART	4	4	4	4	4	4	4	4	4	4
	LPUART	1	1	1	1	1	1	1	1	1	1
	I2C	1	1	1	1	1	1	1	1	1	1
	I3C slave	1	1	1	1	1	1	1	1	1	1
	SPI / I2S	1 (SPI1/I2S 1)	1 (SPI1/I2S 1)	2	2	2	2	2	2	2	2
	USB Device	-	-	1	1	1	1	1	1	1	1
	FlexCAN -FD	-	1	-	1	-	1	-	1	-	1
GPIO		24	24	28	28	40	40	41	41	57	57
12-bit ADC	Modules	1	1	1	1	1	1	1	1	1	1
	Channels	13	13	13	13	13	13	13	13	14	14
Comparator		2	2	2	2	2	2	2	2	2	2
Supply voltage		2.0V to 5.5V									
Temperature range		-40°C to +85°C / -40°C to +105°C									
Package		QFN28		QFN32		LQFP44		LQFP48		LQFP64	

Note: part numbers marked with “*” are still under development, please contact MindMotion for more information

2.2 Marking information

Notes about the marking: The purpose of this section is to guide users to identify the required information from the chip marking, and the format (including font, font size, alignment, etc.), position, proportion, etc. in the marking figures may be different from the actual chip marking, and the marking of some packages may not contain MindMotion logo, such format, position, proportion, logo, etc. information, please refer to the actual chips.

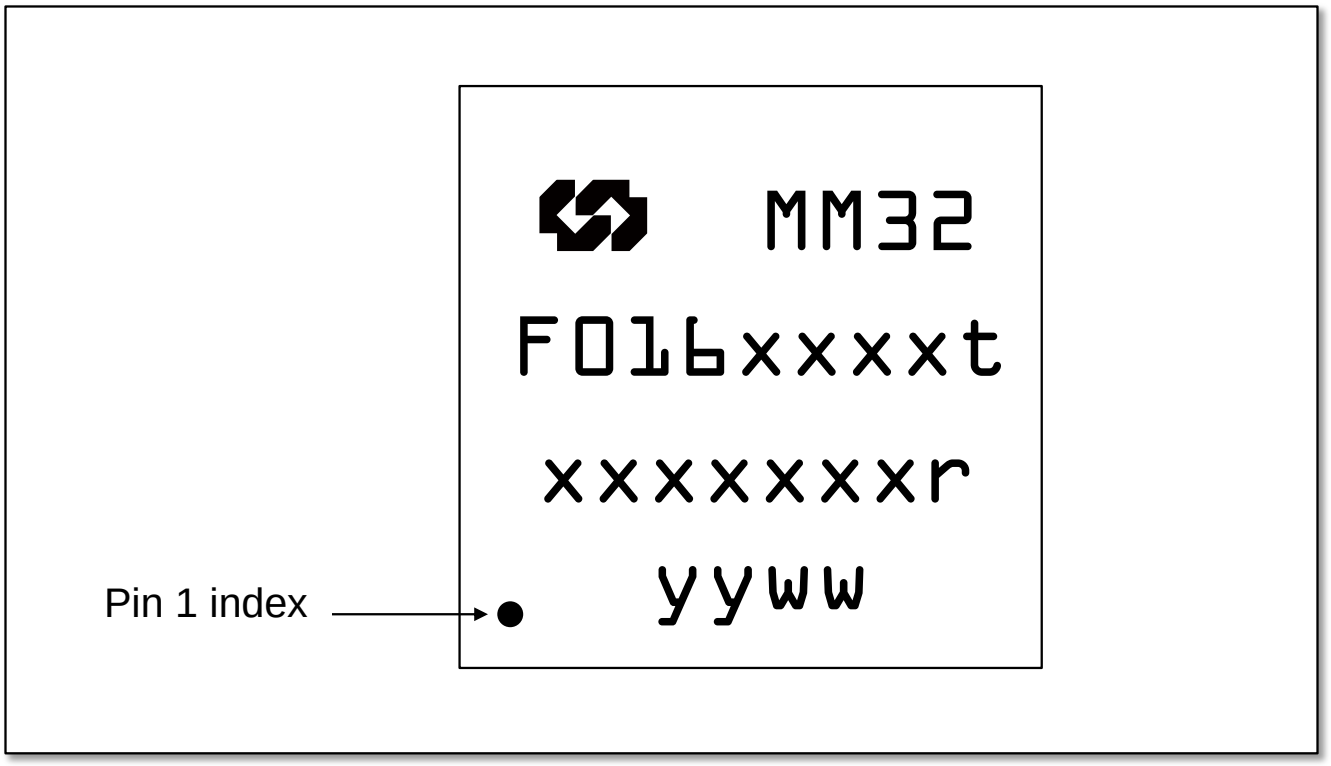

Figure 2-1 LQFP or QFN32 package marking

LQFP or QFN32 package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F016xxxxt
  - Second part of product name, where “t” represents temperature level. “t” = “Empty” means -40 to 85°C (industrial), e.g., F0163D7P. “t” = “V” means -40 to -105°C (extended industrial), e.g., F0162D6PV.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

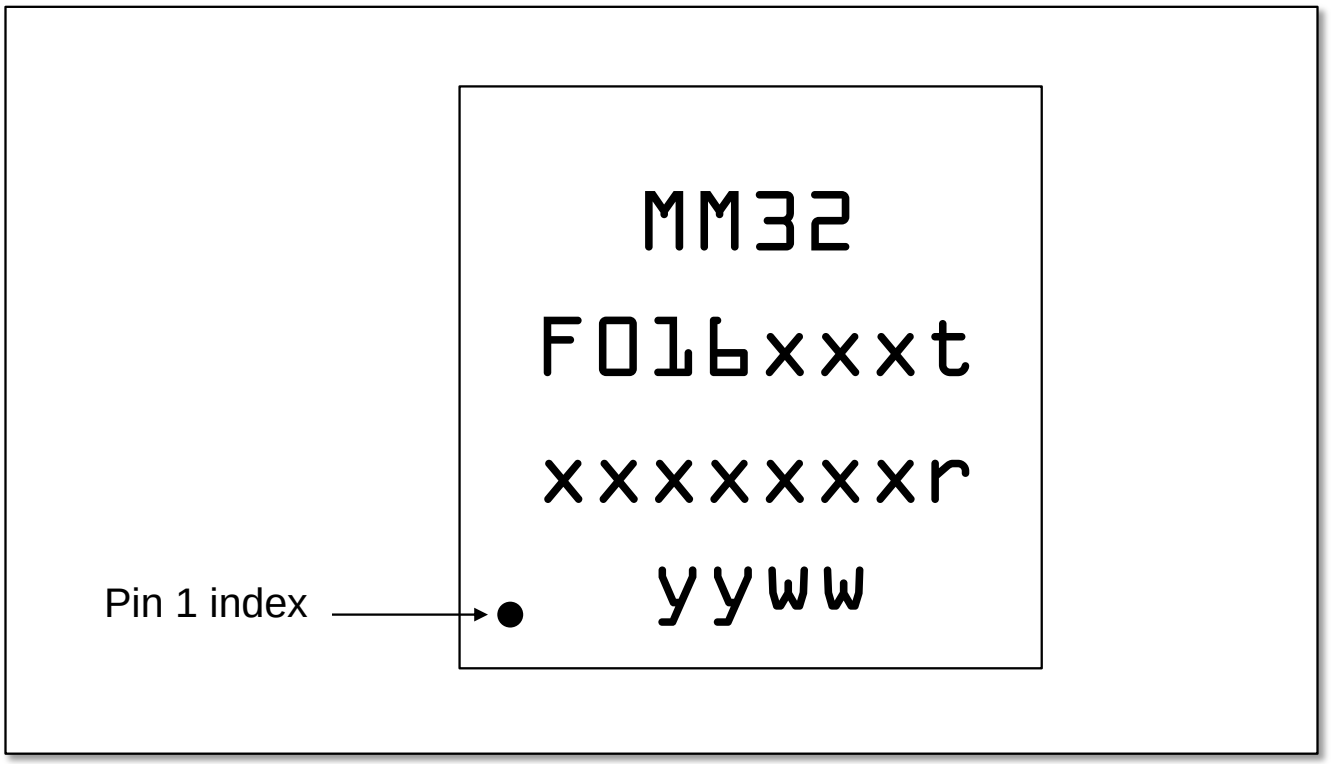

Figure 2-2 QFN28 package marking

QFN28 package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F016xxxt
  - Part of the part number + temperature level, where “t” represents temperature level. “t” = “N” means -40 to 85°C (industrial), e.g., F0163D3N; “t” = “V” means -40 to -105°C (extended industrial), e.g., F0163D3V.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.3 Part identification

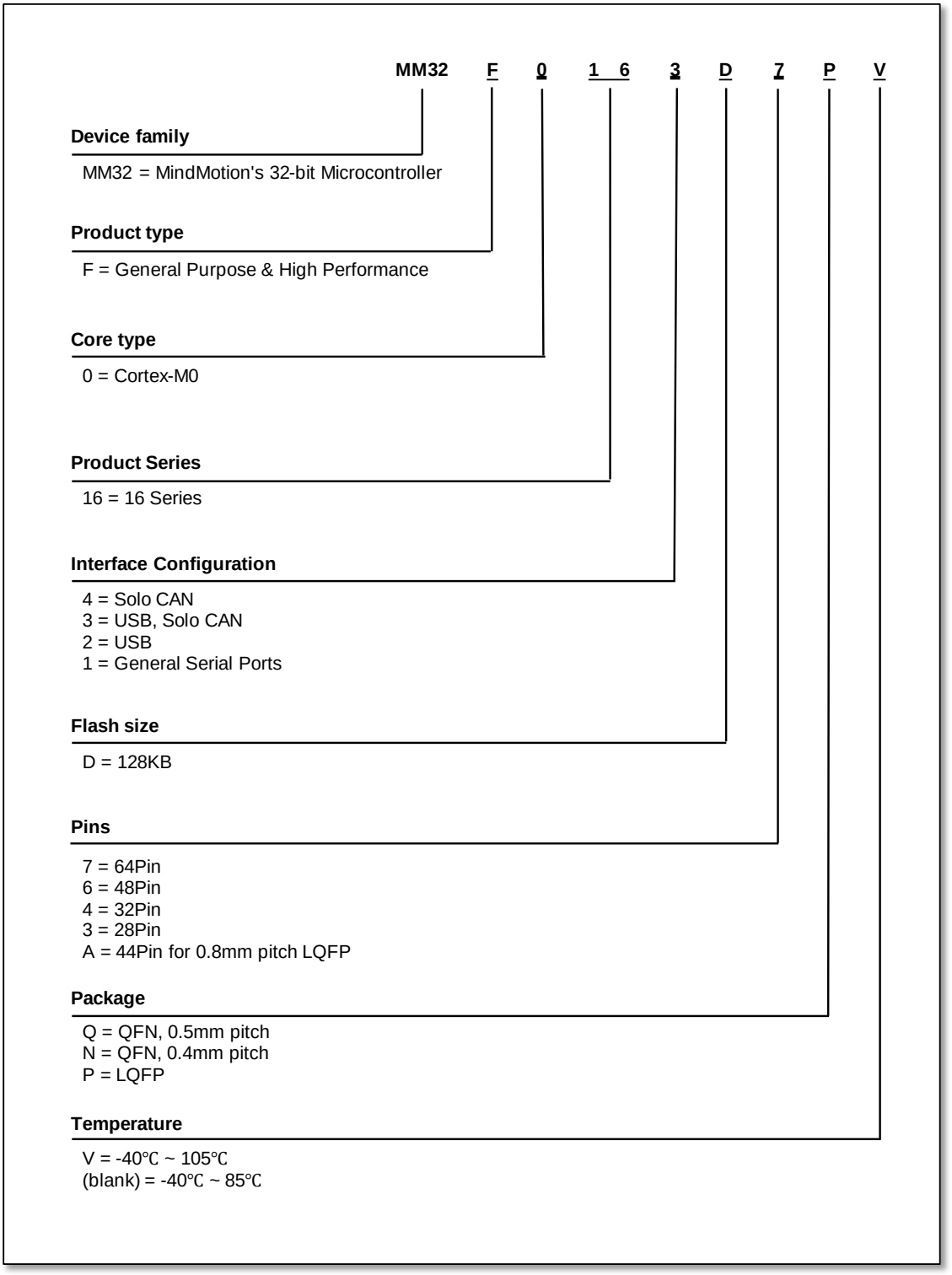

Figure 2-3 Part number naming rule

3 Functional description

3.1 Block diagram

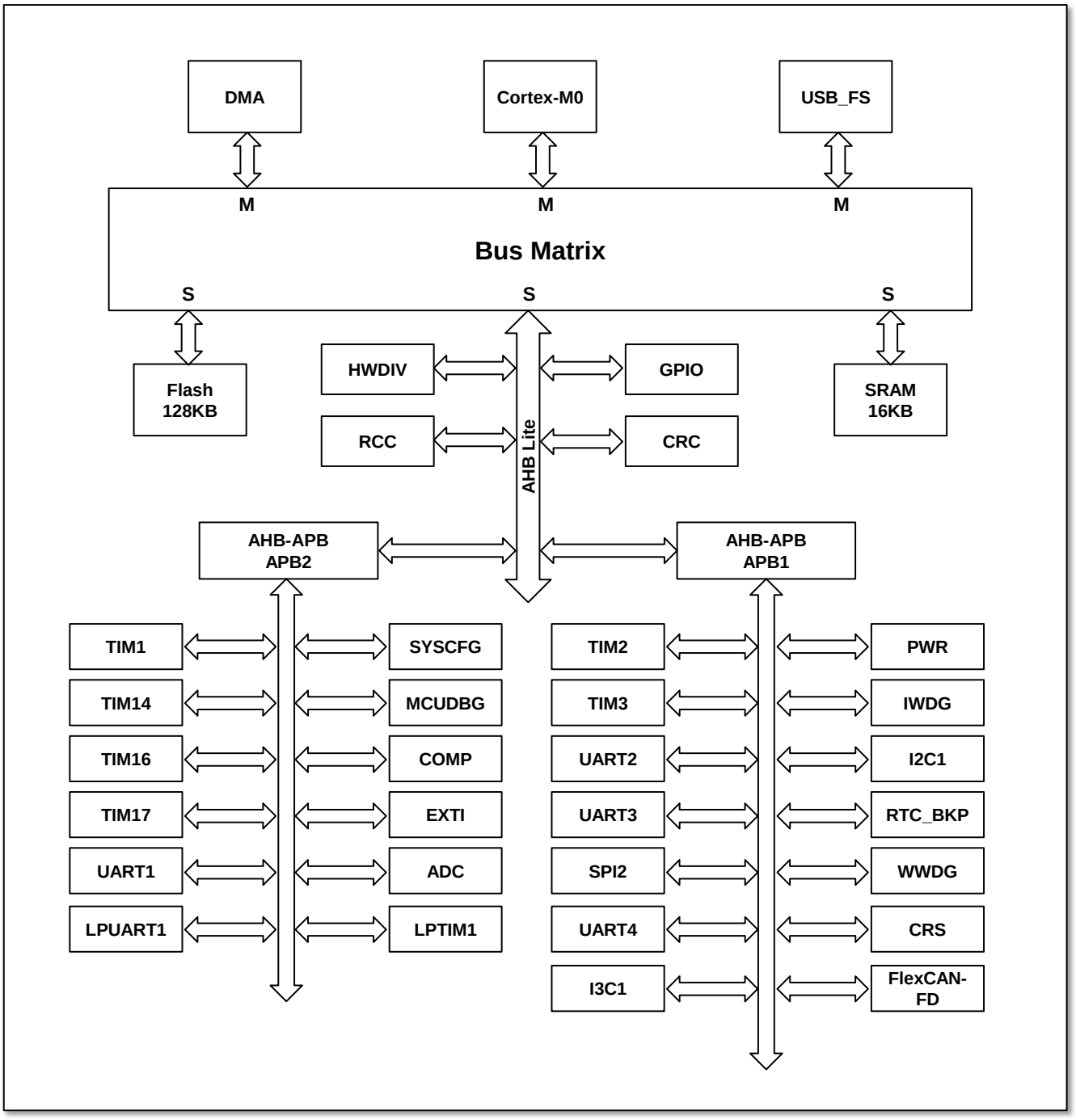

Figure 3-1 System block diagram

3.2 Core introduction

The Arm® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The Arm® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded Arm core, this product is compatible with all the tools and software for Arm-based products.

3.3 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, HWDIV, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.4 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x00000000 - 0x0001FFFF	128 KB	Map to main Flash, system memory or SRAM according to boot configuration
	0x00020000 - 0x07FFFFFF	127.875 MB	Reserved
	0x08000000 - 0x0801FFFF	128 KB	Main Flash
	0x08020000 - 0x1FFE0FFF	~384 MB	Reserved
	0x1FFE1000 - 0x1FFE25FF	5.5 KB	Encrypted area
	0x1FFE2600 - 0x1FFFF3FF	115.5 KB	Reserved
	0x1FFFF400 - 0x1FFFF7FF	1 KB	System memory
	0x1FFFF800 - 0x1FFFF9FF	0.5 KB	Option bytes
	0x1FFFFA00 - 0x1FFFFFFF	1.5 KB	Reserved
SRAM	0x20000000 - 0x20003FFF	16 KB	SRAM
	0x20004000 - 0x3FFFFFFF	~512 MB	Reserved
APB1	0x40000000 - 0x400003FF	1 KB	TIM2
	0x40000400 - 0x400007FF	1 KB	TIM3
	0x40000800 - 0x400027FF	8 KB	Reserved
	0x40002800 - 0x40002BFF	1 KB	RTC_BKP
	0x40002C00 - 0x40002FFF	1 KB	Reserved

Bus	Address range	Size	Peripheral
	0x40003000 - 0x400033FF	1 KB	IWDG
	0x40003400 - 0x400037FF	1 KB	Reserved
	0x40003800 - 0x40003BFF	1 KB	SPI2
	0x40003C00 - 0x400043FF	2 KB	Reserved
	0x40004400 - 0x400047FF	1 KB	UART2
	0x40004800 - 0x40004BFF	1 KB	Reserved
	0x40004C00 - 0x40004FFF	1 KB	UART4
	0x40005000 - 0x400053FF	1 KB	Reserved
	0x40005400 - 0x400057FF	1 KB	I2C1
	0x40005800 - 0x40006BFF	5 KB	Reserved
	0x40006C00 - 0x40006FFF	1 KB	CRS
	0x40007000 - 0x400073FF	1 KB	PWR
	0x40007400 - 0x40009FFF	11 KB	Reserved
	0x4000A000 - 0x4000AFFF	4 KB	I3C1
	0x4000B000 - 0x4000BFFF	4 KB	Reserved
	0x4000C000 - 0x4000FFFF	16 KB	FlexCAN-FD
APB2	0x40010000 - 0x400103FF	1 KB	SYSCFG
	0x40010400 - 0x400107FF	1 KB	EXTI
	0x40010800 - 0x40010BFF	1 KB	LPUART1
	0x40010C00 - 0x400123FF	6 KB	Reserved
	0x40012400 - 0x400127FF	1 KB	ADC
	0x40012800 - 0x40012BFF	1 KB	LPTIM1
	0x40012C00 - 0x40012FFF	1 KB	TIM1
	0x40013000 - 0x400133FF	1 KB	SPI1
	0x40013400 - 0x400137FF	1 KB	DBGMCU
	0x40013800 - 0x40013BFF	1 KB	UART1
	0x40013C00 - 0x40013FFF	1 KB	COMP
	0x40014000 - 0x400143FF	1 KB	TIM14
	0x40014400 - 0x400147FF	1 KB	TIM16
	0x40014800 - 0x40014BFF	1 KB	TIM17
	0x40014C00 - 0x4001FFFF	45 KB	Reserved
AHB1	0x40020000 - 0x400203FF	1 KB	DMA
	0x40020400 - 0x40020FFF	3 KB	Reserved
	0x40021000 - 0x400213FF	1 KB	RCC
	0x40021400 - 0x40021FFF	3 KB	Reserved
	0x40022000 - 0x400223FF	1 KB	Flash Interface
	0x40022400 - 0x40022FFF	3 KB	Reserved
	0x40023000 - 0x400233FF	1 KB	CRC

Bus	Address range	Size	Peripheral
	0x40023400 - 0x4002FFFF	51 KB	Reserved
	0x40030000 - 0x400303FF	1 KB	HWDIV
	0x40030400 - 0x47FFFFFF	~128 MB	Reserved
	0x48000000 - 0x480003FF	1 KB	GPIOA
	0x48000400 - 0x480007FF	1 KB	GPIOB
	0x48000800 - 0x48000BFF	1 KB	GPIOC
	0x48000C00 - 0x48000FFF	1 KB	GPIOD
	0x48001000 - 0x4FFFFFFF	~128 MB	Reserved
AHB2	0x50000000 - 0x5003FFFF	256 KB	USB_FS

3.5 Flash

This product provides up to 128KB embedded Flash memory available for storing code and data.

3.6 SRAM

This product provides up to 16KB embedded SRAM.

3.7 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.8 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect a pulse width shorter than the internal APB2 clock period.

3.9 Clock and boot

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 96MHz.

3.10 Boot modes

During boot, BOOT0 pin and nBOOT1 bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.11 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 2.0V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.

3.12 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can

send out warning information or put the chip into safe mode. The PVD function can be configured to be enabled.

3.13 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that used by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.14 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their application to achieve a balance between power consumption, wakeup time and wakeup source.

Sleep mode

In sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

In stop mode, low power consumption can be achieved with all RAM and registers content in retention. In stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep Stop mode

Similar as stop mode, but with lower power consumption.

Standby mode

In standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the 1.5V domain are shut down. PLL, HSI and HSE are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin, IWDG reset. SRAM and registers content are lost in this mode. Only standby circuit are powered.

The peripheral status in each low-power mode is shown in Table 3-2, please note:

- Power Down indicates that the module is powered off and all data except Flash is lost.
- Optional indicates that the peripheral can be turned on or off through software configuration.
- ON means work.
- OFF indicates that the function is turned off.
- Retention indicates that data is retained but not operational.
- High-z represents a high-impedance state.

Table 3-2 Peripheral status in different power modes

Module/Mode	Run	Sleep	Stop	Deep Stop	Standby
Max. Freq.	96MHz	96MHz	40KHz	40KHz	40KHz
PVD	Optional	Optional	Optional	Optional	OFF
POR/BOR	ON	ON	ON	ON	ON
CPU	ON	OFF	OFF	OFF	Power Down
SRAM	ON	ON	Retention	Retention	Power Down
Flash	ON	Standby	Standby	Deep Standby	Power Down
HSI	Optional	Optional	OFF	Power Down	Power Down
PLL1	Optional	Optional	Power Down	Power Down	Power Down
PLL2	Optional	Optional	Power Down	Power Down	Power Down
LSI	Optional	Optional	Optional	Optional	Optional
HSE	Optional	Optional	OFF	OFF	OFF
ADC	Optional	Optional	OFF	OFF	OFF
COMP	Optional	Optional	Optional	Optional	OFF
IWDG	Optional	Optional	Optional	Optional	Optional
RTC	Optional	Optional	Optional	Optional	Optional
LSE	Optional	Optional	Optional	Optional	Optional
Backup registers	Optional	Optional	Optional	Optional	Optional
LPTIM/LPUART	Optional	Optional	Optional	Optional	Power Down
Other Peripherals	Optional	Optional	OFF	OFF	Power Down
I/O	Optional	Optional	Retention	Retention	High-z (1)

1. NRST maintains the reset function, wakeup I/O (WKUP) can wake up, RTC tamper detection pin (TAMP1) is operational, other I/Os are high impedance.

3.15 Hardware divider

This product has a hardware divider unit (HWDIV). It can automatically run the 32-bit signed or unsigned integer division operation. The HWDIV is especially useful in some high-performance applications.

3.16 DMA

This product has a 7-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be

triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

DMA can be used for peripherals include UART, LPUART, I2C, I3C, SPI, ADC, FlexCAN-FD, and general purpose, advanced, or basic timers.

3.17 Timers and watchdogs

This product has one advanced timer, two general purpose timers, three basic timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 3-3 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	up, down, up/down	1 to 65536	Yes	4	No
	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM14	16-bit	up	1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	up	1 to 65536	Yes	1	1
Low power	LPTIM1	16-bit	up	Any integer between 1 ~ 128	No	1 (Compare only)	No

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

In debug mode, the counter can be frozen.

General-purpose timer (TIMx)

This product has two general-purpose timers (TIM2, TIM3). The timer has a 16- or 32-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

32-bit general-purpose timer

This timer has a 32-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used as input capture, output compare, PWM or single pulse output.

16-bit general-purpose timer

This timer has a 16-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used for input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter can be frozen.

Basic timer (TIM14 / TIM16 / TIM17)

This product has three 16-bit basic timers (TIM14, TIM16, TIM17). Each timer has one 16-bit counter, supporting only up counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and one independent channel. Each channel can be used as input capture, output compare, PWM or one pulse mode output. When working in PWM mode, TIM14 has no complementary ports, TIM16 and TIM17 support complementary ports to generate complementary PWM pairs and support hardware dead time insertion function.

Low-power timer (LPTIM)

LPTIM consists of a 16-bit counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock running, it can work with external clock running and achieve external pulse counting in sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock,

it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.18 Real-time clock (RTC)

The real-time clock is an independent timer, which provides a set of continuously running counters. It can provide a real calendar function with corresponding software configuration. The current time and date of the system can be reset by modifying the value of the counter. The RTC module and clock configuration system (RCC_BDCR register) are in the backup area, namely, RTC setting and time remain unchanged after the system reset or the wake-up of the Standby mode.

3.19 Backup register

The backup register is composed of ten 16-bit registers that can be used to store user application data. These registers will not reset when the system is woken up in Standby mode, or when the system or power is reset.

3.20 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.21 UART

This product has up to four UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. These UART interfaces support up to 4.5 Mbps data rate. All UART interfaces support DMA operation.

3.22 LPUART

This product has one built-in low power UART interface (LPUART). Compared with UART, it has lower power consumption and supports running and waking up the chip in Stop and Deep Stop modes. The clock source can be selected between the HSI, LSI, LSE, and the peripheral clock.

3.23 I2C

This product has up to one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard mode (100 Kbps) and fast mode (400 Kbps). The I2C interface supports 7-bit or 10-bit addressing. All I2C interfaces support DMA operation.

3.24 I3C

This product has up to one I3C slave interface. The I3C interface is conformed to MIPI I3C Basic protocol v1.0, it's an upgrade to the I2C protocol in multiple ways and keep compatibility with I2C. This I3C interface supports up to 12.5 MHz clock rate. This I3C interface supports DMA operation.

3.25 SPI

This product has up to two SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 36 Mbps in master mode and 18 Mbps in slave mode. All SPI interfaces support DMA operation.

3.26 I2S

This product has up to two I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.27 FlexCAN-FD

This product has up to one FlexCAN-FD interface. The FlexCAN-FD interface is compatible with CAN 2.0A, 2.0B (active) and Flexible Data rate (CAN-FD) standard. Under CAN-FD mode, an independent PLL2 is integrated to provide clock source to the FlexCAN-FD module and enable up to 8 Mbps in FD mode. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

3.28 USB FS

This product has one USB controller compatible with USB 2.0 full-speed specification, provides up to 12 Mbps data rate, support Device mode. This USB controller provides up to eight endpoints. This product has built-in USB PHY.

3.29 ADC

This product has one 12-bit analog/digital converter (ADC), with up to 14 external channels available, supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.30 COMP

This product has two build-in analog comparators (COMP), which can be used independently (applicable to all I/O ports that have comparator function) or combined with timers. Each comparator can select the voltage reference from the external I/O ports or the internal voltage reference (CRV) output, where the CRV output is derived from a 4-bit resistance divider ladder of the V_{DDA} or internal bandgap voltage. The COMP module can be used for a variety of functions including low-power mode wake-up event triggered by analog input, fast PWM output break when over-current detected, events capture and OCref-clr events used for cycle-by-cycle current control. The COMP module supports programmable hysteresis voltage, programmable rate, and power consumption.

3.31 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.32 SWD

This product equips Arm standard Serial Wire Debug (SWD).

4 Pinout and assignment

4.1 Pinout diagram

4.1.1 LQFP64 pinout

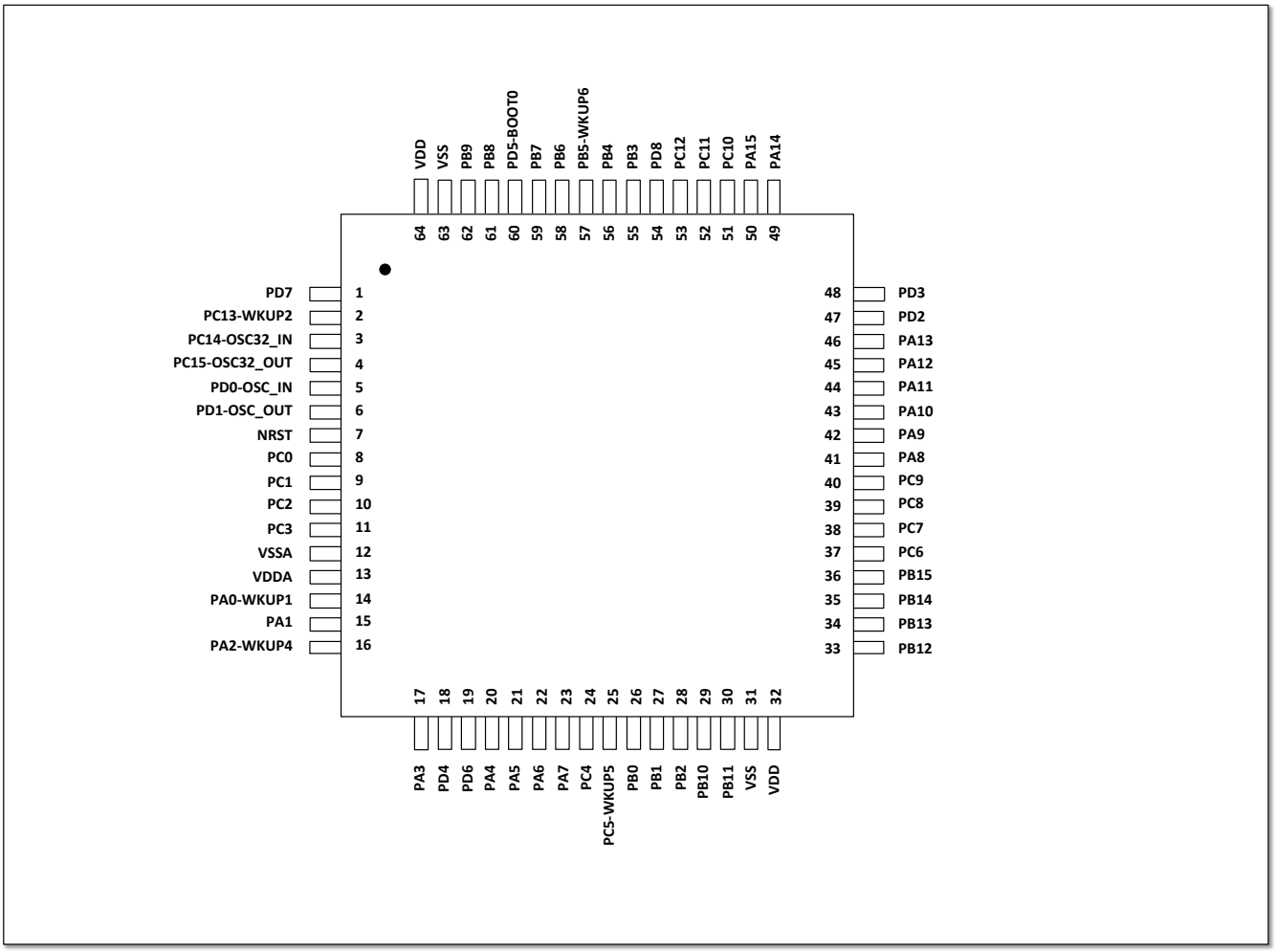

Figure 4-1 LQFP64 pinout diagram

4.1.2 LQFP48 pinout

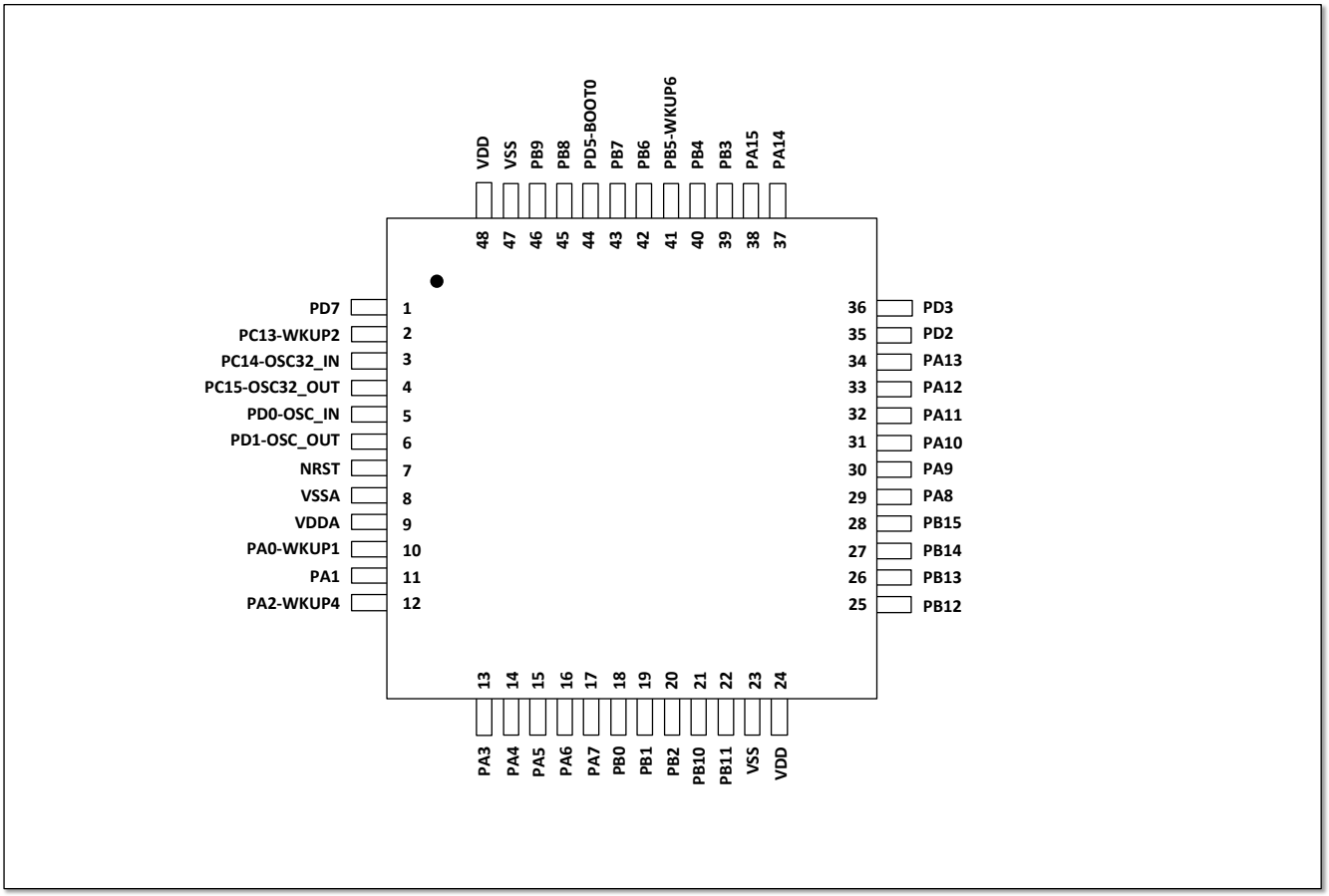

Figure 4-2 LQFP48 pinout diagram

4.1.3 LQFP44 pinout

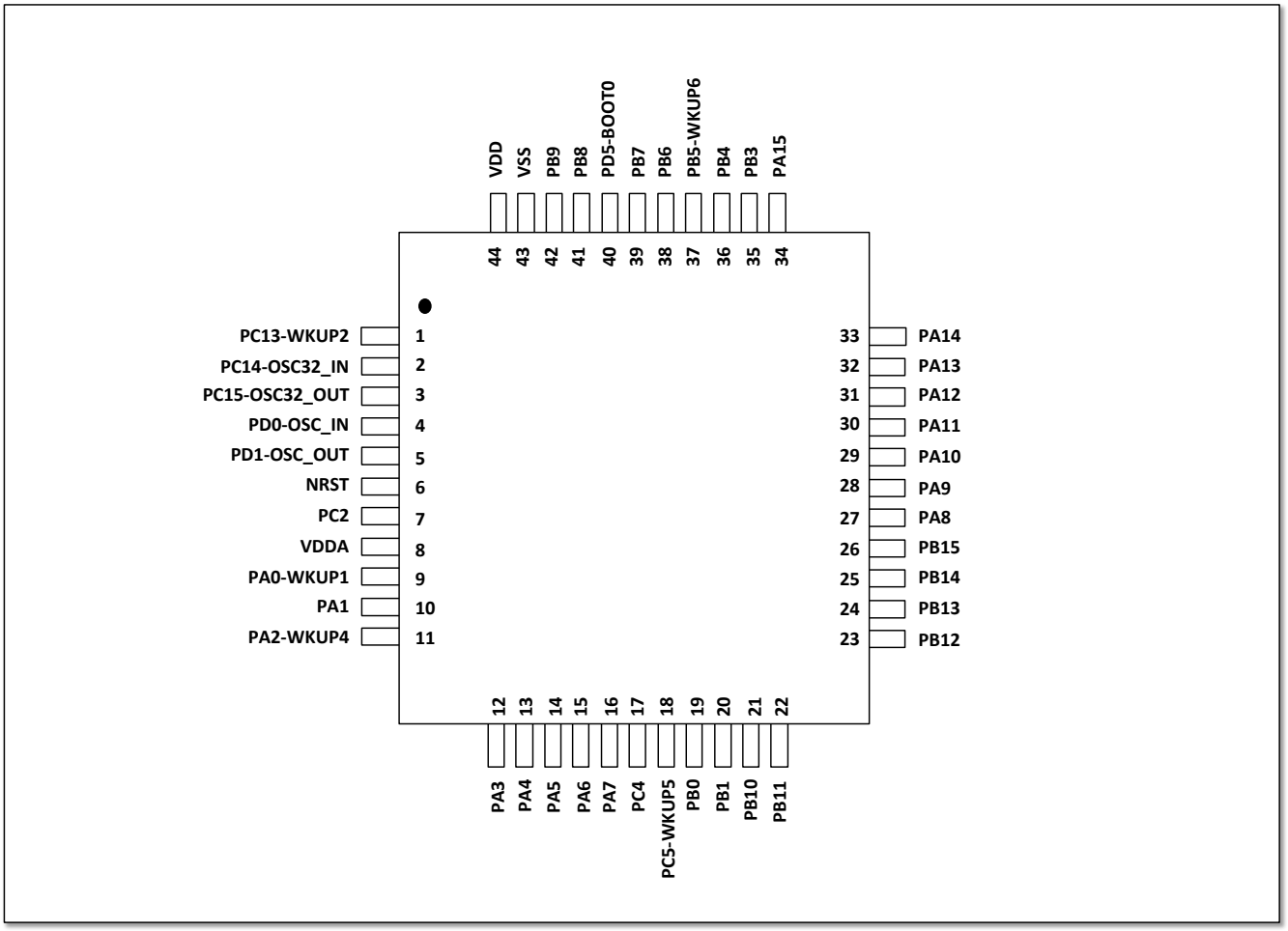

Figure 4-3 LQFP44 pinout diagram

4.1.4 QFN32 pinout

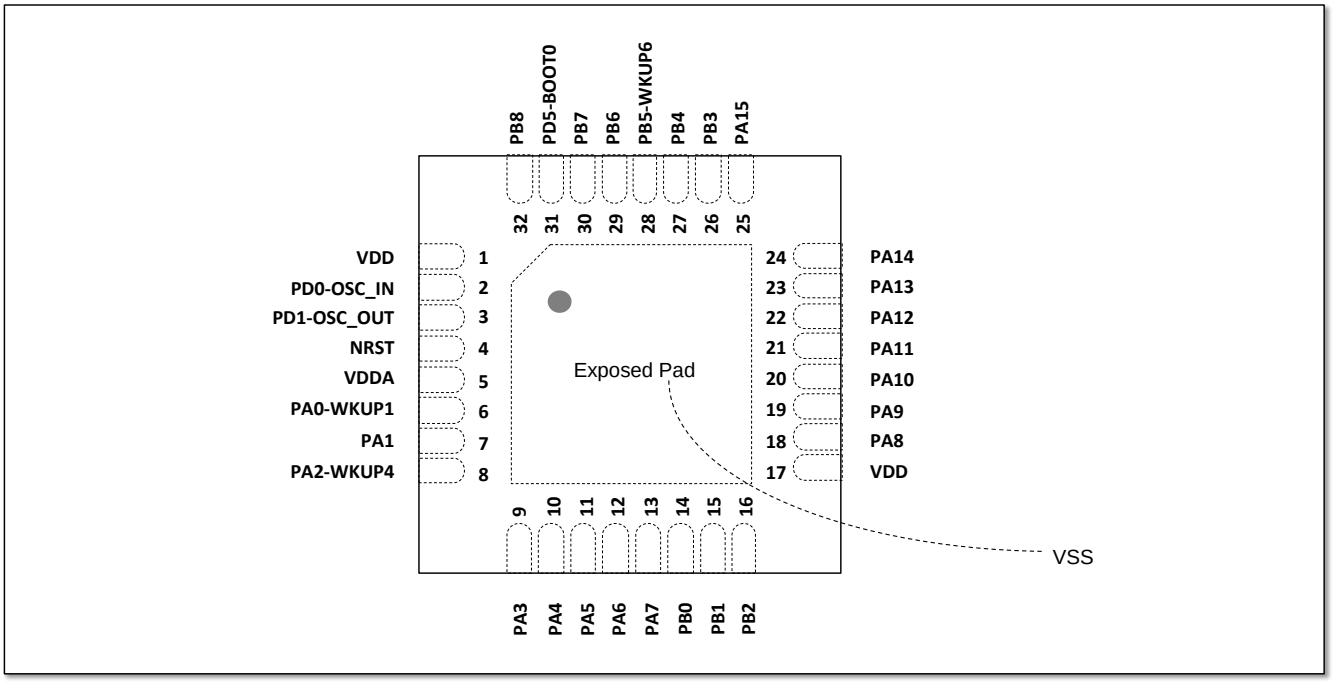

Figure 4-4 QFN32 pinout diagram

4.1.5 QFN28 pinout

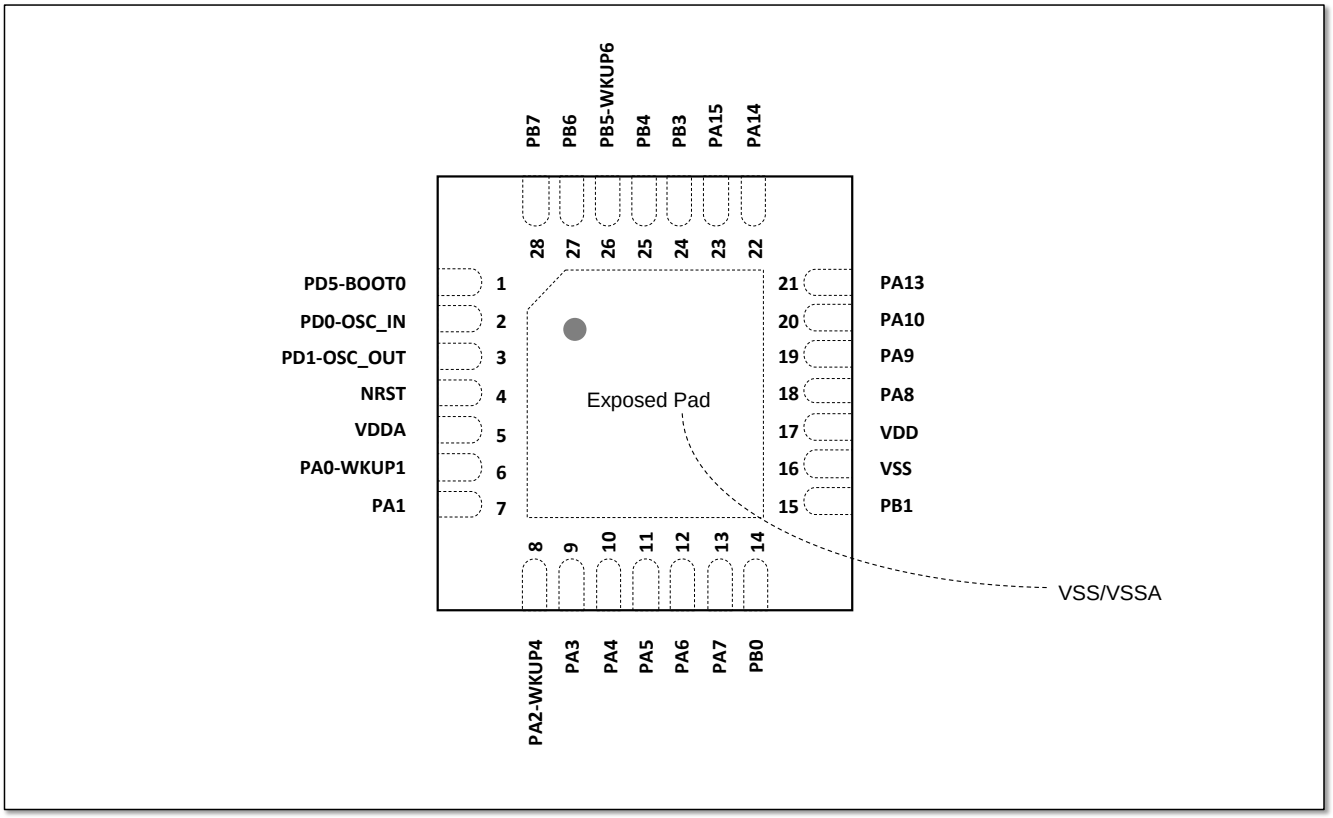

Figure 4-5 QFN28 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

LQFP64	LQFP48	LQFP44	QFN32	QFN28	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
1	1	-	-	-	PD7	I/O	TC	PD7	TIM2_CH4 TIM17_CH1	-
2	2	1	-	-	PC13 WKUP2	I/O	TC	PC13	TIM2_CH1	TAMP1
3	3	2	-	-	PC14 OSC32_IN	I/O	TC	PC14	TIM2_CH2	-
4	4	3	-	-	PC15 OSC32_OUT	I/O	TC	PC15	TIM2_CH3	-
5	5	4	2	2	PD0 OSC_IN	I/O	TC	PD0	UART3_TX I2C1_SDA CRS_SYNC	-
6	6	5	3	3	PD1 OSC_OUT	I/O	TC	PD1	UART3_RX I2C1_SCL	-
7	7	6	4	4	NRST	I/O	TC	NRST	-	-
8	-	-	-	-	PC0	I/O	TC	PC0	LPUART1_TX	-
9	-	-	-	-	PC1	I/O	TC	PC1	LPUART1_RX	-
10	-	7	-	-	PC2	I/O	TC	PC2	SPI2_MISO/I2S2_MCK LPTIM1_TRIG	-
11	-	-	-	-	PC3	I/O	TC	PC3	SPI2_MOSI/I2S2_SD LPTIM1_OUT	ADC1_VIN[13]
12	8	-	-	-	VSSA	S	-	VSSA	-	-
13	9	8	5	5	VDDA	S	-	VDDA	-	-
14	10	9	6	6	PA0 WKUP1	I/O	TC	PA0	UART2_CTS TIM2_CH1/TIM2_ETR SPI2_NSS/I2S2_WS TIM2_CH3 UART4_TX COMP1_OUT	ADC1_VIN[0] COMP2_INP[0]/COMP1_INM[3]
15	11	10	7	7	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2 UART4_RX	ADC1_VIN[1] COMP1_INP[0]/COMP2_INP[1]
16	12	11	8	8	PA2 WKUP4	I/O	TC	PA2	UART2_TX TIM2_CH3 SPI2_NSS/I2S2_WS I3C1_SCL COMP2_OUT	ADC1_VIN[2] COMP1_INP[1]/COMP2_INP[2]/COMP2_INM[3]
17	13	12	9	9	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4 I3C1_SDA	ADC1_VIN[3] COMP1_INP[2]/COMP2_INP[3]
18	-	-	-	-	PD4	I/O	TC	PD4	SPI1_MISO/I2S1_MCK	-
19	-	-	-	-	PD6	I/O	TC	PD6	SPI1_MOSI/I2S1_SD	-
20	14	13	10	10	PA4	I/O	TC	PA4	SPI1_NSS/I2S1_WS LPUART1_TX TIM1_BKIN TIM14_CH1 I2C1_SDA	ADC1_VIN[4] COMP1_INP[3]/COMP2_INM[0]

LQFP64	LQFP48	LQFP44	QFN32	QFN28	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
21	15	14	11	11	PA5	I/O	TC	PA5	SPI1_SCK/I2S1_CK LPUART1_RX TIM2_CH1/ TIM2_ETR TIM1_ETR I2C1_SCL TIM1_CH3N	ADC1_VIN[5] COMP1_INM[0]/COMP2_INM[1]
22	16	15	12	12	PA6	I/O	TC	PA6	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM1_BKIN UART2_RX TIM1_ETR TIM16_CH1 TIM1_CH3 COMP1_OUT COMP1_OUT	ADC1_VIN[6] COMP1_INM[1]/COMP2_INM[2]
23	17	16	13	13	PA7	I/O	TC	PA7	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM1_CH1N TIM14_CH1 TIM17_CH1 TIM1_CH2N TIM1_CH3N COMP2_OUT	ADC1_VIN[7] COMP1_INM[2]
24	-	17	-	-	PC4	I/O	TC	PC4	UART3_TX TIM3_CH1 SPI1_MOSI/I2S1_SD	-
25	-	18	-	-	PC5 WKUP5	I/O	TC	PC5	UART3_RX TIM3_CH2 SPI1_MISO/I2S1_MCK	-
26	18	19	14	14	PB0	I/O	TC	PB0	TIM3_CH3 TIM1_CH2N TIM1_CH1N TIM1_CH3	ADC1_VIN[8]
27	19	20	15	15	PB1	I/O	TC	PB1	TIM14_CH1 TIM3_CH4 TIM1_CH3N TIM1_CH4 TIM1_CH2N MCO TIM1_CH2 TIM1_CH1N UART3_RTS	ADC1_VIN[9]
28	20	-	16	-	PB2	I/O	TC	PB2	-	-
29	21	21	-	-	PB10	I/O	TC	PB10	I3C1_SCL I2C1_SCL TIM2_CH3 UART3_TX SPI2_SCK/I2S2_CK	-
30	22	22	-	-	PB11	I/O	TC	PB11	I3C1_SDA I2C1_SDA TIM2_CH4 UART3_RX	-
31	23	-	-	16	VSS	S	-	VSS	-	-
32	24	-	17	17	VDD	S	-	VDD	-	-

LQFP64	LQFP48	LQFP44	QFN32	QFN28	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
33	25	23	-	-	PB12	I/O	TC	PB12	SPI2_NSS/I2S2_WS SPI2_SCK/I2S2_CK TIM1_BKIN SPI2_MOSI/I2S2_SD SPI2_MISO/I2S2_MCK I3C1_SCL LPTIM1_TRIG	-
34	26	24	-	-	PB13	I/O	TC	PB13	SPI2_SCK/I2S2_CK SPI2_MISO/I2S2_MCK TIM1_CH1N SPI2_NSS/I2S2_WS SPI2_MOSI/I2S2_SD I2C1_SCL TIM1_CH3N TIM2_CH1 UART3_CTS	-
35	27	25	-	-	PB14	I/O	TC	PB14	SPI2_MISO/I2S2_MCK SPI2_MOSI/I2S2_SD TIM1_CH2N SPI2_SCK/I2S2_CK SPI2_NSS/I2S2_WS I2C1_SDA TIM1_CH3 TIM1_CH1 UART3_RTS	-
36	28	26	-	-	PB15	I/O	TC	PB15	SPI2_MOSI/I2S2_SD SPI2_NSS/I2S2_WS TIM1_CH3N SPI2_MISO/I2S2_MCK SPI2_SCK/I2S2_CK I3C1_SDA TIM1_CH2N TIM1_CH2 LPTIM1_OUT	-
37	-	-	-	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM2_CH4 SPI1_NSS/I2S1_WS	-
38	-	-	-	-	PC7	I/O	TC	PC7	TIM3_CH2 TIM2_CH3 SPI1_SCK/I2S1_CK	-
39	-	-	-	-	PC8	I/O	TC	PC8	TIM3_CH3 TIM2_CH2	-
40	-	-	-	-	PC9	I/O	TC	PC9	TIM3_CH4 TIM2_CH1/ TIM2_ETR	-

LQFP64	LQFP48	LQFP44	QFN32	QFN28	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
41	29	27	18	18	PA8	I/O	TC	PA8	MCO TIM1_CH1 TIM1_CH2 TIM1_CH3 CRS_SYNC	-
42	30	28	19	19	PA9	I/O	TC	PA9	UART1_TX TIM1_CH2 UART1_RX I2C1_SCL MCO TIM1_CH1N TIM1_CH4 CAN_RX	-
43	31	29	20	20	PA10	I/O	TC	PA10	TIM17_BKIN UART1_RX TIM1_CH3 UART1_TX I2C1_SDA TIM1_CH1 SPI2_SCK/I2S2_CK CAN_TX	-
44	32	30	21	-	PA11	I/O	TC	PA11	UART3_TX UART1_CTS TIM1_CH4 CAN_RX SPI2_MOSI/I2S2_SD I2C1_SCL COMP1_OUT	USBDM
45	33	31	22	-	PA12	I/O	TC	PA12	UART3_RX UART1_RTS TIM1_ETR CAN_TX SPI2_MISO/I2S2_MCK I2C1_SDA TIM1_CH2 COMP2_OUT	USBDP
46	34	32	23	21	PA13	I/O	TC	PA13	SWDIO UART1_TX SPI2_MISO/I2S2_MCK MCO TIM1_CH2 TIM1_BKIN	-
47	35	-	-	-	PD2	I/O	TC	PD2	I3C1_SCL	-
48	36	-	-	-	PD3	I/O	TC	PD3	I3C1_SDA	-
49	37	33	24	22	PA14	I/O	TC	PA14	SWDCLK UART2_TX UART1_RX SPI1_NSS/I2S1_WS	-
50	38	34	25	23	PA15	I/O	TC	PA15	SPI1_NSS/I2S1_WS UART2_RX TIM2_CH1/ TIM2_ETR UART4_RTS	-
51	-	-	-	-	PC10	I/O	TC	PC10	UART4_TX UART3_TX	-
52	-	-	-	-	PC11	I/O	TC	PC11	UART4_RX UART3_RX	-

LQFP64	LQFP48	LQFP44	QFN32	QFN28	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
53	-	-	-	-	PC12	I/O	TC	PC12	-	-
54	-	-	-	-	PD8	I/O	TC	PD8	TIM3_ETR UART3_RTS	-
55	39	35	26	24	PB3	I/O	TC	PB3	SPI1_SCK/I2S1_CK TIM2_CH2 UART1_TX TIM2_CH3 TIM1_CH1 TIM2_CH1	ADC1_VIN[10]
56	40	36	27	25	PB4	I/O	TC	PB4	SPI1_MISO/I2S1_MCK TIM3_CH1 UART1_RX TIM17_BKIN TIM1_CH2 TIM2_CH2	ADC1_VIN[11]
57	41	37	28	26	PB5 WKUP6	I/O	TC	PB5	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM16_BKIN MCO TIM1_CH3 TIM2_CH3	-
58	42	38	29	27	PB6	I/O	TC	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM2_CH1	-
59	43	39	30	28	PB7	I/O	TC	PB7	UART1_RX I2C1_SDA TIM17_CH1N UART2_TX UART4_CTS	ADC1_VIN[12]
60	44	40	31	1	PD5 BOOT0	I/O	TC	PD5	-	-
61	45	41	32	-	PB8	I/O	TC	PB8	I2C1_SCL TIM16_CH1 CAN_RX UART2_RX	-
62	46	42	-	-	PB9	I/O	TC	PB9	I2C1_SDA TIM17_CH1 CAN_TX TIM1_CH4 SPI2_NSS/I2S2_WS	-
63	47	43	-	-	VSS	S	-	VSS	-	-
64	48	44	1	-	VDD	S	-	VDD	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.

4.3 Pin multiplexing

Table 4-2 PA port multiplexing AF0-AF8

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PA0	-	UART2_CTS	TIM2_CH1/TIM2_ETR	SPI2_NSS/I2S2_WS	TIM2_CH3	UART4_TX	-	COMP1_OUT	-
PA1	-	UART2_RTS	TIM2_CH2	-	-	UART4_RX	-	-	-
PA2	-	UART2_TX	TIM2_CH3	SPI2_NSS/I2S2_WS	-	I3C1_SCL	-	COMP2_OUT	-
PA3	-	UART2_RX	TIM2_CH4	-	-	I3C1_SDA	-	-	-
PA4	SPI1_NSS/I2S1_WS	LPUART1_TX	-	TIM1_BKIN	TIM14_CH1	I2C1_SDA	-	-	-
PA5	SPI1_SCK/I2S1_CK	LPUART1_RX	TIM2_CH1/TIM2_ETR	TIM1_ETR	-	I2C1_SCL	TIM1_CH3N	-	-
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT	COMP1_OUT
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	TIM1_CH2N	TIM1_CH3N	COMP2_OUT
PA8	MCO	-	TIM1_CH1	-	-	-	TIM1_CH2	TIM1_CH3	CRS_SYNC
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	TIM1_CH4	CAN_RX
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	TIM1_CH1	SPI2_SCK/I2S2_CK	CAN_TX
PA11	UART3_TX	UART1_CTS	TIM1_CH4	CAN_RX	SPI2_MOSI/I2S2_SD	I2C1_SCL	-	COMP1_OUT	-
PA12	UART3_RX	UART1_RTS	TIM1_ETR	CAN_TX	SPI2_MISO/I2S2_MCK	I2C1_SDA	-	TIM1_CH2	COMP2_OUT
PA13	SWDIO	-	UART1_TX	-	SPI2_MISO/I2S2_MCK	MCO	TIM1_CH2	TIM1_BKIN	-
PA14	SWDCLK	UART2_TX	UART1_RX	SPI1_NSS/I2S1_WS	-	-	-	-	-
PA15	SPI1_NSS/I2S1_WS	UART2_RX	TIM2_CH1/TIM2_ETR	-	-	UART4_RTS	-	-	-

Table 4-3 PB port multiplexing AF0-AF8

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N	UART3_RTS
PB2	-	-	-	-	-	-	-	-	-
PB3	SPI1_SCK/I2S1_CK	-	TIM2_CH2	UART1_TX	TIM2_CH3	-	TIM1_CH1	TIM2_CH1	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	UART1_RX	-	TIM17_BKIN	TIM1_CH2	TIM2_CH2	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	MCO	-	-	TIM1_CH3	TIM2_CH3	-
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM2_CH1	-	-	-	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	UART2_TX	UART4_CTS	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	CAN_RX	UART2_RX	-	-	-	-
PB9	-	I2C1_SDA	TIM17_CH1	CAN_TX	TIM1_CH4	SPI2_NSS/I2S2_WS	-	-	-
PB10	I3C1_SCL	I2C1_SCL	TIM2_CH3	-	UART3_TX	SPI2_SCK/I2S2_CK	-	-	-
PB11	I3C1_SDA	I2C1_SDA	TIM2_CH4	-	UART3_RX	-	-	-	-
PB12	SPI2_NSS/I2S2_WS	SPI2_SCK/I2S2_CK	TIM1_BKIN	SPI2_MOSI/I2S2_SD	SPI2_MISO/I2S2_MCK	I3C1_SCL	-	-	LPTIM1_TRIG
PB13	SPI2_SCK/I2S2_CK	SPI2_MISO/I2S2_MCK	TIM1_CH1N	SPI2_NSS/I2S2_WS	SPI2_MOSI/I2S2_SD	I2C1_SCL	TIM1_CH3N	TIM2_CH1	UART3_CTS
PB14	SPI2_MISO/I2S2_MCK	SPI2_MOSI/I2S2_SD	TIM1_CH2N	SPI2_SCK/I2S2_CK	SPI2_NSS/I2S2_WS	I2C1_SDA	TIM1_CH3	TIM1_CH1	UART3_RTS
PB15	SPI2_MOSI/I2S2_SD	SPI2_NSS/I2S2_WS	TIM1_CH3N	SPI2_MISO/I2S2_MCK	SPI2_SCK/I2S2_CK	I3C1_SDA	TIM1_CH2N	TIM1_CH2	LPTIM1_OUT

Table 4-4 PC port multiplexing AF0-AF8

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PC0	-	-	LPUART1_TX	-	-	-	-	-	-
PC1	-	-	LPUART1_RX	-	-	-	-	-	-
PC2	-	SPI2_MISO/ I2S2_MCK	-	LPTIM1_TRIG	-	-	-	-	-
PC3	-	SPI2_MOSI/ I2S2_SD	-	LPTIM1_OUT	-	-	-	-	-
PC4	-	UART3_TX	-	-	-	TIM3_CH1	SPI1_MOSI/ I2S1_SD	-	-
PC5	-	UART3_RX	-	-	-	TIM3_CH2	SPI1_MISO/ I2S1_MCK	-	-
PC6	TIM3_CH1	-	-	TIM2_CH4	-	-	SPI1_NSS/I 2S1_WS	-	-
PC7	TIM3_CH2	-	-	TIM2_CH3	-	-	SPI1_SCK/I 2S1_CK	-	-
PC8	TIM3_CH3	-	-	TIM2_CH2	-	-	-	-	-
PC9	TIM3_CH4	-	-	TIM2_CH1/ TIM2_ETR	-	-	-	-	-
PC10	UART4_TX	UART3_TX	-	-	-	-	-	-	-
PC11	UART4_RX	UART3_RX	-	-	-	-	-	-	-
PC12	-	-	-	-	-	-	-	-	-
PC13	-	-	-	-	-	-	TIM2_CH1	-	-
PC14	-	-	-	-	-	-	TIM2_CH2	-	-
PC15	-	-	-	-	-	-	TIM2_CH3	-	-

Table 4-5 PD port multiplexing AF0-AF8

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PD0	UART3_TX	I2C1_SDA	CRS_SYNC	-	-	-	-	-	-
PD1	UART3_RX	I2C1_SCL	-	-	-	-	-	-	-
PD2	-	I3C1_SCL	-	-	-	-	-	-	-
PD3	-	I3C1_SDA	-	-	-	-	-	-	-
PD4	SPI1_MISO/ I2S1_MCK	-	-	-	-	-	-	-	-
PD5	-	-	-	-	-	-	-	-	-
PD6	SPI1_MOSI/ I2S1_SD	-	-	-	-	-	-	-	-
PD7	-	-	-	-	-	-	TIM2_CH4	TIM17_CH1	-
PD8	TIM3_ETR	UART3_RTS	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

5.1.1 Load capacitor

The load conditions for pin parameters measurement are shown in the Figure 5-1.

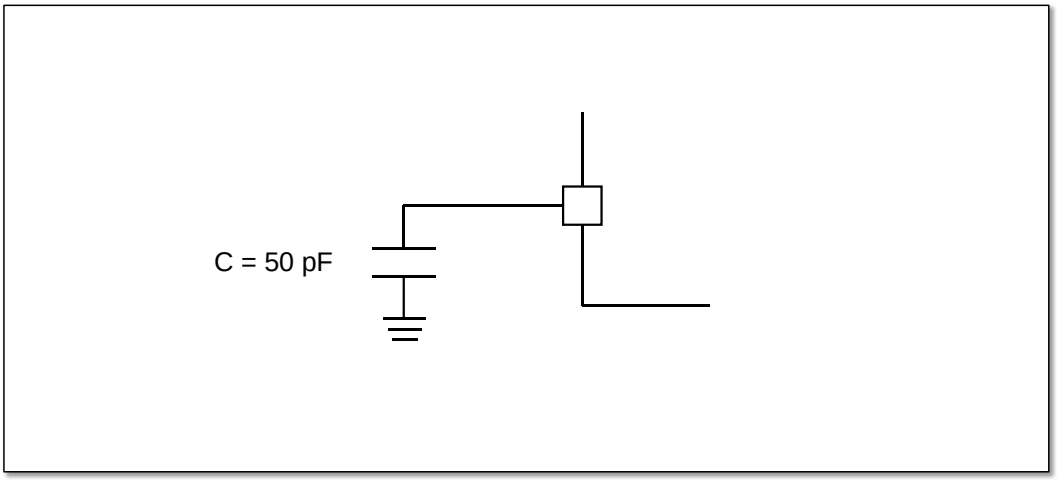

Figure 5-1 Load condition of the pin

5.1.2 Pin input voltage

The measurement of the input voltage on the pin is shown in Figure 5-2.

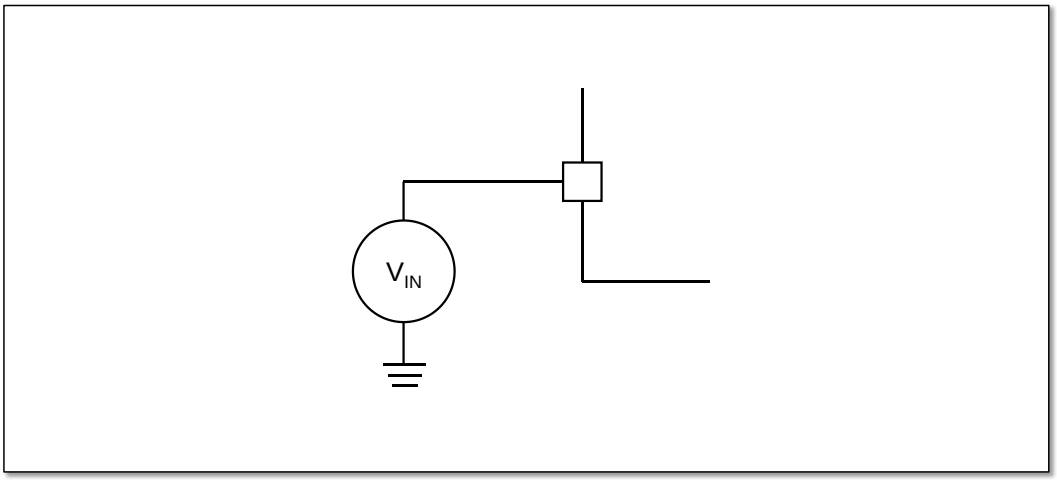

Figure 5-2 Pin input voltage

5.1.3 Power scheme

The power supply design scheme is shown in Figure 5-3.

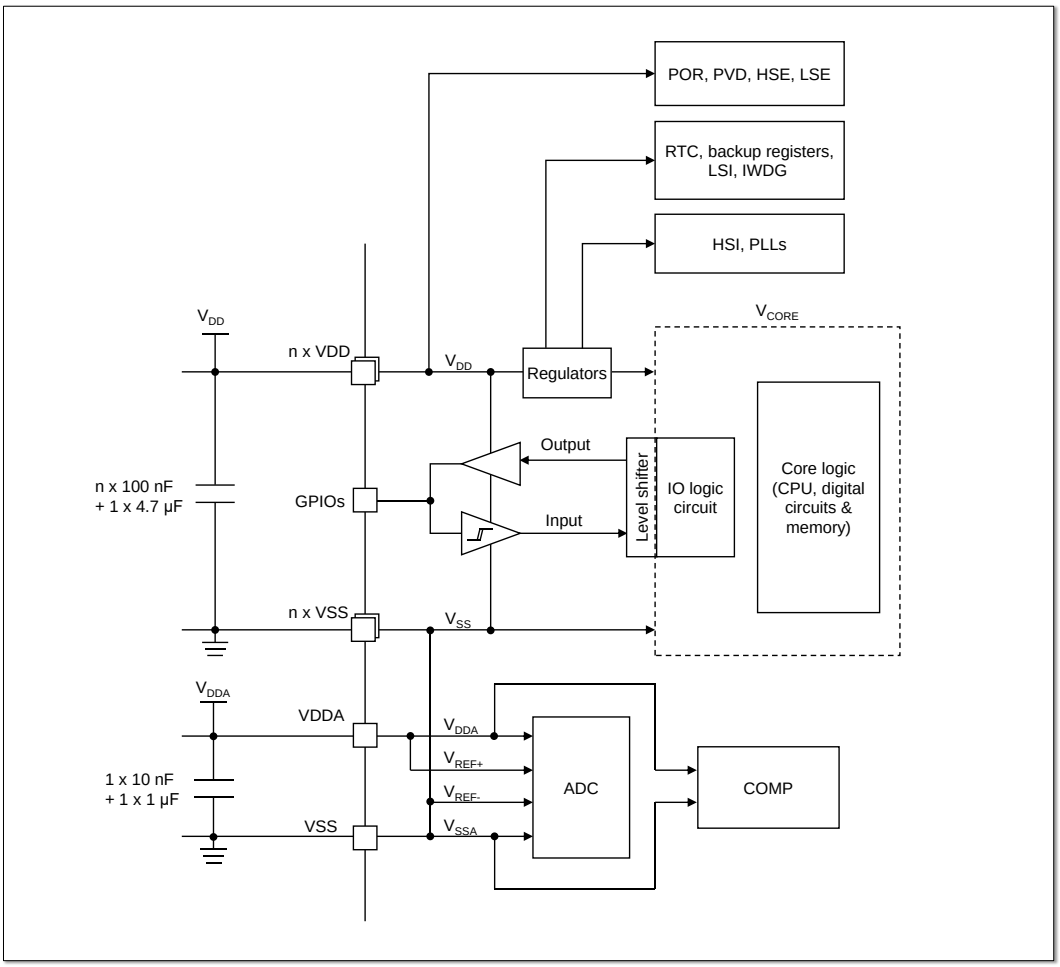

Figure 5-3 Power scheme

5.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 5-4.

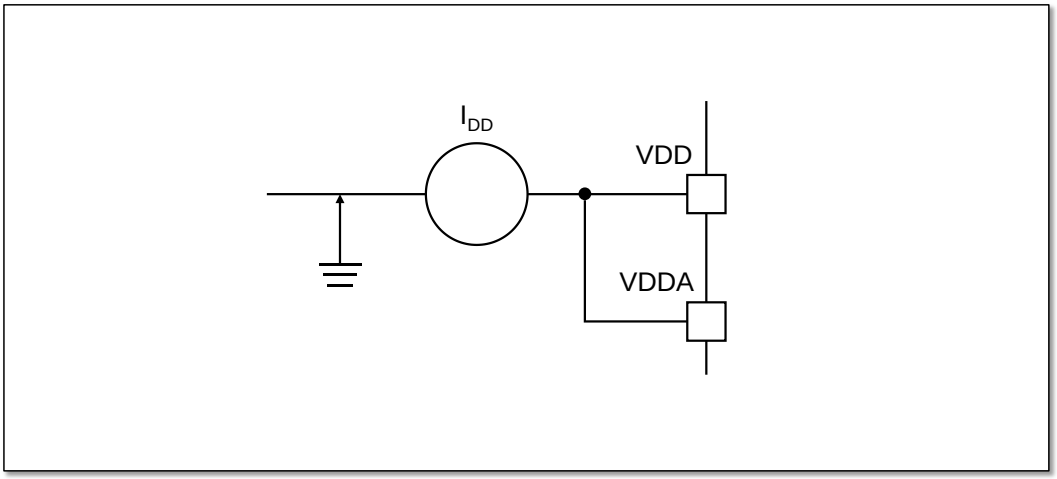

Figure 5-4 Current consumption measurement scheme

5.2 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 5-1, Table 5-2 and Table 5-3) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA}) (1)	-0.3	5.8	V
V_{IN} (2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply system within the permitted range.
2. The maximum value of V_{IN} must be respected. Refer to the table below for the maximum allowed injected current values.

Table 5-2 Current characteristics

Symbol	Description	Maximum	Unit
$I_{VDD/VDDA}$ (1)	Total current through V_{DD}/V_{DDA} power pins (supply current) (1)	+120	mA
$I_{VSS/VSSA}$ (1)	Total current through V_{SS}/V_{SSA} ground pins (outflow current) (1)	-120	
I_{IO}	Output sink current on any I/O and control pins	+25	
	Output current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (5)	Other pins injection current (4)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an

external power supply in the permitted range.

2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP package.
3. The reverse injection current can interfere with the analog performance of the device.
4. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

5.3 Operating conditions

5.3.1 General operating conditions

Table 5-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	96	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	-	-	96	
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	96	
V_{DD}	Digital circuit operating voltage	-	2.0	3.3	5.5	V
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD} (1)	2.5	3.3	5.5	
	Analog circuit operating voltage (Performance is not guaranteed)		2.0	-	2.5	
P_D	Power dissipation Temperature: T_A = 85°C (2) or: T_A = 105°C (2)	LQFP64	-	-	339	mW
		LQFP48	-	-	357	
		QFN32	-	-	571	
T_A	Ambient temperature (industrial level)	-	-40	-	85	°C
	Ambient temperature (extended industrial level)	-	-40	-	105	°C
T_J	Junction temperature (3) (industrial level)	-	-40	-	105	°C
	Junction temperature (3) (extended industrial level)	-	-40	-	125	°C

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mVduring power up and normal operation.
2. If T_A is low, higher P_D values are allowed as long as T_J (T_J=125°C is the absolute maximum rating value) does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range as long as T_J (T_J=125°C is the absolute maximum rating value) does not exceed T_{Jmax}.

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-4 Operating conditions at power-up/power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time t_r	1	-	∞	us
	V_{DD} fall time t_f	400	-	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

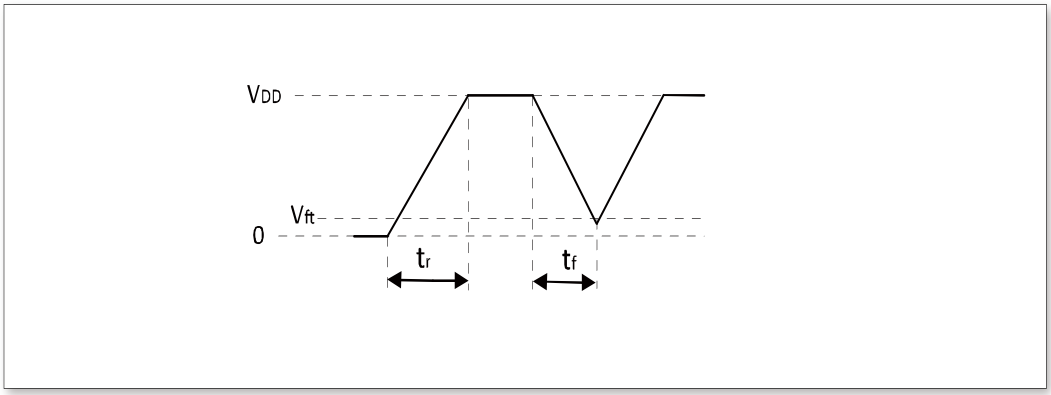

Figure 5-5 Power-on and power-down waveforms

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-5 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	
		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{POR/PDR}$ (1)	Power-on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	30	-	mV
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	2.7	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction

5.3.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-6 Build-in voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	-40°C < T_A < 105°C	-	1.2	-	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	-	-	11.8	-	us

1. The sampling time is obtained through multiple tests

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating

frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle, 48 ~ 72 MHz is 2 waiting cycles, 72 ~ 96 MHz is 3 waiting cycles).
- The instruction prefetching function is on. When the peripherals are enabled: $f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-7 Typical current consumption in Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Supply current in Run mode	Internal clock source	96M	19.02	19.43	19.67	19.76	10.81	11.17	11.37	11.46	mA
			72M	15.59	15.87	16.12	16.22	9.42	9.66	9.88	9.98	
			48M	11.91	12.14	12.35	12.44	7.78	8.01	8.21	8.29	
			24M	7.34	7.46	7.59	7.66	5.28	5.38	5.52	5.57	
			8M	2.40	2.45	2.52	2.56	1.79	1.84	1.91	1.95	
			4M	1.59	1.62	1.67	1.70	1.25	1.29	1.33	1.36	
			2M	0.95	0.98	1.01	1.03	0.79	0.81	0.84	0.87	
			1M	0.65	0.67	0.69	0.71	0.57	0.58	0.61	0.63	
			500K	0.50	0.51	0.54	0.56	0.46	0.47	0.50	0.52	
			125K	0.39	0.40	0.42	0.44	0.38	0.39	0.41	0.43	

Table 5-8 Typical current consumption in Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Supply current in Sleep mode	Internal clock source	96M	12.77	12.86	12.89	12.89	4.54	4.56	4.56	4.57	mA
			72M	9.80	9.86	9.89	9.89	3.63	3.64	3.64	3.64	
			48M	6.83	6.87	6.89	6.89	2.71	2.72	2.72	2.72	

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
			24M	3.86	3.87	3.88	3.88	1.79	1.80	1.79	1.79	
			4M	1.17	1.18	1.21	1.23	0.56	0.57	0.59	0.61	
			2M	0.79	0.80	0.83	0.84	0.46	0.47	0.49	0.50	
			1M	0.57	0.58	0.60	0.62	0.40	0.41	0.43	0.45	
			500K	0.45	0.46	0.49	0.50	0.37	0.38	0.40	0.42	
			125K	0.40	0.41	0.43	0.45	0.36	0.37	0.39	0.40	

Table 5-9 Typical and maximum current consumption in stop and Standby modes (1)

Symbol	Parameter	Conditions	Typical	Unit
			25℃	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	105.5	μA
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	1.63	
	Supply current in Standby mode	LSI, LSE, RTC, IWDG all disabled	0.38	
		LSI and IWDG enabled	0.62	
		LSE and RTC enabled	1.46	

1. The I/O state is an analog input.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 5-3.

Table 5-10 On-chip peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	1.07	uA/MHz
	GPIOA		0.68	
	GPIOB		0.74	
	GPIOC		0.66	

Symbol	Parameter	Bus	Typical	Unit
	GPIOD		0.68	
	DMA		1.84	
	HWDIV		0.96	
	USB		7.13	
	TIM1	APB2	7.33	
	TIM14		1.87	
	TIM16		2.25	
	TIM17		2.34	
	LPTIM1		0.43	
	SPI1		4.56	
	UART1		4.13	
	LPUART1		0.46	
	SYSCFG		0.50	
	MCUDBG		0.08	
	COMP		0.79	
	EXTI		0.01	
	ADC		3.49	
	TIM2	APB1	4.19	
	TIM3		3.22	
	RTC		0.82	
	BKP		0.01	
	UART2		4.10	
	UART3		4.08	
	UART4		4.09	
	CRS		0.40	
	SPI2		4.48	
	I2C1		4.66	
	I3C1		2.12	
	IWDG		0.01	
	WWDG		0.24	
	FlexCAN		12.91	

1. f_{HCLK} = 96MHz，f_{APB1} = f_{HCLK}，f_{APB2} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

- Stop or Standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-11 Wake up time from low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSI	3	cycles
t_{WUSTOP}	Wake up from Stop mode (regulator is in Run mode)	System clock is HSI	9.6	μs
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode (regulator is in low power mode)	System clock is HSI	5.2	μs
$t_{WUSTDBY}$	Wake up from Standby mode	System clock is HSI	534.5	μs

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

Table 5-12 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency (1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	15	-	-	ns

1. Guaranteed by design, not tested in production

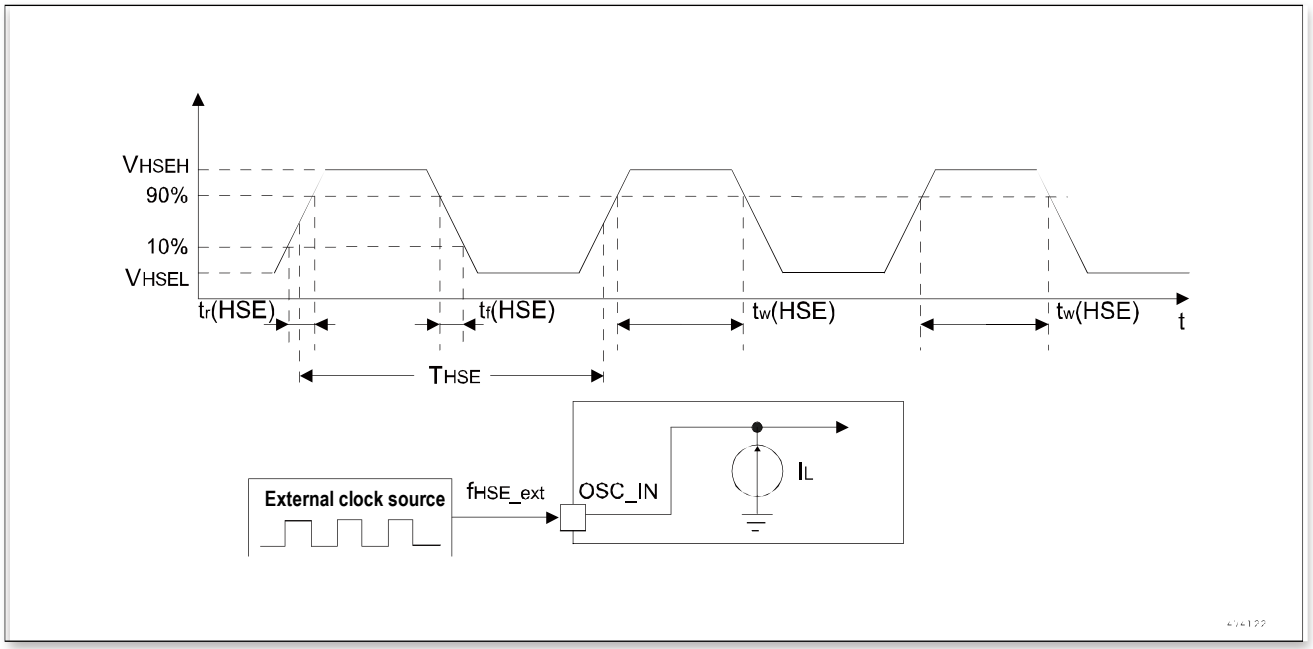

Figure 5-6 High-speed external clock source AC timing diagram

Low-speed external user clock generated from external oscillator source

The parameters of characteristics given in the following table are measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 5-13 Low-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User external clock frequency (1)	-	-	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time (1)	-	250	-	-	ns

1. Guaranteed by design, not tested in production

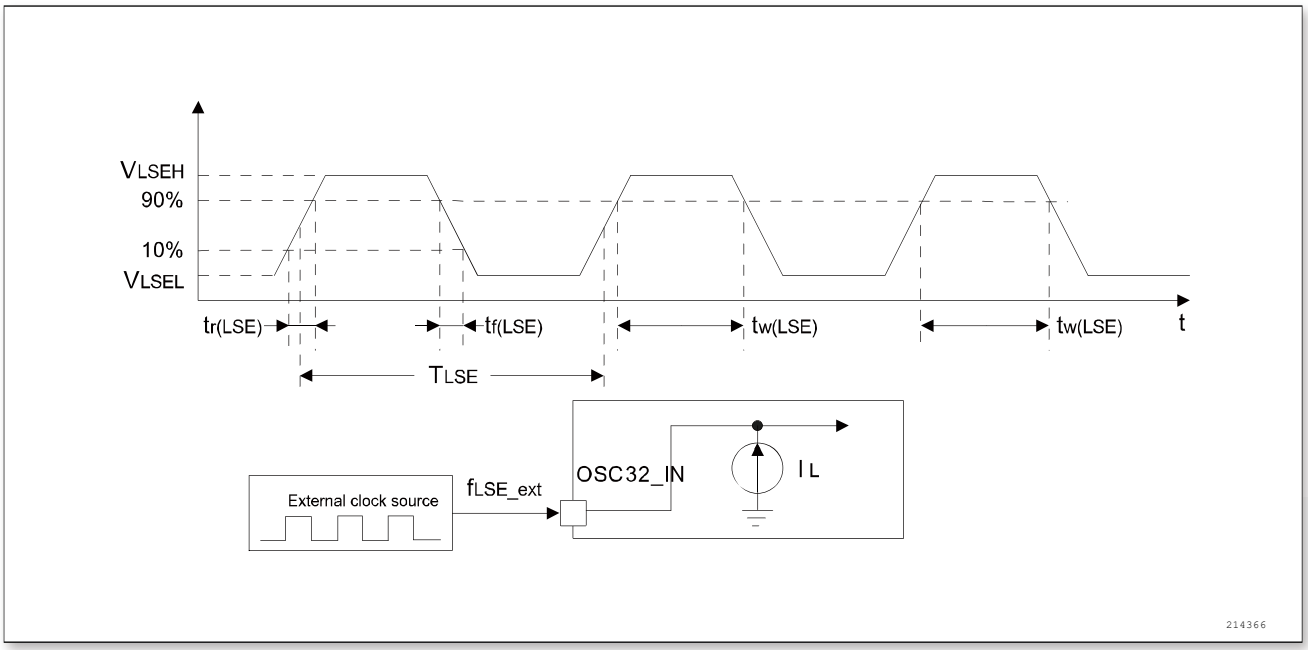

Figure 5-7 Low-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on the design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 5-14 HSE oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency (2)	2V<V_{DD}<3.6V	4	8	12	MHz
		3.0V<V_{DD}<5.5V	8	16	24	MHz
R_F	Feedback resistor (4)	-	-	1000	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2} (3) is 16pF)	f_{OSC_IN} =24MHz, V_{DD}=3V	-	-	50	Ω
		f_{OSC_IN} =12MHz, V_{DD}=2V	-	-	120	Ω
I_2	HSE current consumption	f_{OSC_IN} =24MHz, ESR=30 V_{DD} = 3.3V, C_{L1} C_{L2} (3) is 20pF	-	1.5	-	mA
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stable	-	3	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer characteristics Parameter.

2. Guaranteed by design, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the R_F resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment results in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

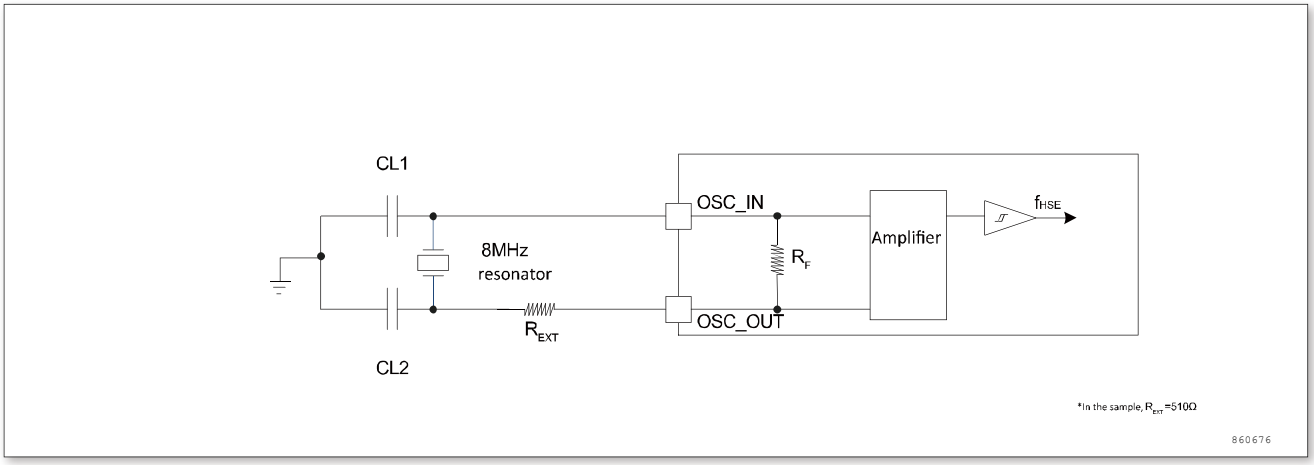

Figure 5-8 Typical application with an 8 MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.). (Note: the crystal oscillator is the passive crystal oscillator we usually refer to)

Note: For C_{L1} and C_{L2}, it is recommended to use a high quality 5pF ~ 15pF ceramic capacitor and a conformance crystal resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically gives the load capacitance parameters in serial combination of C_{L1} and C_{L2}. The load capacitor C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} pin capacitor and PCB board or

PCB-related capacitor, and its typical value is in 2pF ~7pF. Warning: To avoid surpassing the maximum value (15pf) of C_{L1} and C_{L2}, it is highly recommended to use a resonator with load capacitor $C_L \leq 7PF$. The resonator with load capacitor 12.5pF cannot be used. For example, if a resonator with load capacitor C_L = 6pF is selected and C_{stray} = 2pF, C_{L1} = C_{L2}= 8pF.

Table 5-15 LSE oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	2.0V<V_{DD}<5.5V	-	32.768	-	KHz
$I_{DD(LSE)}$ (2)	LSE current consumption	IBSEL=01 DR=00(recommend)	-	230	-	nA
		IBSEL=10 DR=01(Default)	-	300	-	nA
$t_{SU(LSE)}$ (3)	Startup time	V_{DD} is stablized	-	1	3	s

1. Drawn from comprehensive evaluation, not tested in production.
2. Select a high-quality oscillator (such as MSIVTIN 32.768KHz) with a smaller RS value to optimize current consumption. For details, please consult the crystal manufacturer.
3. $t_{SU(LSE)}$ is the startup time, measured from the moment it is enabled LSE by software to a stabilized 32.768KHz is reached. This value is measured from a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

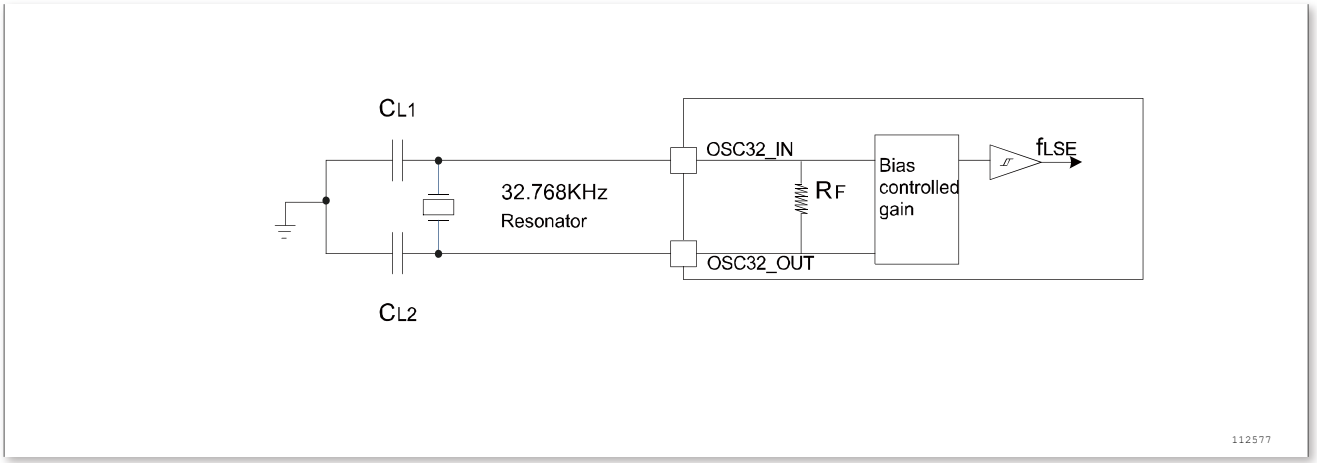

Figure 5-9 Typical application with a 32.768KHz crystal

5.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 5-16 HSI oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
ACC_{HSI}	HSI oscillator deviation	T_A = 0°C~ 55°C	-1	-	+1	%
		T_A = -40°C~ 85°C	-1.5	-	+1.5	%
		T_A = -40°C~ 105°C	-2.0	-	+2.0	%
$T_{stab(HSI)}$	HSI oscillator startup time	-	-	-	20	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	-	μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 5-17 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI} (2)	Frequency	T_A = -40°C~ 105°C	20	40	70	KHz
$t_{SU(LSI)}$ (3)	LSI oscillator startup time	-	-	-	100	μs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	-	0.20	-	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, unless otherwise stated.
2. Drawn from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

5.3.8 PLL1 characteristics

The relationship between the input clock frequency f_{PLL1_IN} and output clock f_{PLL1_OUT} frequency is:

$$\frac{f_{PLL1\_IN}}{(\mathrm{PLL1DIV}[2:0]+1)*(\mathrm{PLL1PDIV}[2:0]+1)} = \frac{f_{PLL1\_OUT}}{\mathrm{PLL1MUL}[7:0]+1}$$

PLL1MUL[6:0] and PLL1PDIV[2:0] and PLL1DIV[2:0] are the frequency division ratio settings of the PLL1 frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-18 PLL1 characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL1_IN}	PLL1 input clock (2)	-	4	8	24	MHz
D_{PLL1_IN}	PLL1 input clock duty cycle	-	20	-	80	%
f_{VCO}	VCO output clock	-	80	-	200	MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL1_OUT}	PLL1 output clock	-	40	-	100	MHz
$I_{DD(PLL1)}$	PLL1 current consumption	-	-	1550	-	uA

1. Guaranteed by design, not tested in production.
2. Use the correct multiplication factor to ensure the f_{PLL1_OUT} is within the allowable range according to the PLL1 input clock frequency.

5.3.9 PLL2 characteristics

The relationship between the input clock frequency f_{PLL2_IN} and output clock f_{PLL2_OUT} frequency is:

$$\frac{f_{PLL2\_IN}}{(\mathrm{PLL2DIV}[2:0]+1)*(\mathrm{PLL2PDIV}[2:0]+1)}=\frac{f_{PLL2\_OUT}}{\mathrm{PLL2MUL}[7:0]+1}$$

PLL2MUL[6:0] and PLL2PDIV[2:0] and PLL2DIV[2:0] are the frequency division ratio settings of the PLL2 frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

Table 5-19 PLL2 characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL2_IN}	PLL2 input clock (2)	-	4	8	24	MHz
D_{PLL2_IN}	PLL2 input clock duty cycle	-	20	-	80	%
f_{VCO}	VCO output clock	-	80	-	200	MHz
f_{PLL2_OUT}	PLL2 output clock	-	40	-	100	MHz
$I_{DD(PLL2)}$	PLL2 current consumption	-	-	1550	-	uA

1. Guaranteed by design, not tested in production.
2. Use the correct multiplication factor to ensure the f_{PLL2_OUT} is within the allowable range according to the PLL2 input clock frequency.

5.3.10 Memory characteristics

Table 5-20 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	131.5	-	154.5	μs
t_{ERASE}	Page (1024 bytes) erase time	-	4	-	6	ms
t_{ME}	Mass erase time	-	30	-	40	ms
I_{DD}	Supply current	Read mode	-	-	5.5	mA
		Write mode	-	-	2	mA
		Erase mode	-	-	1.5	mA

Table 5-21 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	-	100000	-	-	Cycles
T_{DR}	Data retention	T_A = 85℃	20	-	-	Years
		T_A = 25℃	100	-	-	

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB： A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 5-22 EMS characteristics

Symbol	Parameter	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 96MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	V_{DD} = 3.3V， T_A = +25℃, f_{HCLK} = 96MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.12 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 5-23 ESD & LU characteristics

Symbol	Parameter	Conditions	Class	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	C3	±1000	V

Symbol	Parameter	Conditions	Class	Maximum	Unit
I_{LU}	Latch-up current	T_A = 25°C, conforming to JESD78E	II, A	±200	mA
		T_A = 105°C, conforming to JESD78E		±100	mA

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 5-3 are used for tests. All I/O ports are CMOS compatible.

Table 5-24 I/O static characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	V_{DD} = 3.3V	-	-	0.8	V
V_{IL}	Low level input voltage	V_{DD} = 5V	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	V_{DD} = 3.3V	2.0	-	-	V
V_{IH}	High level input voltage	V_{DD} = 5V	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	V_{DD} = 3.3V	0.1 * V_{DD}	0.50	-	V
V_{hy}	Schmitt trigger hysteresis (1)	V_{DD} = 5V	0.1 * V_{DD}	0.60	-	V
I_{lkg}	Input leakage current (2)	V_{DD} = 3.3V	-1	-	1	μA
I_{lkg}	Input leakage current (2)	V_{DD} = 5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	V_{DD} = 3.3V, V_{IN} = V_{SS}	50	60	75	kΩ
R_{PU}	Weak pull-up equivalent resistor (3)	V_{DD} = 5V, V_{IN} = V_{SS}	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{DD} = 3.3V, V_{IN} = V_{DD}	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{DD} = 5V, V_{IN} = V_{DD}	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 5-1:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum

rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 5-3. All I/O ports are CMOS compatible.

Table 5-25 Output voltage static characteristics

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
11	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA, VDD=3.3V	-	0.13	-	V
	V_{OH} (2)	Output high voltage		-	3.12	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA, VDD=3.3V	-	0.18	-	
	V_{OH} (2)(3)	Output high voltage		-	3.06	-	
	V_{OL} (2)(3)	Output low voltage	$\|I_{IO}\|$=20mA, VDD=3.3V	-	0.5	-	
	V_{OH} (2)(3)	Output high voltage		-	2.62	-	
10	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA, VDD=3.3V	-	0.27	-	
	V_{OH} (2)	Output high voltage		-	2.94	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA, VDD=3.3V	-	0.37	-	
	V_{OH} (2)(3)	Output high voltage		-	2.80	-	
01	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA, VDD=3.3V	-	0.26	-	
	V_{OH} (2)	Output high voltage		-	2.94	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA, VDD=3.3V	-	0.37	-	
	V_{OH} (2)(3)	Output high voltage		-	2.80	-	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.
3. Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 5-3.

Table 5-26 I/O AC characteristics (1)(2)(3)

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
11	$t_{f(IO)out}$	Output fall time	C_L = 50pF VDD=3.3V	-	4.2	-	ns
	$t_{r(IO)out}$	Output rise time		-	5.0	-	ns
10	$t_{f(IO)out}$	Output fall time		-	8.9	-	ns
	$t_{r(IO)out}$	Output rise time		-	10.0	-	ns
01	$t_{f(IO)out}$	Output fall time		-	9.1	-	ns
	$t_{r(IO)out}$	Output rise time		-	10.5	-	ns

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this chip user manual.
2. The maximum frequency is defined in Figure 5-10.
3. Guaranteed by design, not tested in production.

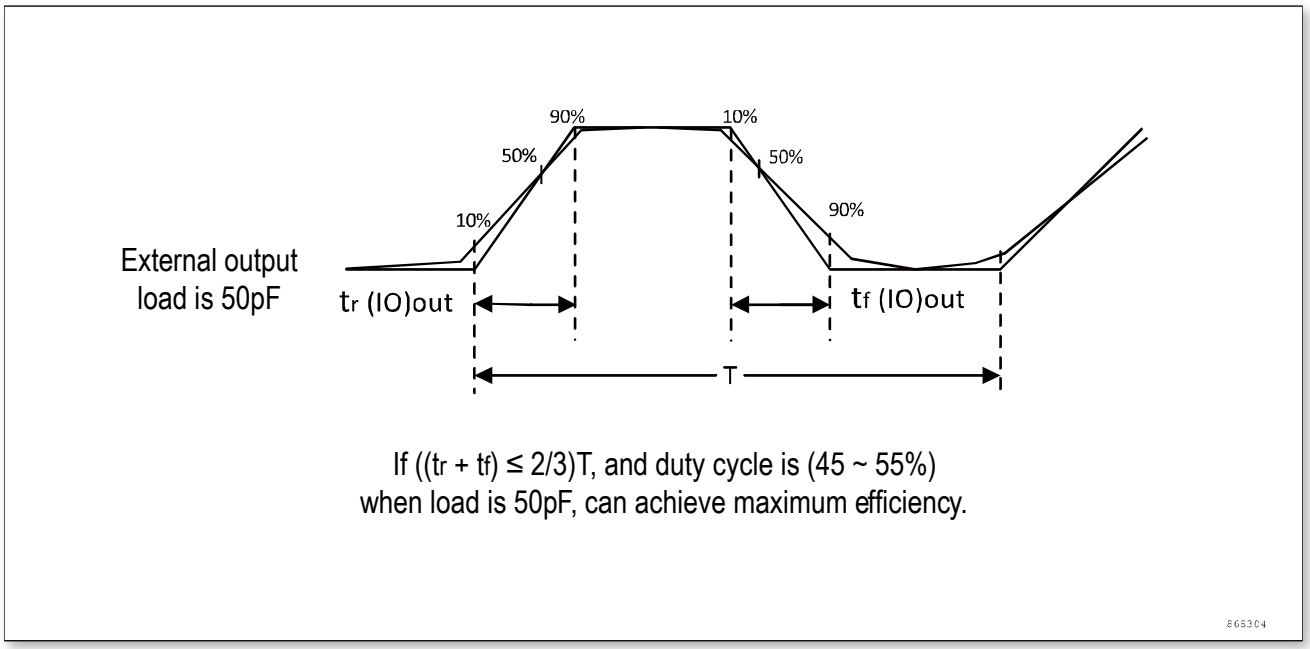

Figure 5-10 I/O AC characteristics

5.3.14 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured under the ambient temperature and V_{DD} supply voltage in accordance with the condition summarized in Table 5-3.

Table 5-27 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$ (1)	NRST input low voltage	V_{DD}=3.3V	-	-	0.8	V
$V_{IH(NRST)}$ (1)	NRST input high voltage	V_{DD}=3.3V	2.0	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD}=3.3V	-	0.6	-	V
R_{PU}	Weak pull-up equivalent resistor (1)	V_{IN} = V_{SS}	50	60	75	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	-	-	-	0.1	uS
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse	-	0.4	-	-	uS

1. Guaranteed by design, not tested in production.

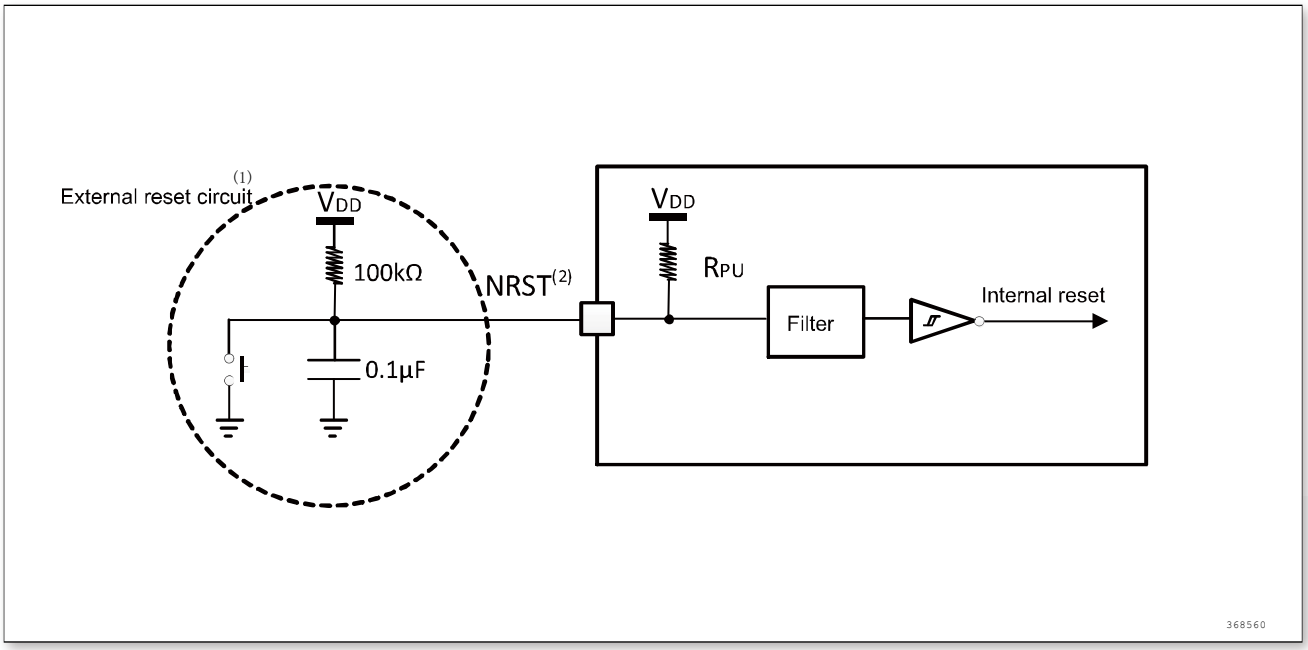

Figure 5-11 Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 5-27, otherwise the MCU cannot be reset.

5.3.15 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 5.3.13 I/O port characteristics.

Table 5-28 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	10.42	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 96MHz	0	96	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	0.01042	682.7	μs
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	-	44.74	S
t_{MAX_IN}	TIM maximum input frequency	-	-	192	MHz

1. Guaranteed by design, not tested in production.

5.3.16 I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 5-3.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 5.3.13 I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 5-29 I2C characteristics

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	9*t_{PCLK}	-	9*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	18*t_{PCLK}	-	18*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA setup time	1*t_{PCLK}	-	1*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (3)	- (4)	0 (3)	- (4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20×(V_{DD}/5.5V)	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{h(STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{su(STA)}$	Start condition setup time	19*t_{PCLK}	-	17*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition setup time	17*t_{PCLK}	-	17*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	484*t_{PCLK}	-	144*t_{PCLK}	-	us
C_b	Capacitive load of each bus	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. Ensure SCL drops below 0.3V_{DD} on falling edge before SDA crosses into the indeterminate range of 0.3V_{DD} to 0.7V_{DD}.

   NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to 0.3V_{DD} should be used to insert a delay of the SDA transition with respect to SCL.
4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
6. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

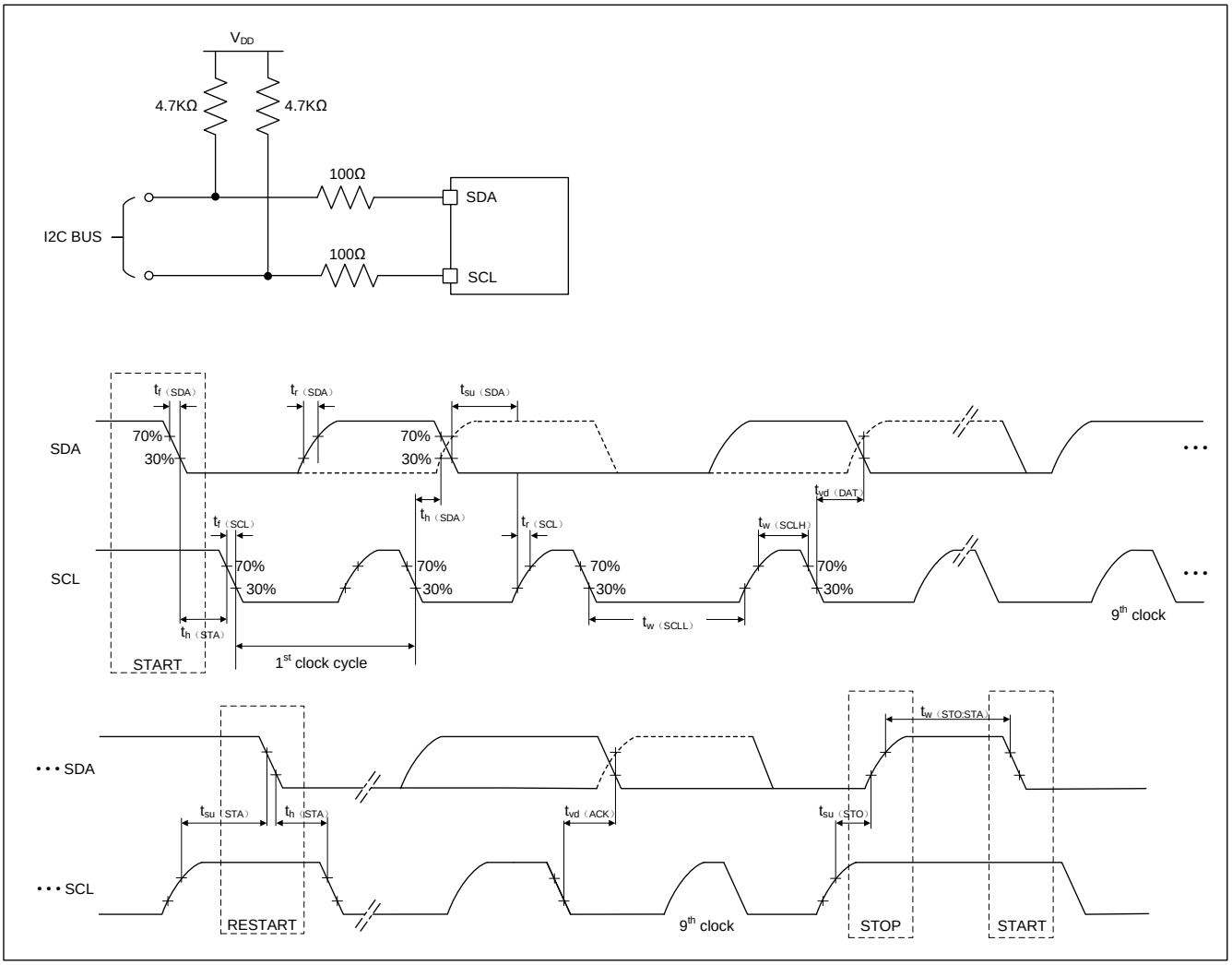

Figure 5-12 I2C bus AC waveform and measurement circuit (1)

1. Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.17 SPI interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 5-3.

Refer to section 5.3.13 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 5-30 SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, T_A = 25°C	-	36 (4)	MHz
		Slave mode, T_A = 25°C	-	18	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	10	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	10	-	ns
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	ns
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	15	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	15	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	15	ns

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.
4. When the SPI works at its limit speed, it is recommended to connect a serial matching resistor to the SCK wire to ensure the stability of transmission; and ensure that the SCK wire of the SPI Master and SPI Slave are as short as possible.

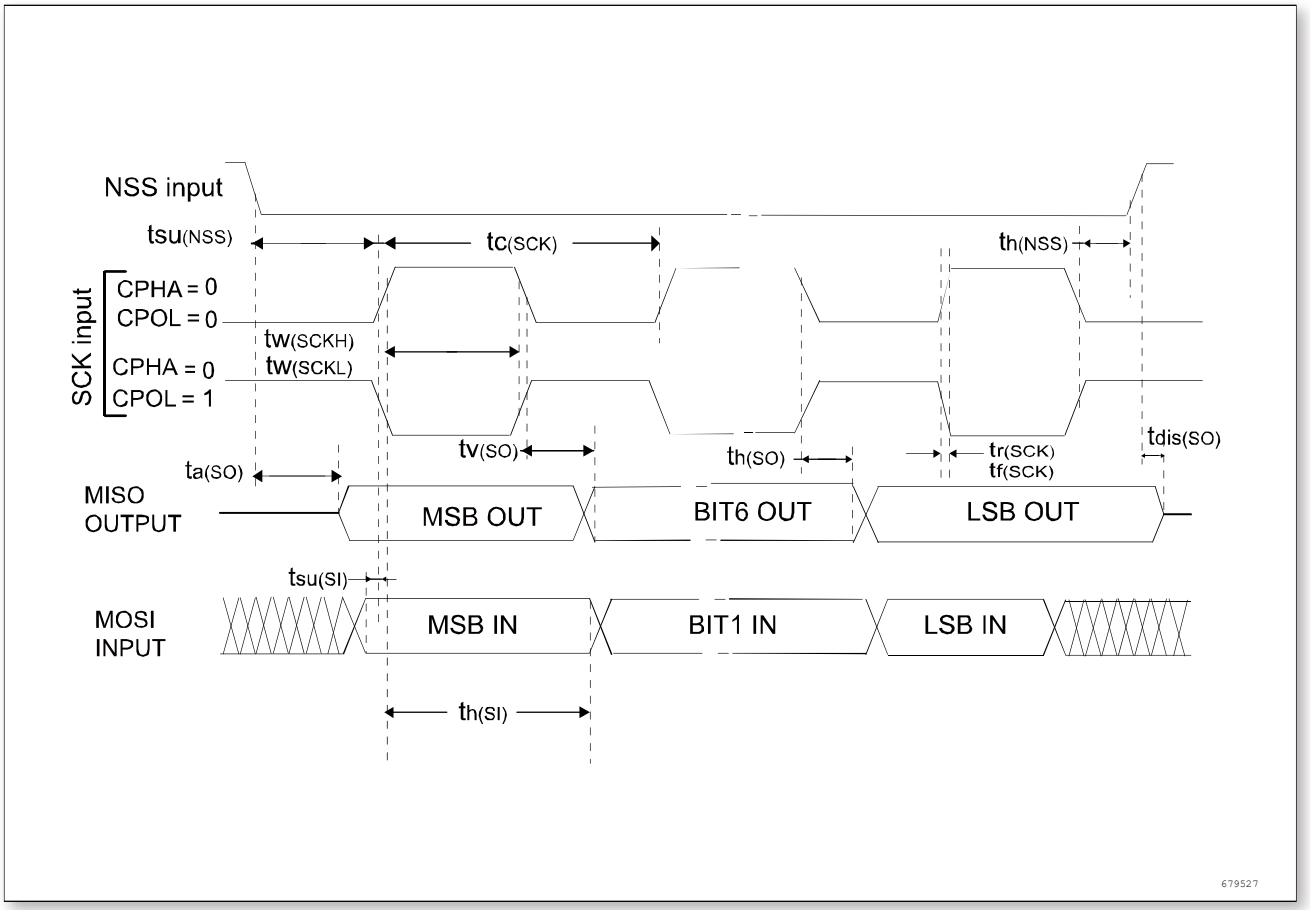

Figure 5-13 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

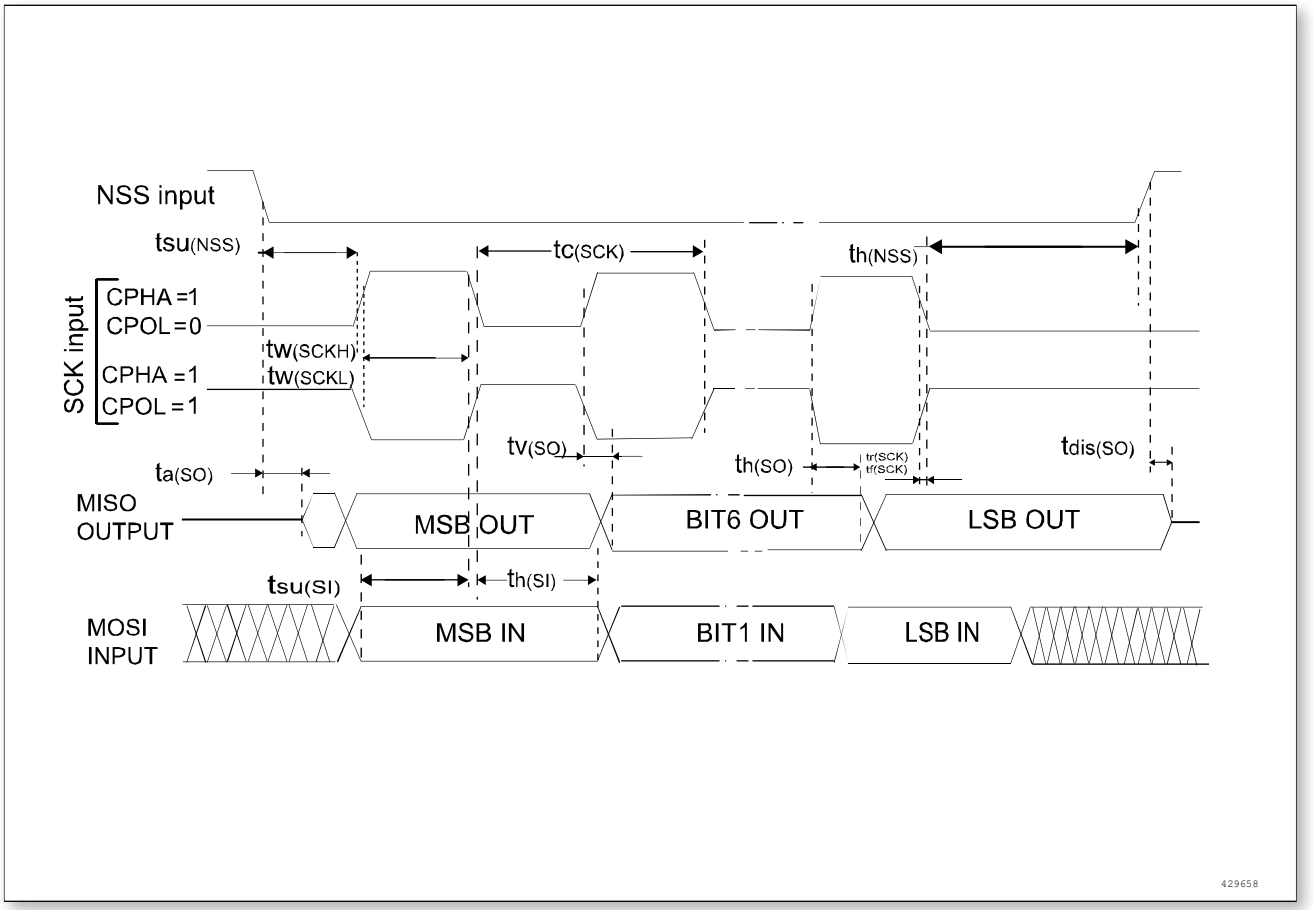

Figure 5-14 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

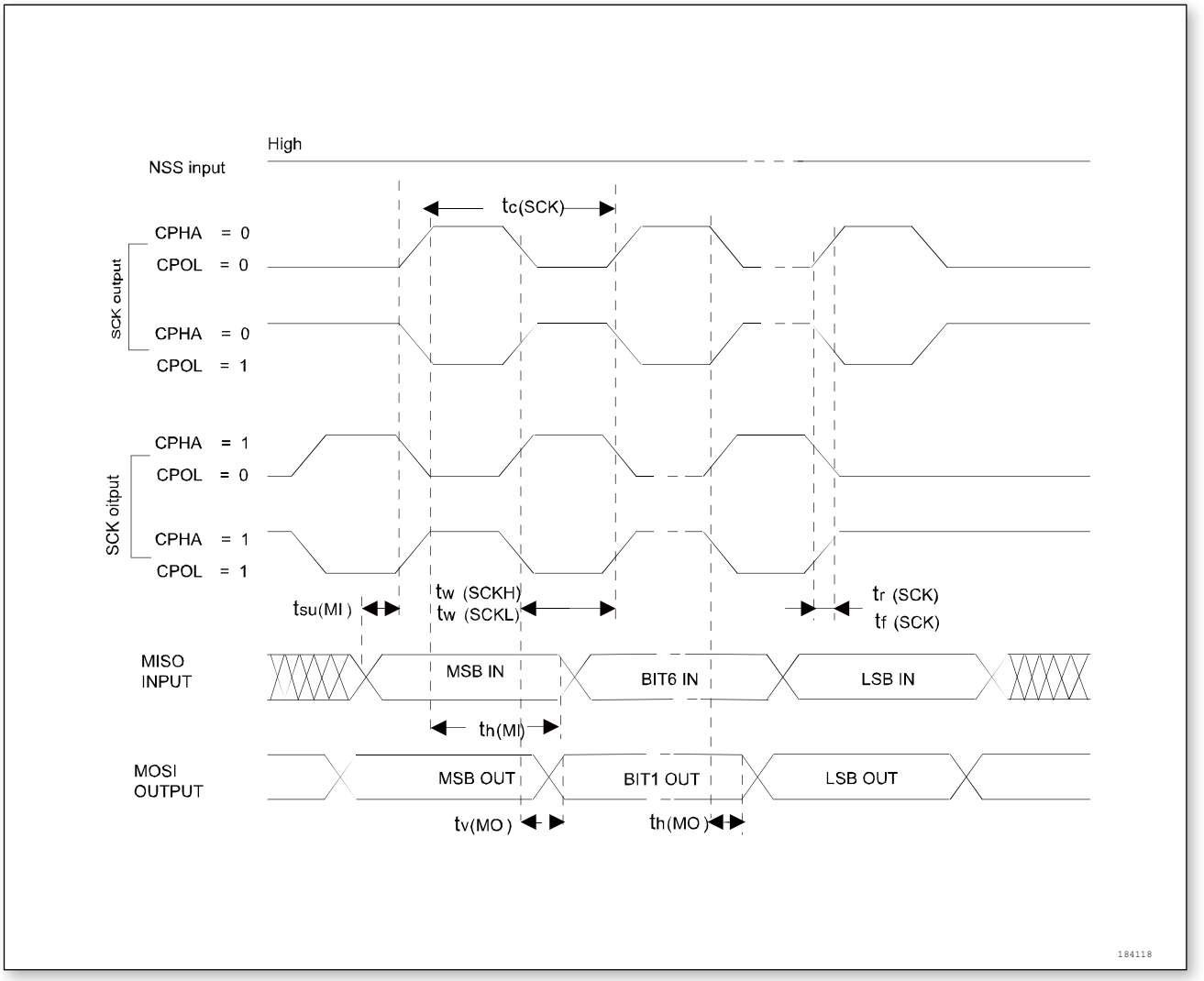

Figure 5-15 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.18 I3C slave interface characteristics

Table 5-31 I3C slave interface characteristics (communicate with legacy I2C device)

Symbol	Parameter	Fast mode		Fast+ mode		Unit
		Minimum	Maximum	Minimum	Maximum	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1	MHz
$t_{su(SDA)}$	SDA setup time	100	-	50	-	ns
$t_{h(SDA)}$	SDA hold time	-	-	-	-	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL Fall time	20*(V_{DD}/5.5V)	300	20*(V_{DD}/5.5V)	120	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL Rise time	20	300	-	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

Table 5-32 I3C slave interface characteristics (open-drain mode)

Symbol	Parameter	Minimum	Maximum	Unit
$t_{f(SDA\_OD)}$	SDA Fall time	-	12	ns
$t_{su(SDA\_OD)}$	SDA setup time during open drain mode	3	-	ns
t_{AVAL}	Bus available condition	1	-	us
t_{IDLE}	Bus idle condition	200	-	us

Table 5-33 I3C slave interface characteristics (push-pull mode)

Symbol	Parameter	Minimum	Typic	Maximum	Unit
f_{SCL}	SCL Clock Frequency	-	12.5	-	MHz
t_{SCO}	Clock in to data out for a slave	-	-	12	ns
$t_{r(SCL)}$	SCL rise time	-	-	$150/f_{SCL}$ (capped at 60)	ns
$t_{f(SCL)}$	SCL fall time	-	-	$150/f_{SCL}$ (capped at 60)	ns
$t_{su(SDA\_PP)}$	SDA setup in Push-Pull Mode	3	-	-	ns
C_b	Capacitive load per bus line	-	-	50	pF

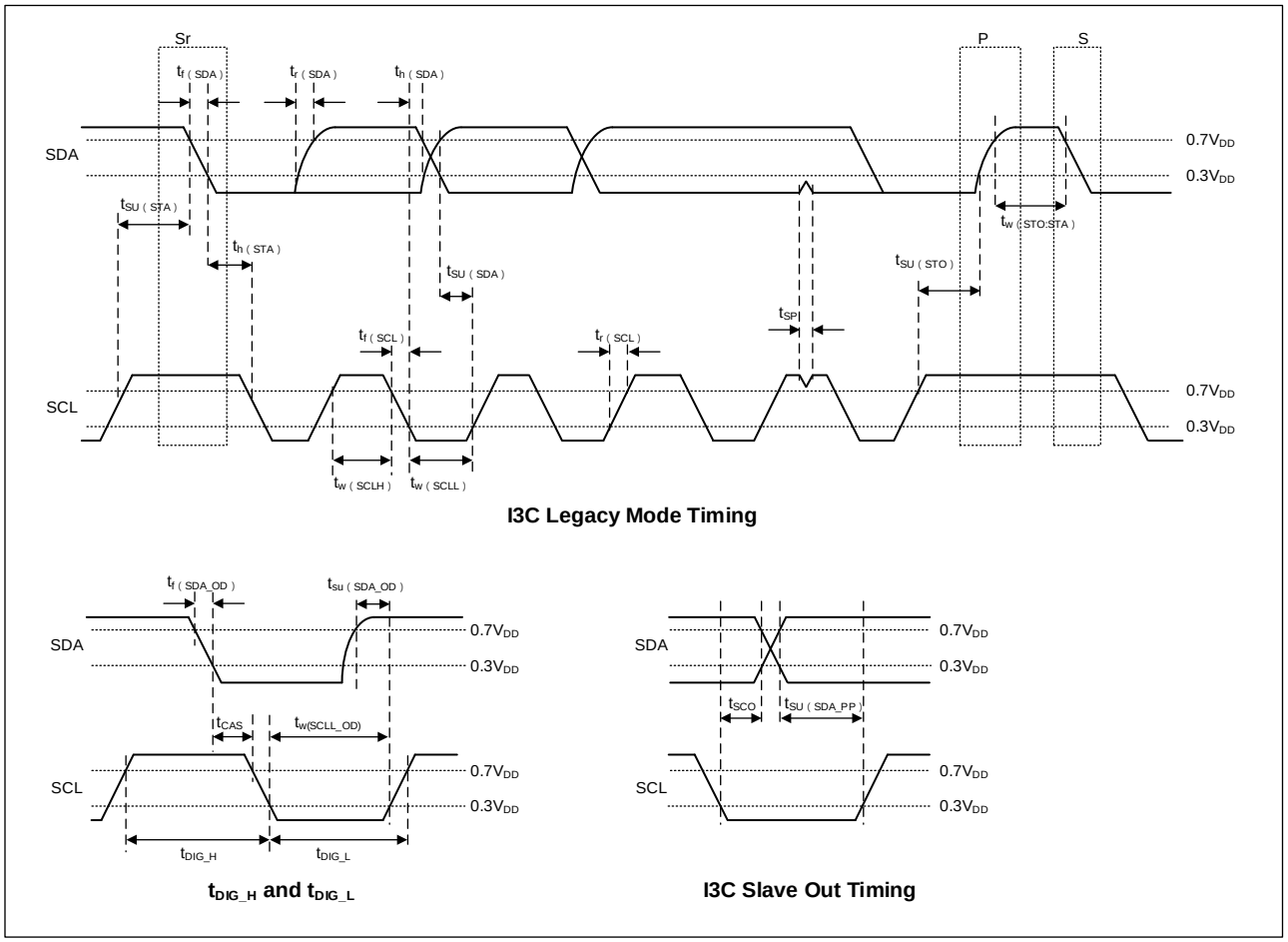

Figure 5-16 I3C slave interface characteristics

5.3.19 FlexCAN interface characteristics

For details on the characteristics of the input and output alternate function pins (CAN_TX and CAN_RX), see section 5.3.13 I/O port characteristics.

5.3.20 USB interface characteristics

Table 5-34 USB electrical characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
V_{DD}	USB operating voltage	D	-	3.0	3.6	V
V_{DI}	Differential input range	D	-	0.2	-	V
V_{CM}	Differential common mode range	D	-	0.8	2.64	V
V_{SE}	Single-end reception threshold	D	-	0.8	1.32	V
V_{OL}	Electrostatic output low voltage	D	Load resistance 1.5kΩ connected to 3.6V	-	0.3	V
V_{OH}	Electrostatic output high voltage	D	Load resistance 15kΩ connected to V_{SS}	2.8	3.6	V
R_{PU}	PA11/PA12 pull-up resistance	D	-	1.25	1.75	kΩ

Table 5-35 USB dynamic characteristics

Symbol	Parameter	Type	Conditions	Min.	Max.	Unit
t_r	Rising edge	D	C_L = 50pF	4	20	ns
t_f	Falling edge	D	C_L = 50pF	4	20	ns
V_{CRS}	Output signal crossover voltage	D	-	1.3	2.0	V

5.3.21 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 5-3.

Table 5-36 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S (1)	Sampling frequency	-	-	-	1	MHz
f_{TRIG} (1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	V_{DDA}	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	10	pF
t_{STAB} (1)	Stabilization time	-	-	-	10	μs
t_{latr} (1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S (1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	10.3	-	bit

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product, VREF+ is internally connected to VDDA， VREF− is internally connected to VSSA.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of $1/f_{ADC}$ must be added.

Input impedance

Equation 2

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 5-37 Maximum R_{AIN} at f_{ADC} = 16MHz (1)

T_S (cycles)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design. Not tested in production.

Table 5-38 ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-6/+5	LSB
EO	Offset error		-4/+2	
EG	Gain error		+5	
ED	Differential linearity error		-1/+2	
EL	Integral linearity error		-4/+3	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section 5.2 Absolute maximum rating does not affect the ADC accuracy.
2. Guaranteed based on characterization. Not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 5-17.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

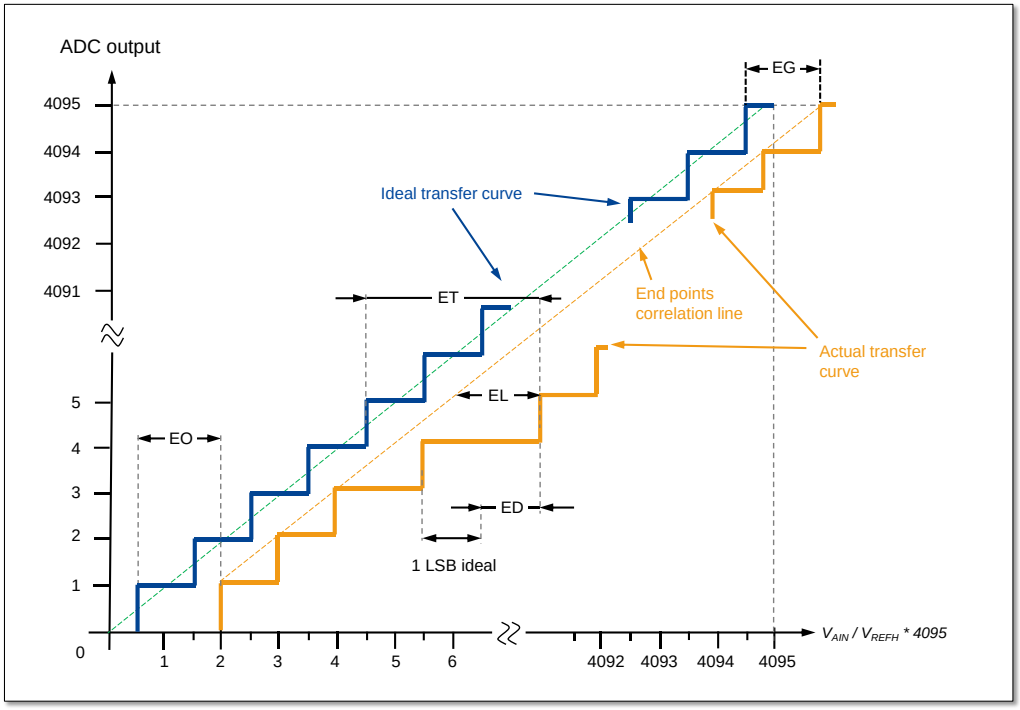

Figure 5-17 Schematic diagram of ADC static parameters

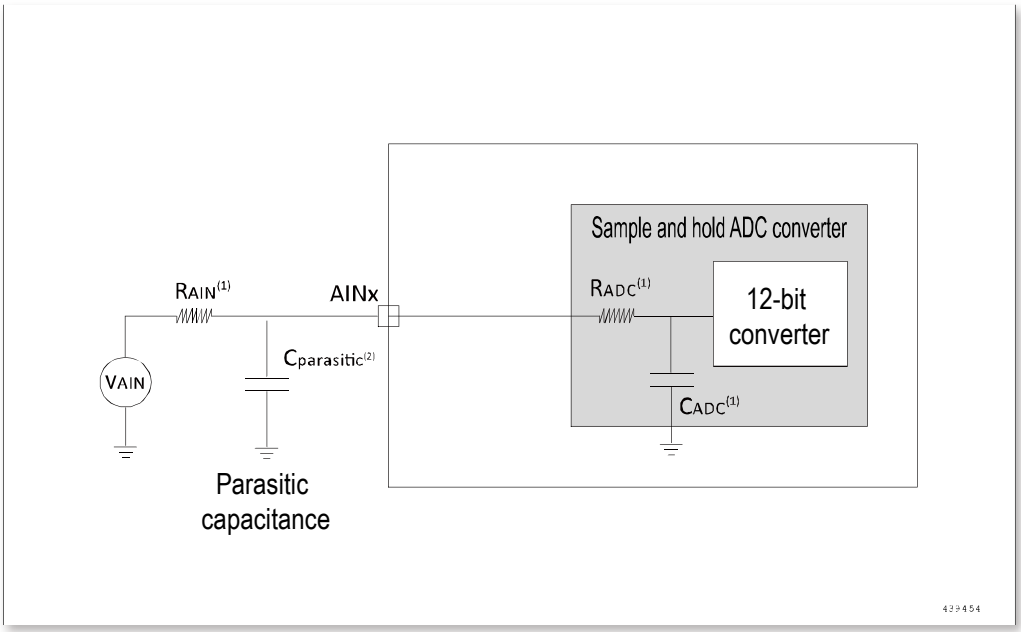

Figure 5-18 Typical connection diagram using the ADC

1. See Table 5-36 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nF capacitor in the figure must be a ceramic capacitor (good quality), and they should be as close as possible to the MCU chip.

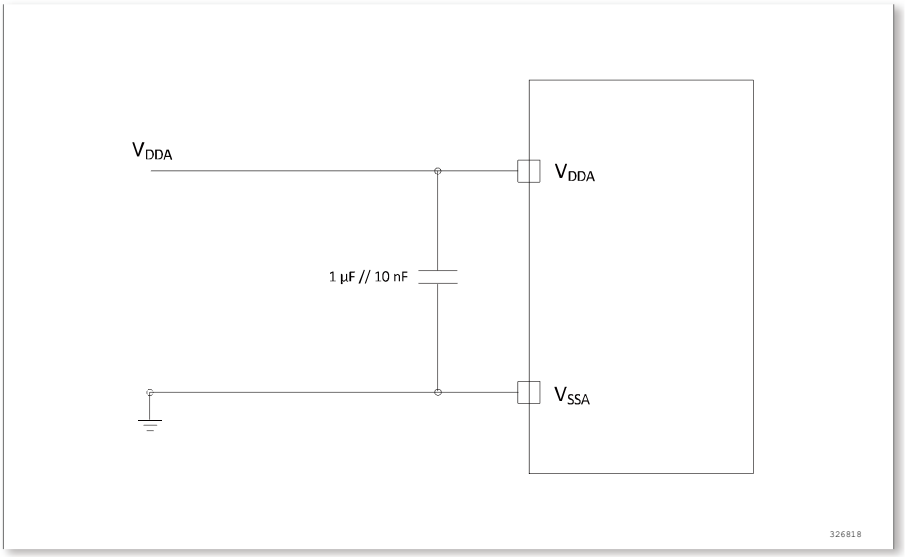

Figure 5-19 Power supply and reference power supply decoupling circuit

5.3.22 Temperature sensor characteristics

The temperature sensor is calculated using the formula below:

Temperature formula

$$TS_{adc} = 25 + \frac{Value * V_{DDA} - offset * 3300}{4096 * Avg\_Slope}$$

Where offset is recorded in the lower 12bits of 0x1FFFF7F6

Table 5-39 Temperature sensor characteristics (3)(4)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature	-10	-	+10	°C
Avg_Slope (2)	Average slope	4.4	4.955	5.313	mV/°C
V_{25} (1)	Voltage at 25℃	1.086	1.465	1.744	V
t_{START} (2)	Setup time	-	-	10	µS
t_{S_temp} (2)	ADC sampling time when reading temperature	-	11.8	-	µS

1. Guaranteed based on characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. The shortest sampling time can be determined by application through multiple iterations.
4. VDD = 3.3V

5.3.23 Comparator characteristics

Table 5-40 Comparator characteristics (1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{HYST}	Hysteresis	HYST = 00, MODE = 00	-	0	-	mV
		HYST = 01, MODE = 00	15	22	43	mV
		HYST = 10, MODE = 00	32	45	92	mV
		HYST = 11, MODE = 00	55	85	182	mV
		HYST = 00, MODE != 00	-	0	-	mV
		HYST = 01, MODE != 00	13	15	23	mV
		HYST = 10, MODE != 00	25.2	32	46.7	mV
		HYST = 11, MODE != 00	25.5	60	83.9	mV
V_{OFFSET}	Offset voltage	HYST = 00	-	±6	±15	mV
		HYST = 01	-	±5.5	±15	mV
		HYST = 10	-	±5	±15	mV
		HYST = 11	-	±4	±15	mV
t_{DELAY}	Propagation delay	MODE = 00	8.7	24	63	ns
		MODE = 01	10.0	45	103	ns
		MODE = 10	13.8	55	114	ns
		MODE = 11	22.2	95	194.5	ns
I_q	Average working current	MODE = 00	6.5	45	89.2	uA
		MODE = 01	3.3	8.6	24.7	uA
		MODE = 10	2.6	6	25.4	uA
		MODE = 11	1.7	4.6	16	uA

1. Guaranteed by design, not tested in production.

6 Package dimensions

6.1 LQFP64

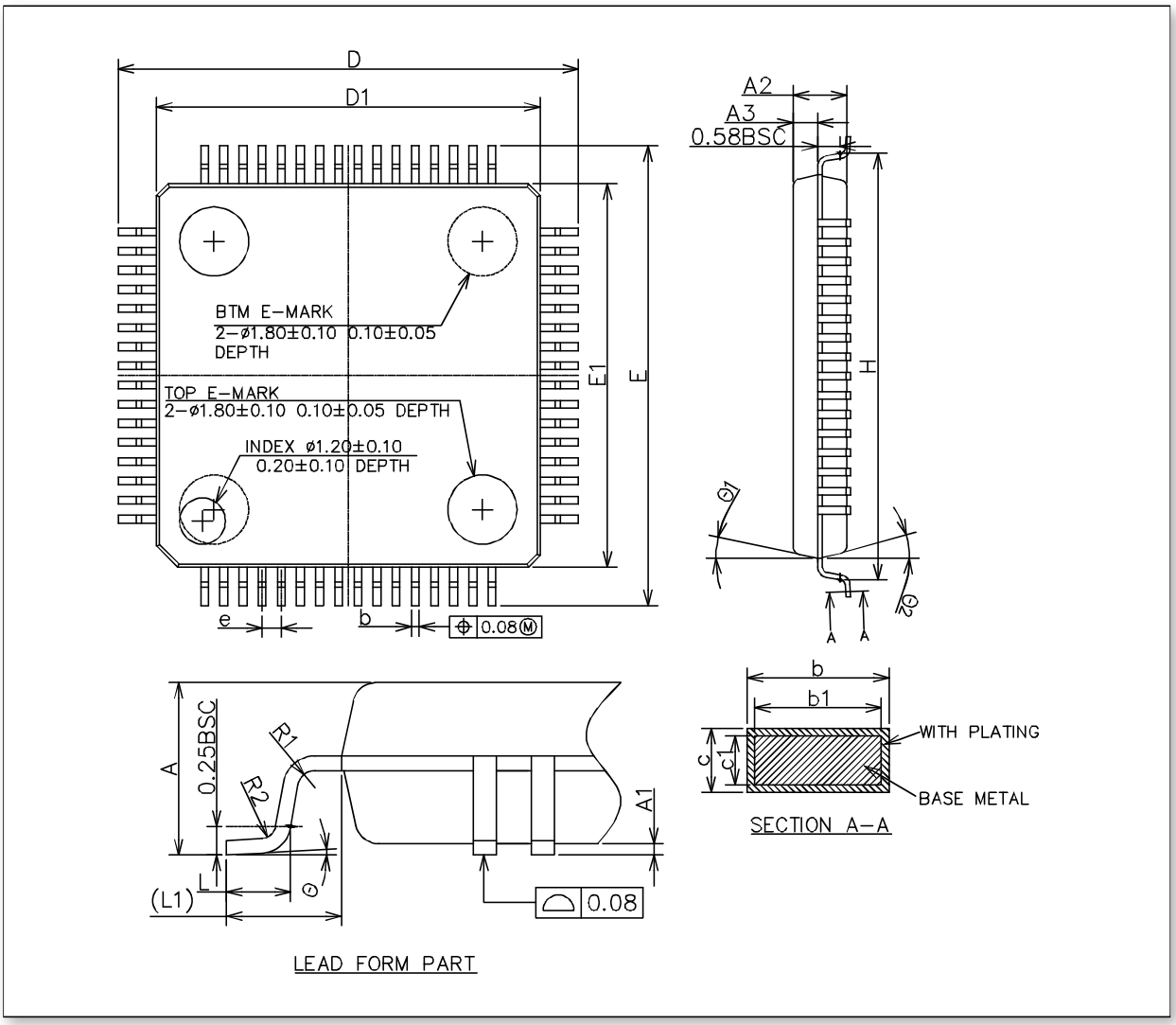

Figure 6-1 LQFP64 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 6-1 LQFP64 package dimension details

Symbol	Millimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	-	0.50	-
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

6.2 LQFP48

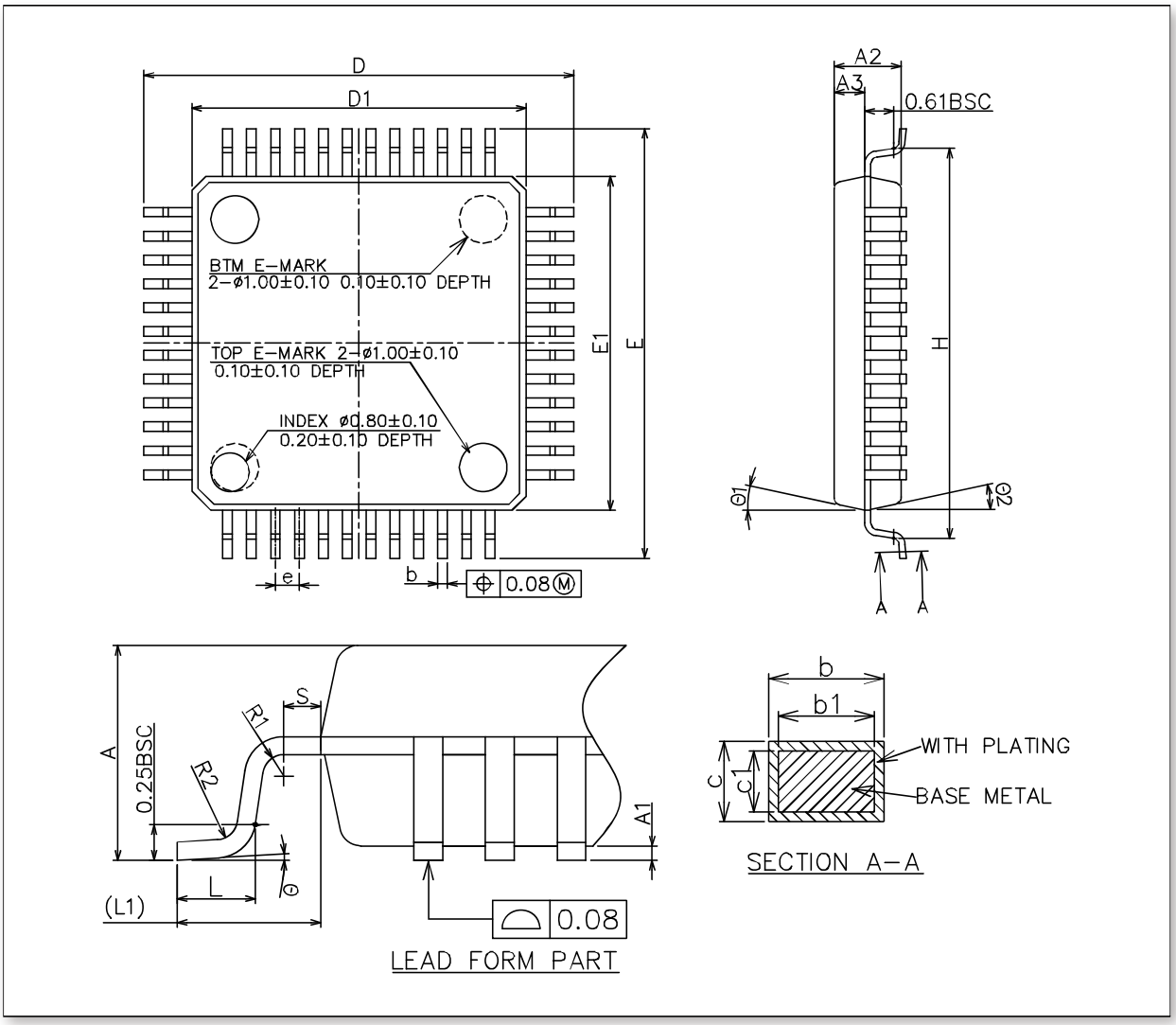

Figure 6-2 LQFP48 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-2 LQFP48 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

6.3 LQFP44

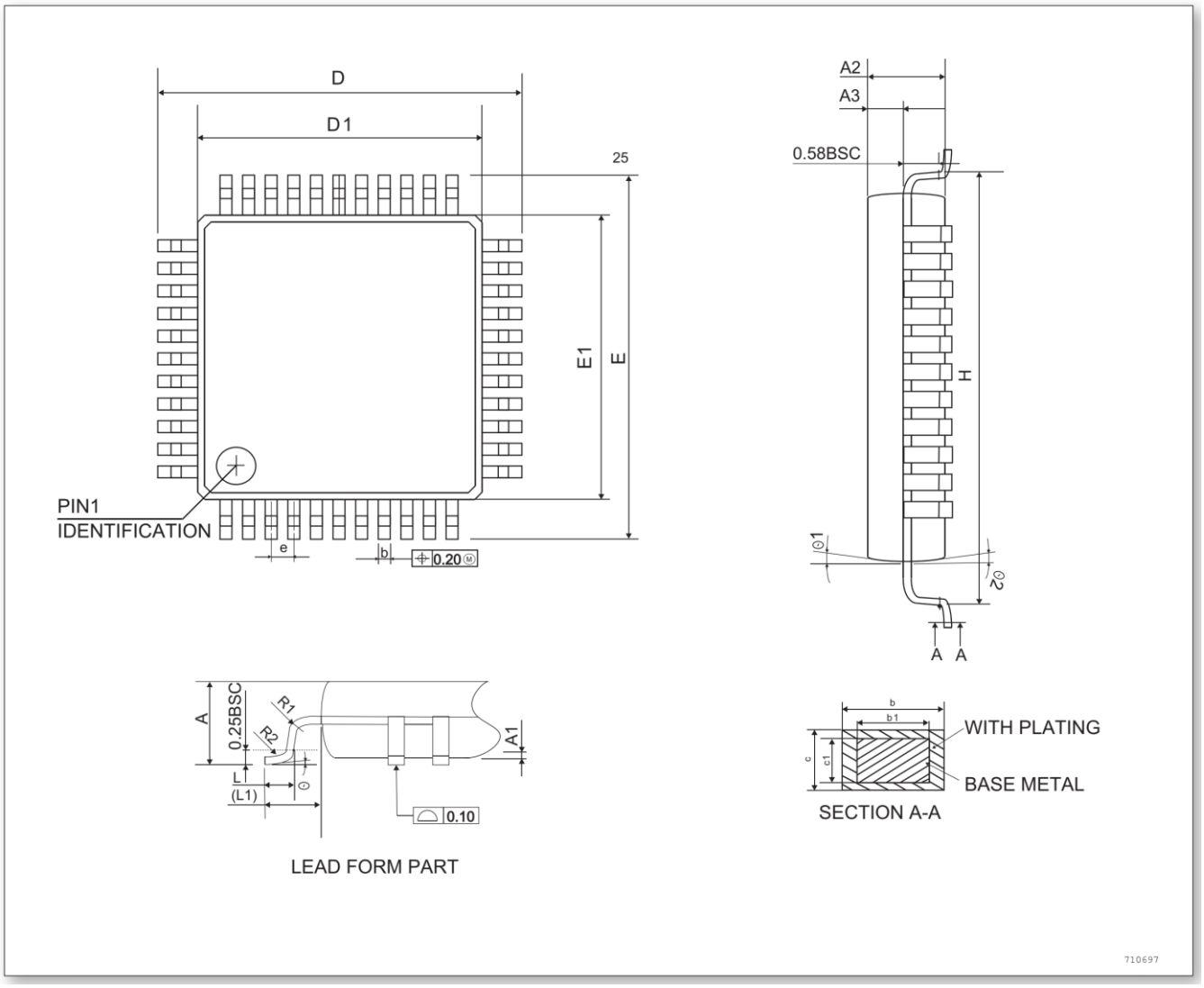

Figure 6-3 LQFP44 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-3 LQFP44 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12	12.05
D1	9.9	10	10.1
E	11.95	12	12.05
E1	9.9	10	10.1
e	-	0.8	-
H	11.09	11.13	11.17
L	0.53	-	0.7
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0 ◦	3.5 ◦	7 ◦
θ1	11 ◦	12 ◦	13 ◦
θ2	11 ◦	12 ◦	13 ◦

6.4 QFN32

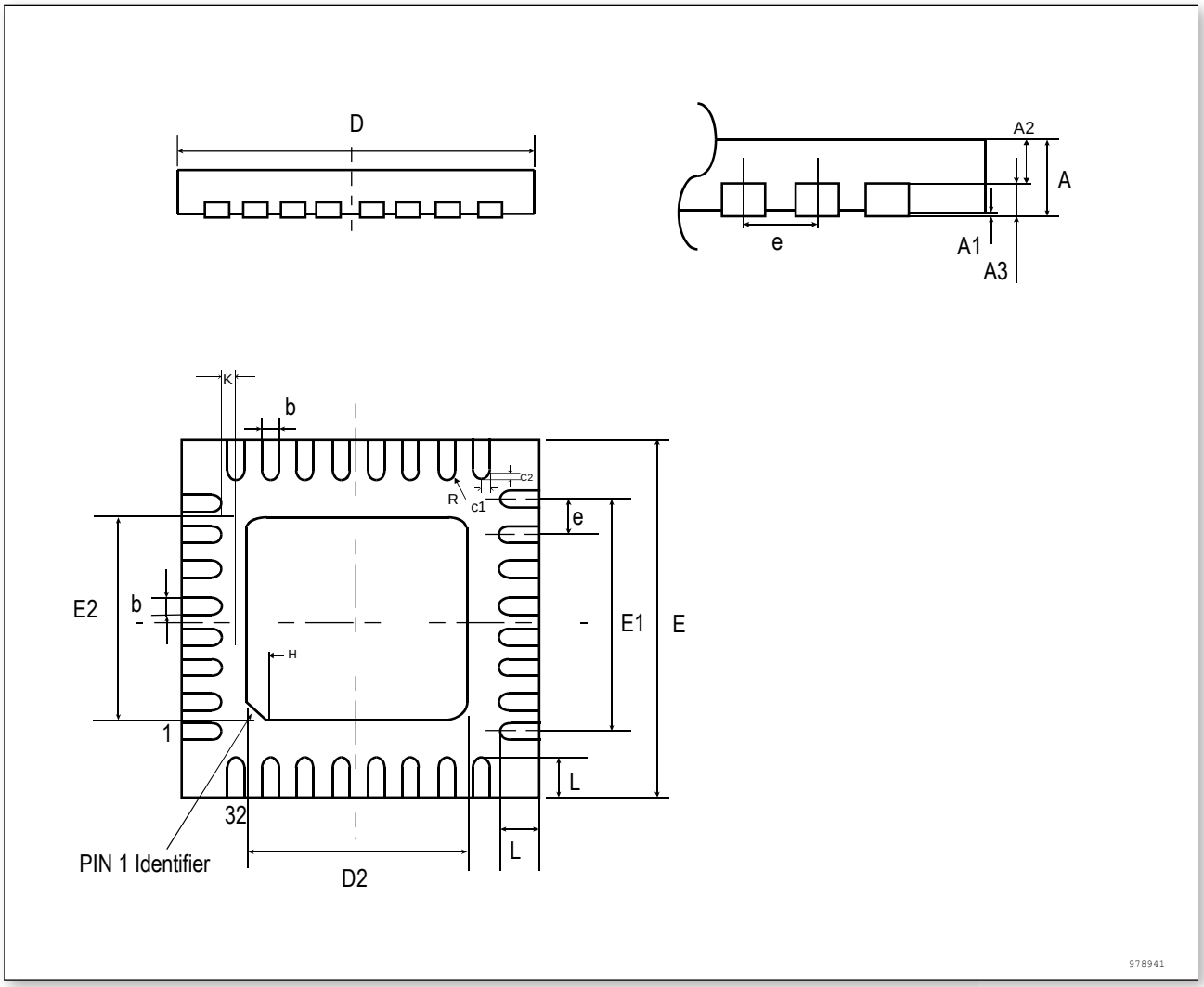

Figure 6-4 QFN32 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-4 QFN32 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e	-	0.5	-
H	0.30REF		
K	0.35REF		
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-
N	Pin count = 32		

6.5 QFN28

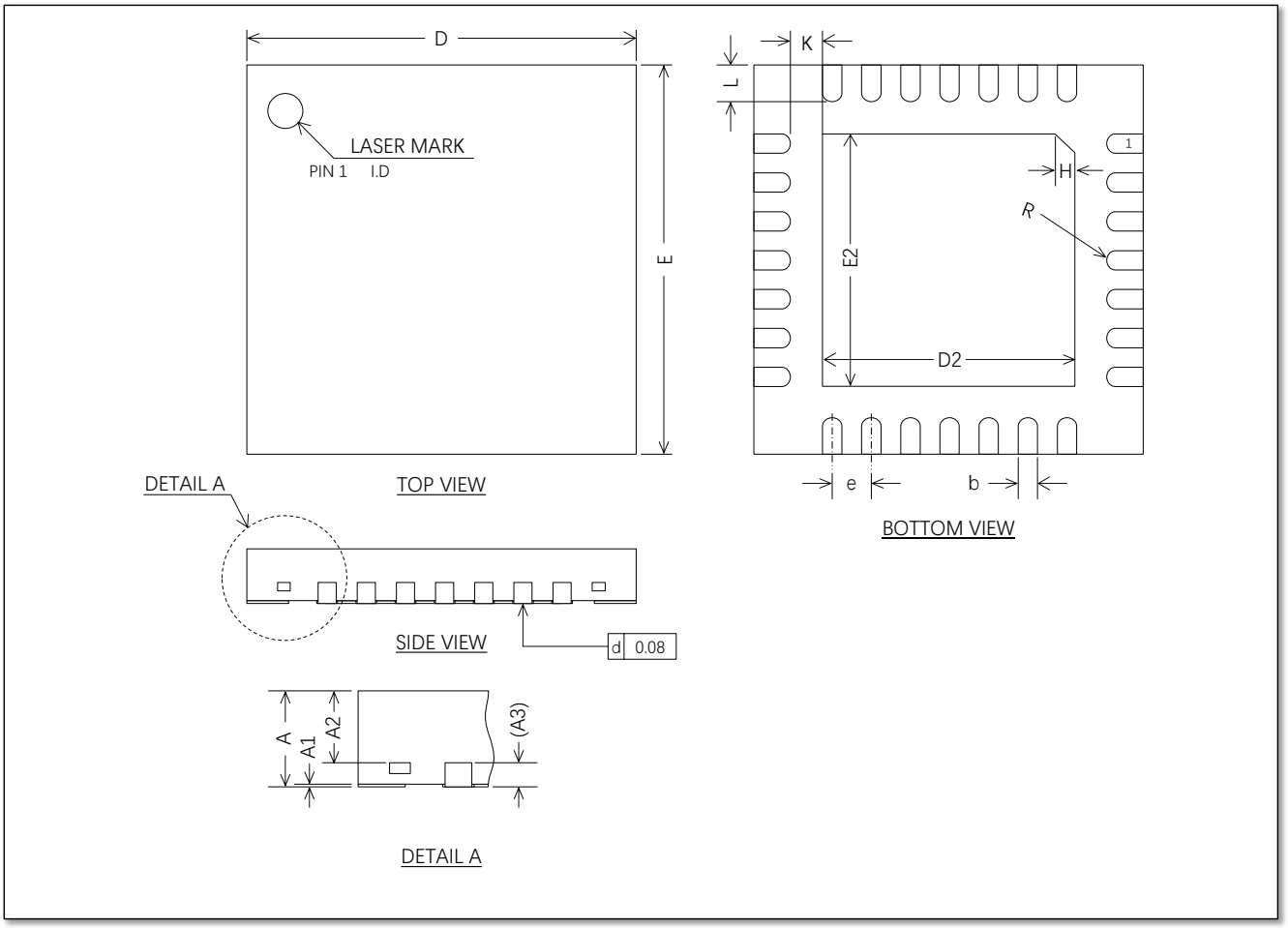

Figure 6-5 QFN28 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Table 6-5 QFN28 package dimension details

ID	Millimeters		
	Minimum	Typical	Maximum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	-	0.40	-
H	0.35REF		
K	0.30REF		
L	0.35	0.40	0.45
R	0.075	-	-

7 Revision history

Table 7-1 Revision history

Date	Revision	Description
2023/7/4	Rev1.1	Updated the maximum operation frequency to 96MHz
2023/5/30	Rev1.0	Added data to ESD & LU characteristics Added Peripheral status in different power modes table Updated Power scheme figure Removed watermark Added LQFP44 package
2023/1/5	Rev0.5	Preliminary release