Datasheet

MM32F103xx

32-Bit Micro controller based on Arm® Cortex® M3

Version: 1.11_n

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1 General Introduction

General Introduction

1.1 Introduction

This product incorporates a high-performance 32-bit microcontroller with the core of Arm® Cortex®-M3. The highest operating frequency is up to 96MHz, with built-in high-speed memory, a rich set of enhanced I/O ports and peripherals connected to the external bus. This product contains two 12-bit ADCs, two 12-bit DACs, three 16-bit general-purpose timers and one 16-bit advanced timer as well as standard communication interfaces: two I2Cs, two SPIs, one USB, one CAN and three UARTs.

The device works between 2.0V to 5.5V range. The regular temperature for the device is -40°C to +85°C. A comprehensive set of power-saving mode allows the design of low-power applications.

The devices are available in 4 different packages: LQFP64, LQFP48, LQFP32 and QFN32.

The abundant peripherals make this microcontroller suitable for a variety of applications:

- Motor drive and application control
- Healthcare and handheld device
- PC gaming peripherals and GPS platform
- Industrial applications: programmable controllers (PLCs), inverters, printers and scanners
- Alarm system, video intercom, heating, ventilation and air conditioning

1.2 Product Characteristics

- Core and system
  - 32-bit Arm® Cortex®-M3 processor as the core
  - Maximum operating frequency is up to 96MHz
- Memory
  - Up to 128K Bytes of Flash memory
  - Up to 20K Bytes of SRAM
  - Boot loader supports Chip Flash and ISP (In-System Programming)
- Clock, reset and power management
  - 2.0V to 5.5V power supply
  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - External 8 ~ 24MHz high speed crystal oscillator

  - Embedded factory-tuned 48MHz high speed oscillator
  - Support multiple PLL and divider modes for USB clock sources
  - PLL supports CPU running at 96MHz
  - Built-in 40KHz low speed oscillator
  - External 32.768KHz low speed oscillator
- Low-power
  - Sleep, Stop and Standby modes
- Two 12-bit ADCs and 1μS of conversion time (up to 16 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
- Two 12-bit DACs
- One 7-channel DMA controller
  - Supported peripherals: Timer, ADC, DAC, UART, I2C, SPI and USB
- Up to 51 fast I/Os:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports are capable of inputting and outputting 5V signals
- Debug mode
  - Serial wire debug (SWD) and JTAG interface
- Up to 7 timers
  - One 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead time generation and emergency stop functions
  - Three 16-bit timers providing up to 4 input captures/output compares, usable for IR control decoding
  - Two watchdog timers (independent and window type)
  - SysTick timer: 24-bit downcounter
- Up to 9 Communication interfaces
  - Three UART interfaces
  - Two I2C interfaces
  - Two SPI interfaces
  - One CAN interface
  - One USB device full-speed interface
- Packages LQFP64, LQFP48, LQFP32 and QFN32

For more information about the complete product, refer to Section 2.2 of the data sheet. The relevant information about the Cortex®-M3, please refer to Cortex®-M3 technical reference manual.

2 Specification

Specification

2.1 Device contrast

Table 1. MM32F103xx device features and peripheral counts

Peripheral		MM32F103RB/8T		MM32F103CB/8T		MM32F103KB/8T		MM32F103KB/8U	
Flash memory -K Bytes		128	64	128	64	128	64	128	64
SRAM -K Bytes		20	20	20	20	20	20	20	20
Timers	General purpose (16 bit)	3		3		3		3	
	Advanced control	1		1		1		1	
Communication interfaces	UART	3		3		2		2	
	I2C	2		2		1		1	
	SPI	2		2		1		1	
	USB	1		1		1		1	
	CAN	1		1		1		1	
GPIOs		51		37		23		25	
12-bit ADC	numbers	2	2	2	2	2	2	2	2
	channels	16	16	10	10	10	10	10	10
12-bit DAC	numbers	2	2	2	2	2	2	2	2
	channels	2	2	2	2	2	2	2	2
Max CPU frequency		96 MHz							
Operating voltage		2.0V ~ 5.5V							
Packages		LQFP64		LQFP48		LQFP32		QFN32	

2.2 Summary

2.2.1 Arm® Cortex®-M3 as the core with embedded flash memory and SRAM

The Arm® Cortex®-M3 processor is configurable and has multilevel pipeline 32-bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Embedded flash memory

The embedded flash memory is up to 128K bytes, usable for storing programs and data.

2.2.3 SRAM

The embedded SRAM is up to 20K bytes

2.2.4 Cyclic Redundancy Check (CRC) Calculation Unit

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based techniques are used to verify the consistency of data transmission or storage.

Within the scope of the EN/IEC60335-1 standard, it provides a means of detecting flash memory errors that can be used to compute the signature of the software in real time and to compare the generated signatures when linking and generating the software.

2.2.5 Nested vectored interrupt controller (NVIC)

This product embeds a nested vectored interrupt controller, which can handle multiple maskable interrupting channels (excluding 16 Cortex™-M3 interrupt lines) with 16 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the core
- Tightly coupled NVIC interfaces
- Allows early processing of interrupts
- Handles higher-priority interrupts that arrive late
- Support tail-chaining of interrupts
- Automatically saves the processor state
- Offer automatic recovery when the interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.2.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of multiple edge detectors used to generate interrupt/event requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge or both) and can be masked independently. A pending register maintains the status of all interrupt requests. The EXTI can detect a signal with a pulse width shorter than the internal AHB clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Clocks and startup

System clock selection is performed on startup; however, the internal 48 MHz oscillator with 6 division is selected as default CPU clock on reset. Then an external 8~24 MHz clock with failure monitoring function can be selected. If an external clock failure is detected, the clock will be isolated and PLL will be turned off. The system automatically switches back to the internal oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure AHB frequency and high-speed APB (APB2 and APB1) domains. The maximum frequency of AHB and high-speed APB is 96MHz. Please refer to the clock drive diagram in figure 2.

2.2.8 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is stored in the system memory, and can reprogram the flash by UART1.

2.2.9 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.5V ~ 5.5V: external power supply for the analog part pf ADC, reset module, oscillator and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
- V_{BAT} = 1.8V ~ 5.5V：power supply for RTC, external clock 32 KHz oscillator and backup registers (through internal power switch) when V_{DD} is not present.

2.2.10 Power supply supervisors

This product has integrated power-on reset (POR)/power-down reset (PDR) circuit. The circuit remains in the working state and ensures proper operation above a threshold of 2.0V. When V_{DD} is below a specified threshold ($V_{POR/PDR}$), the device will be placed in the reset state, without the need for an external reset circuit.

Additionally, the device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, an interrupt can be generated. The interrupt handler will send a warning message or switch the microcontroller to the safe mode. The PVD function should be enabled by a program.

2.2.11 Voltage regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low-power modes (LP)

The product support low-power mode to achieve the best compromise between low-power consumption, short start-up time and multiple wake-up events.

Table 2. Low power mode list

Mode	Entry	Wakeup	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
SLEEP NOW or SLEEP ON EXIT	WFI (Wait for Interrupt)	Any interrupt	CPU clock off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wake-up event			
Stop	PDDS=0 SLEEPDEEP=1 WFI or WFE	Any arbitrary interrupt (set in the external interrupt register)	All 1.5V area clocks are off	PLL, HSI and HSE oscillator off	On
Standby	PDDS=1 SLEEPDEEP=1 WFI or WFE	WKUP pin rising edge, RTC clock event, NRST pin external reset, IWDG reset			Off

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers. The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the EXTI signals. The EXTI signal can be a wake up signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The Standby mode can minimize the power consumption of the system. In the Standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. The entire 1.5V power supply domain is disconnected. PLL, HSI and HSE oscillators are also turned

off. They can be woken up by the rising edge of WKUP pin, external reset of NRST pin and IWDG reset. They also can be woken up by the watchdog timer without reset. The contents of SRAM and registers will be lost. Only the backup registers and the standby circuit provide power supply.

2.2.13 Direct memory access controller (DMA)

The flexible 7-way general-purpose DMA can manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports the management of the ring buffer, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel has a dedicated hardware DMA request logic, with support for software trigger on each channel. The length, the source address and the destination address of the transfer can be set separately by the software.

The DMA can be used with major peripherals: UART, I2C, SPI, ADC, DAC, USB and general-purpose, basic, advanced timer TIMx.

2.2.14 Real-time clock register (RTC)

The real time clock is an independent timer. The RTC module has a set of counters that count continuously and provides the clock calendar function in the appropriate software configuration. Modify the value of the counter to reset the current time and date of the system. The RTC module and the clock configuration system (RCC_BDCR register) are in the backup area, ie the RTC settings and time remain unchanged after a system reset or wake-up in standby mode.

2.2.15 Backup register (BKP)

The backup registers are ten 16-bit registers used to store user application data. when V_{DD} power is not present. they are in the backup registers and still powered by V_{BAT}. They are also not reset when the system is woken up in standby mode, or when the system is reset or power is reset.

2.2.16 Timers and watchdogs

The product includes one advanced timer, three general-purpose timers, two watchdog timers and one SysTick timer.

The following table compares the functions of advanced timer, general-purpose timer and basic timer:

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/-compare channels	Complem-entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	Yes
General purpose	TIM2	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
	TIM4	16-bit	Up	integer from 1 to 65536	Yes	4	No

Advanced-control timer (TIM1)

The advanced control timer is composed of one 16-bit counter, four capture/compare channels and a three-phase complementary PWM generator. It has complementary PWM outputs with dead time insertion and can be used as a complete general-purpose timer. Four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-alignment mode)
- One-pulse mode output

If configured as a 16-bit general-purpose timer, it has the same features as the TIM2 timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

Three synchronizable general-purpose timers (TIM2, TIM3, TIM4) are built into the product. The general-purpose timer has one 16/32 bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and one-pulse mode output.

General-purpose timers 16-bit

The general-purpose timer has one 16-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and one-pulse mode output.

The timer can work together or with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 ~ 4 hall effect sensors.

Independent watchdog (IWDG)

The independent watchdog contains one 12-bit down-counter and one 8-bit prescaler. There is an internal independent 40KHz clock oscillator. This oscillator operates independently from the master clock, so it can work in the Stop and Standby modes. It can be used to reset the entire system in the event of system failure or used as a free timer to provide timeout management for applications.

Window watchdog (WWDG)

The window watchdog has one 7-bit down-counter that can be set to run freely. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. In the debug mode, the counter can be frozen. The option bytes can be configured to boot watchdog via software or hardware. In the debug mode, the counter can be frozen.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.17 Universal asynchronous receiver/transmitter (UART)

The UART interface supports LIN master-slave function.

All UART interface can be served by the DMA controller.

2.2.18 I2C bus

I2C bus interface can operate in the multi-master mode or slave mode and it supports the standard mode and the fast mode.

It supports 7-bit and 10-bit addressing.

2.2.19 Serial peripheral interface (SPI)

The SPI interface can be configured to 1~32 bits per frame in the slave or master mode.The maximum rate is 24M for master mode and 12M for slave mode

All SPI interface can be served by the DMA controller.

2.2.20 Universal serial bus (USB)

The microcontroller embeds a USB device controller compatible with the USB full-speed (12 Mbs) standard, with software-configurable endpoints. The USB-specific 48 MHz clock is generated directly from the internal PLL or the internal clock (HSI) at the room temperature.

2.2.21 Controller area network (CAN)

The CAN is compliant with specifications 2.0 A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

2.2.22 General-purpose inputs/outputs (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without pull-up/pull-down), or alternate peripheral function. Most GPIO pins are shared with digital or analog alternate peripherals.

If required, the peripheral function of the I/O pins can be locked following a specific sequence in order to avoid spurious writing to the I/O registers.

2.2.23 Analog-to-digital converter (ADC)

The product is embedded with two 12-bit analog-to-digital converter (ADC) which has up to 16 external channels and is available for single-shot, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

All ADC can be served by the DMA controller.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timers (TIMx) and the advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize the ADC conversion with the clock.

2.2.24 Digital-to-analog converter (DAC)

The DAC module is a 12-bit digital-to-analog converter with digital input and voltage output. The DAC can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller. In 12-bit mode, the data could be left- or right-aligned. The DAC has two output channels, each with an independent converter, to operate in the dual DAC mode. In this mode, the outputs of the 2 channels can be updated synchronously and the conversion of these 2 channels can be performed simultaneously or separately.

Main characteristics of DAC:

- Two DAC converters: one converter for one output channel
- 8-bit or 12-bit monotonic output
- Left- or right-aligned data in 12-bit mode
- Synchronous update function
- Noise waveform generation
- Triangle waveform generation
- Simultaneous or separate conversion of dual DAC channels
- DMA function for each channel
- External trigger conversion

2.2.25 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.26 Serial single line SWD debug port (SW-DP)

Built-in Arm two-wire serial debug port (SW-DP) and Single line (JTAG).

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

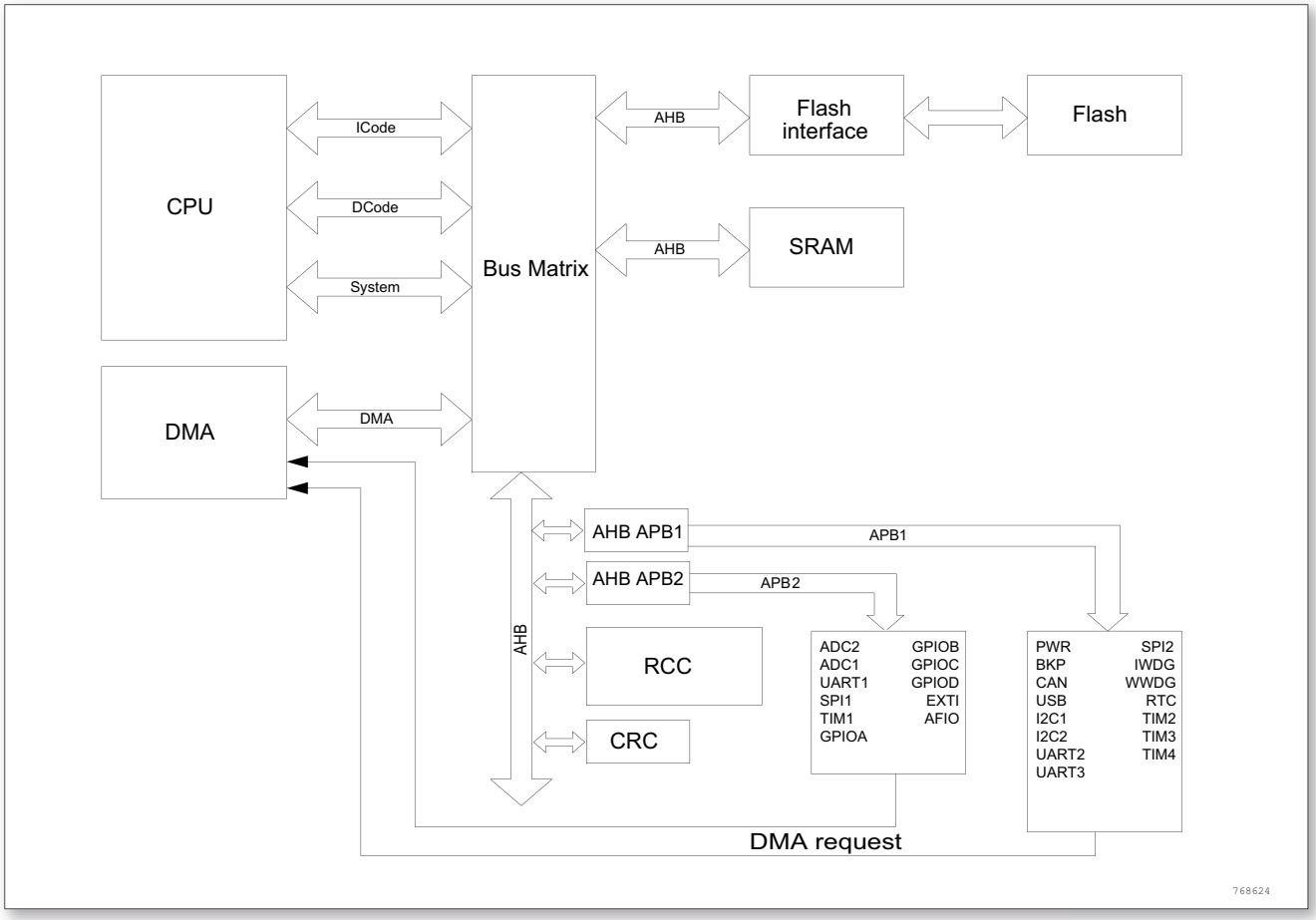

Figure 1. Block diagram

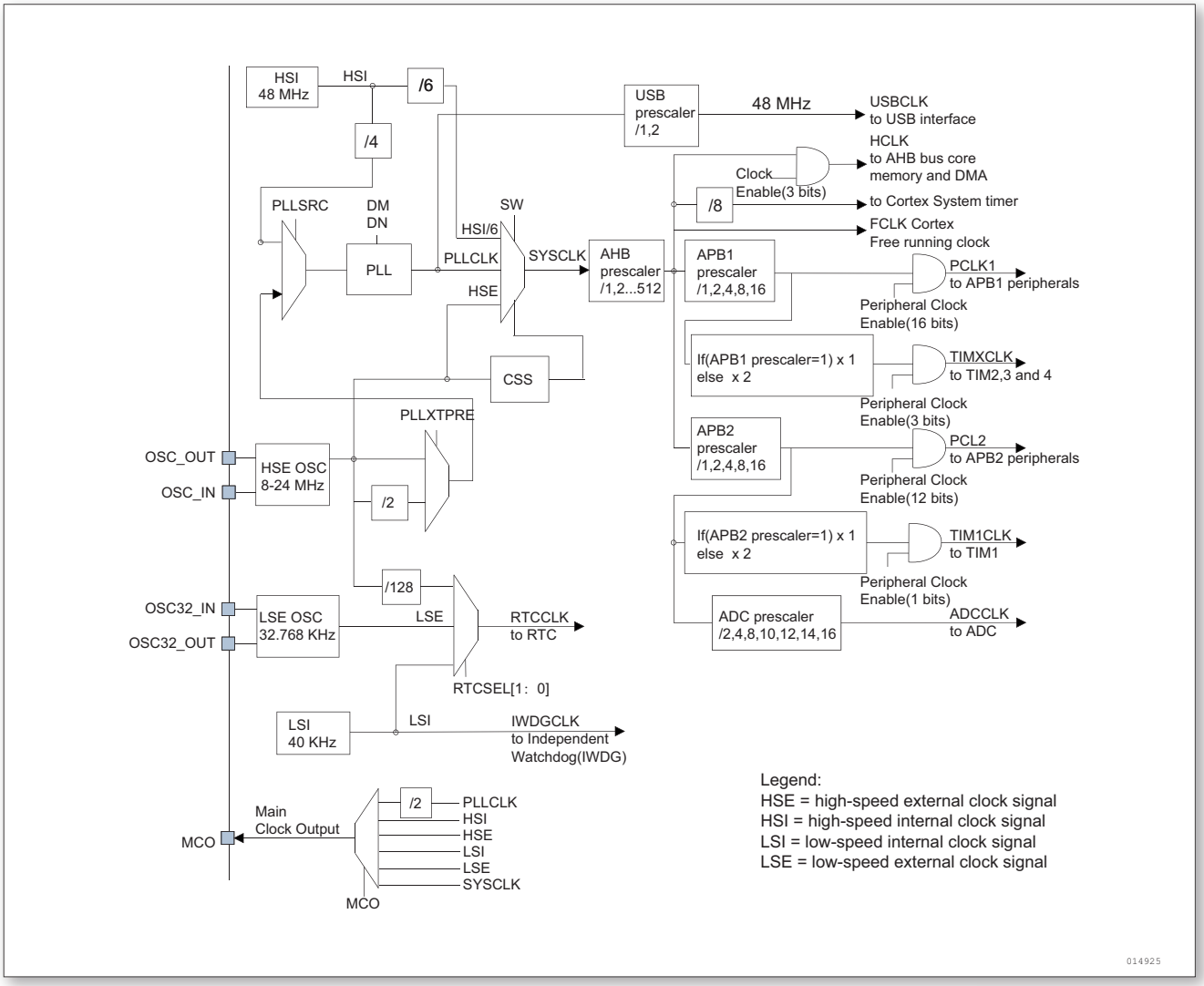

Figure 2. Clock tree

3 Pin definition

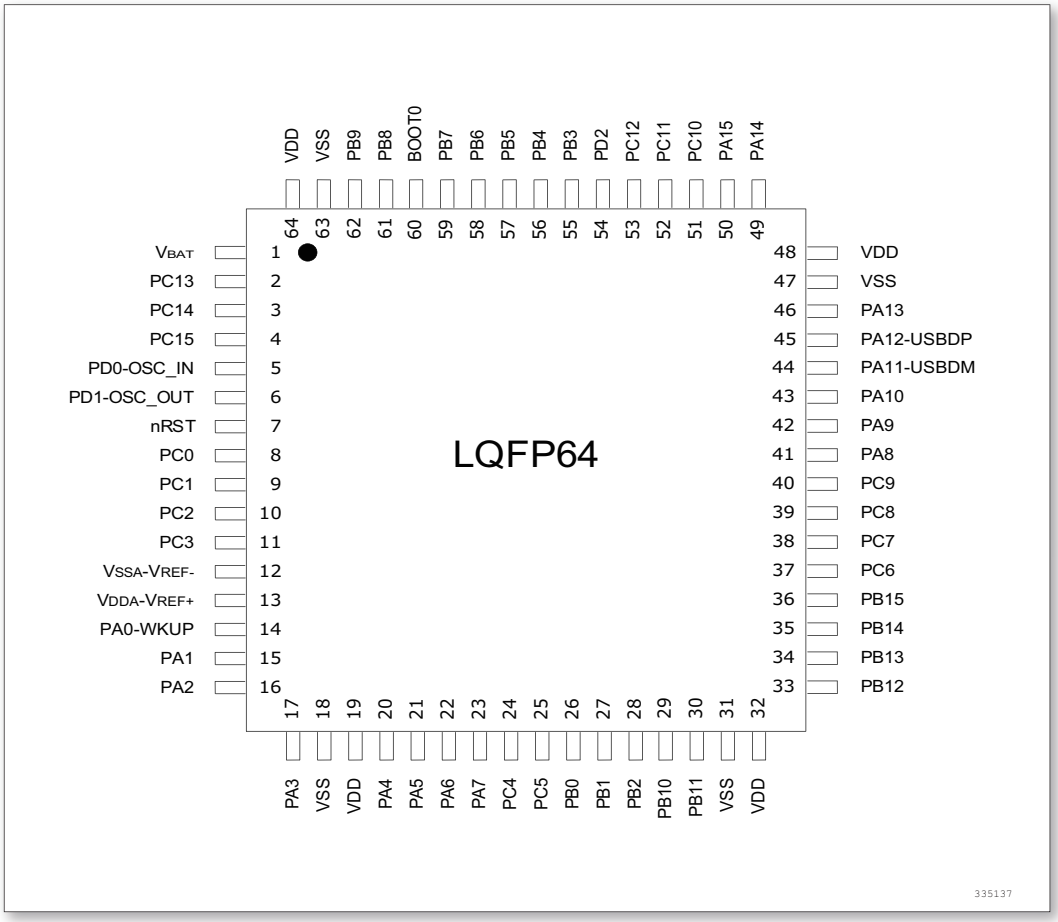

Figure 3. LQFP64 package pinout

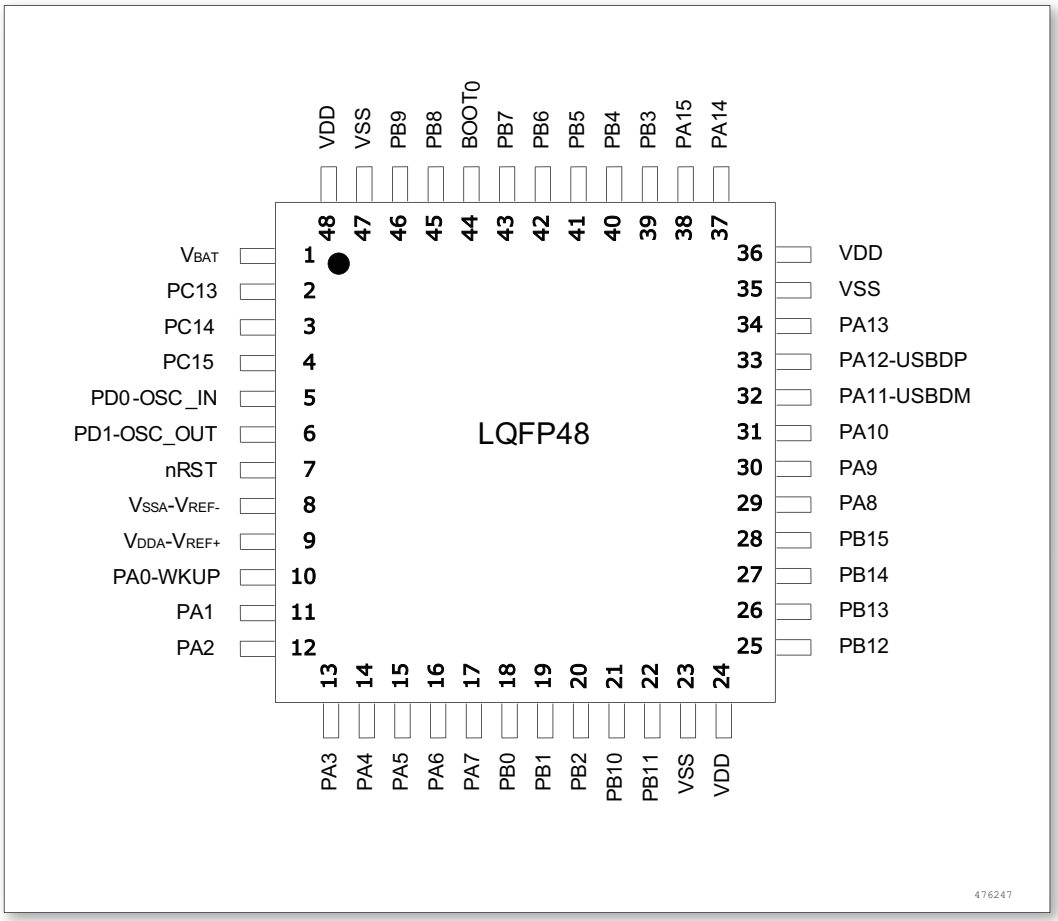

Figure 4. LQFP48 package pinout

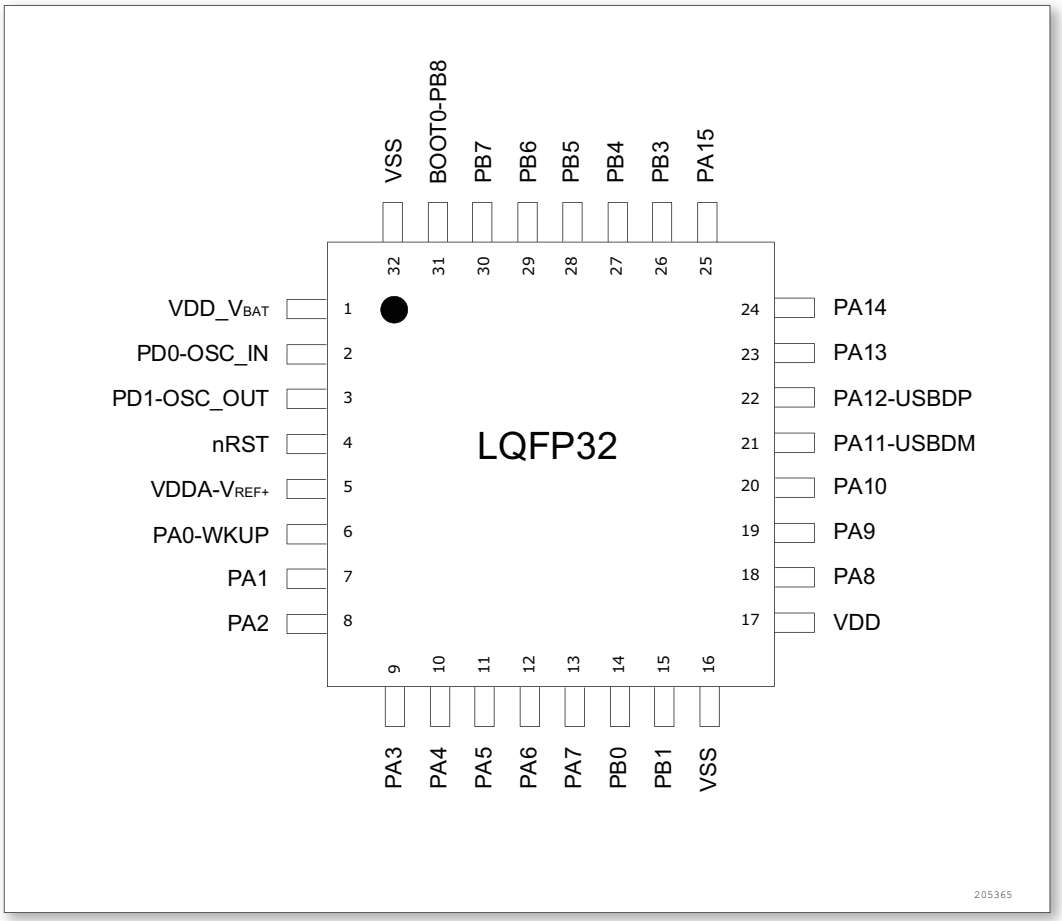

Figure 5. LQFP32 package pinout

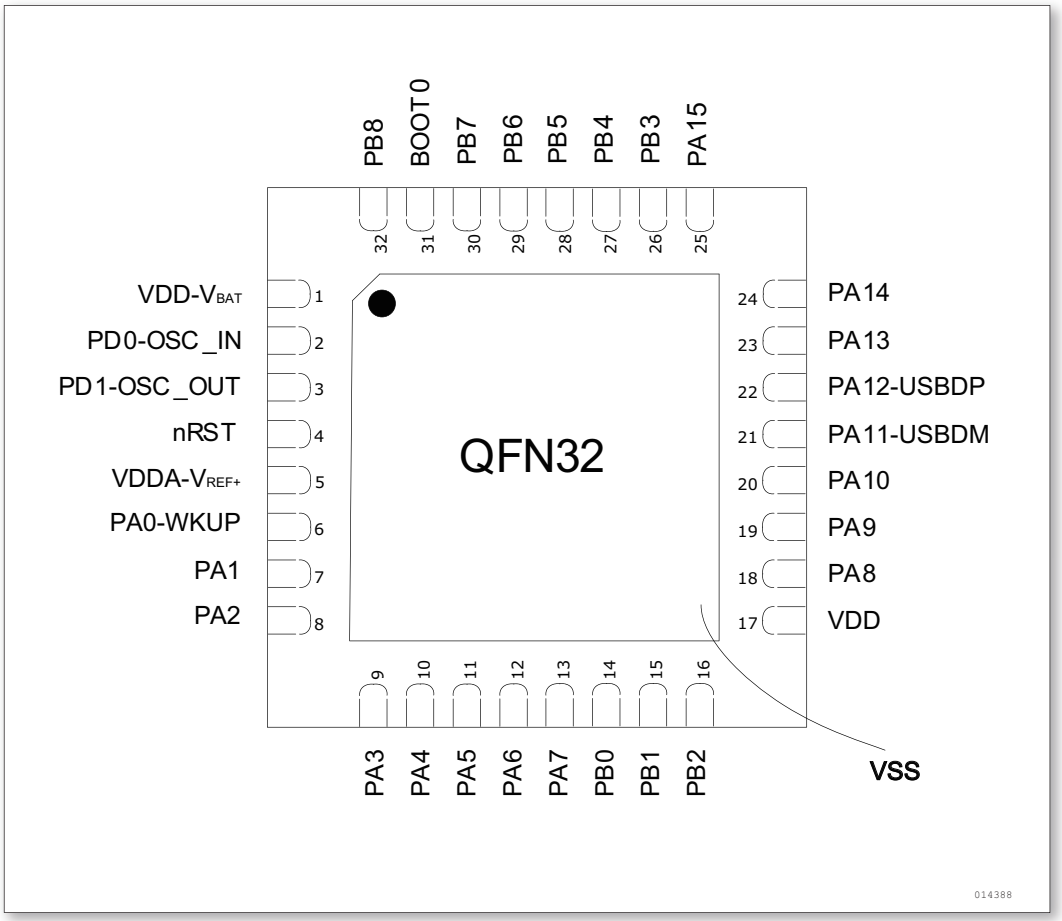

Figure 6. QFN32 package pinout

Table 4. Pin definition

Pin code				Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	LQFP 32	QFN 32						
1	1	-	-	V_{BAT}	S	-	V_{BAT}	-	-
2	2	-	-	PC13-TAMPER-RTC	I/O	-	PC13	TAMPER-RTC	-
3	3	-	-	PC14-OSC32_IN	I/O	-	PC14	OSC32_IN	-
4	4	-	-	PC15-OSC32_OUT	I/O	-	PC15	OSC32_OUT	-
5	5	2	2	PD0-OSC_IN	I/O	-	OSC_IN	-	-
6	6	3	3	PD1-OSC_OUT	I/O	-	OSC_OUT	-	-
7	7	4	4	nRST	I/O	-	nRST	-	-
8	-	-	-	PC0	I/O	-	PC0	ADC2_VIN[2]	-
9	-	-	-	PC1	I/O	-	PC1	ADC2_VIN[3]	-

Pin code				Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	LQFP 32	QFN 32						
10	-	-	-	PC2	I/O	-	PC2	ADC2_VIN[4]	-
11	-	-	-	PC3	I/O	-	PC3	ADC2_VIN[5]	-
12	8	-	-	V_{SSA}	S	-	V_{SSA}	-	-
13	9	5	5	V_{DDA}	S	-	V_{DDA}	-	-
14	10	6	6	PA0-WKUP	I/O	-	PA0	ADC1_VIN[0]/ WKUP/ UART2_CTS/ TIM2_CH1_ETR	-
15	11	7	7	PA1	I/O	-	PA1	ADC1_VIN[1]/ UART2_RTS/ TIM2_CH2	-
16	12	8	8	PA2	I/O	-	PA2	ADC1_VIN[2]/ UART2_TX/ TIM2_CH3	-
17	13	9	9	PA3	I/O	-	PA3	ADC1_VIN[3]/ UART2_RX/ TIM2_CH4	-
18	-	-	0	VSS	S	-	VSS	-	-
19	-	1	0	VDD	S	-	VDD	-	-
20	14	10	10	PA4	I/O	-	PA4	ADC1_VIN[4]/ DAC1_OUT/ SPI1_NSS	-
21	15	11	11	PA5	I/O	-	PA5	ADC1_VIN[5]/ DAC2_OUT/ SPI1_SCK	-
22	16	12	12	PA6	I/O	-	PA6	ADC1_VIN[6]/ SPI1_MISO/ TIM3_CH1	TIM1_BKIN
23	17	13	13	PA7	I/O	-	PA7	ADC1_VIN[7]/ SPI1_MOSI/ TIM3_CH2	TIM1_CH1N
24	-	-	-	PC4	I/O	-	PC4	ADC2_VIN[6]	-
25	-	-	-	PC5	I/O	-	PC5	ADC2_VIN[7]	-
26	18	14	14	PB0	I/O	-	PB0	ADC2_VIN[0]/ TIM3_CH3	TIM1_CH2N
27	19	15	15	PB1	I/O	-	PB1	ADC2_VIN[1]/ TIM3_CH4	TIM1_CH3N

Pin code				Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	LQFP 32	QFN 32						
28	20	-	16	PB2	I/O	FT	PB2/ BOOT1	-	-
29	21	-	-	PB10	I/O	FT	PB10	I2C2_SCL/ UART3_TX	TIM2_CH3
30	22	-	-	PB11	I/O	FT	PB11	I2C2_SDL/ UART3_RX	TIM2_CH4
31	23	16	0	VSS	S	-	VSS	-	-
32	24	17	17	VDD	S	-	VDD	-	-
33	25	-	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ TIM1_BKIN	-
34	26	-	-	PB13	I/O	FT	PB13	SPI2_SCK/ UART3_CTS/ TIM1_CH1N	-
35	27	-	-	PB14	I/O	FT	PB14	SPI2_MISO/ UART3_RTS/ TIM1_CH2N	-
36	28	-	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N	-
37	-	-	-	PC6	I/O	FT	PC6	-	TIM3_CH1
38	-	-	-	PC7	I/O	FT	PC7	-	TIM3_CH2
39	-	-	-	PC8	I/O	FT	PC8	-	TIM3_CH3
40	-	-	-	PC9	I/O	FT	PC9	-	TIM3_CH4
41	29	18	18	PA8	I/O	FT	PA8	TIM1_CH1/ MCO	-
42	30	19	19	PA9	I/O	FT	PA9	UART1_TX/ TIM1_CH2	-
43	31	20	20	PA10	I/O	FT	PA10	UART1_RX/ TIM1_CH3	-
44	32	21	21	PA11/ USBDM	I/O	FT	PA11	UART1_CTS/ CAN_RX/ TIM1_CH4	-
45	33	22	22	PA12/ USBDP	I/O	FT	PA12	UART1_RTS/ CAN_TX/ TIM1_ETR	-
46	34	23	23	PA13	I/O	FT	JTM/ SWDIO	-	PA13

Pin code				Pin name	Type(1)	I/O level(2)	Main function	Alternate function	Additional function
LQFP 64	LQFP 48	LQFP 32	QFN 32						
47	35	32	0	VSS	S	-	VSS	-	-
48	36	-	-	VDD	S	-	VDD	-	-
49	37	24	24	PA14	I/O	FT	JTCK/ SWCLK	-	PA14
50	38	25	25	PA15	I/O	FT	JTDI	-	PA15/ TIM2_CH1 _ETR/ SPI1_NSS
51	-	-	-	PC10	I/O	FT	PC10	-	UART3_TX
52	-	-	-	PC11	I/O	FT	PC11	-	UART3_RX
53	-	-	-	PC12	I/O	FT	PC12	-	-
54	-	-	-	PD2	I/O	FT	PD2	TIM3_ETR	-
55	39	26	26	PB3	I/O	FT	JTDO	-	PB3/ TRACESWO/ TIM2_CH2/ SPI1_SCK
56	40	27	27	PB4	I/O	FT	NJTRST	-	PB4/ TIM3_CH1/ SPI1_MISO
57	41	28	28	PB5	I/O	-	PB5	I2C1_SMBAI	TIM3_CH2/ SPI1_MOSI
58	42	29	29	PB6	I/O	FT	PB6	I2C1_SCL/ TIM4_CH1	UART1_TX
59	43	30	30	PB7	I/O	FT	PB7	I2C1_SDA/ TIM4_CH2	UART1_RX
60	44	31	31	BOOT0	I	-	BOOT0	-	-
61	45	31	32	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL/ CAN_RX
62	46	-	-	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA/ CAN_TX
63	47	32	0	VSS	S	-	VSS	-	-
64	48	-	-	VDD	S	-	VDD	-	-

1. I = Input, O = Output，S = Power Supply, HiZ = High Resistance
2. FT: 5V tolerant

4 Memory mapping

Memory mapping

Table 5. Memory mapping

Bus	Address range	Size	Peripheral	Notes
Flash	0x0000 0000 - 0x0001 FFFF	128KB	Main flash memory, system memory or SRAM, depending on the BOOT configuration	
	0x000 20000 - 0x07FF FFFF	~128KB	Reserved	
	0x0800 0000 - 0x0801 FFFF	128KB	Main Flash memory	
	0x0802 0000 - 0x0FFF FFFF	~128KB	Reserved	
	0x1000 0000 - 0x1000 1FFF	8KB	Reserved	
	0x1000 2000 - 0x1FFD FFFF	~256KB	Reserved	
	0x1FFE 0000 - 0x1FFE 01FF	0.5KB	Protect byte	
	0x1FFE 0200 - 0x1FFE 0FFF	3KB	Reserved	
	0x1FFE 1000 - 0x1FFE 1BFF	3KB	Security space	
	0x1FFE 1C00 - 0x1FFF F3FF	~256KB	Reserved	
	0x1FFF F400 - 0x1FFF F7FF	1KB	System memory	
	0x1FFF F800 - 0x1FFF F80F	16KB	Option bytes	
	0x1FFF F810 - 0x1FFF FFFF	~2KB	Reserved	
SRAM	0x2000 0000 - 0x2000 4FFF	20KB	SRAM	
	0x2000 5000 - 0x3FFF FFFF	~512MB	Reserved	
APB1	0x4000 0000 - 0x4000 03FF	1KB	TIM2	
	0x4000 0400 - 0x4000 07FF	1KB	TIM3	
	0x4000 0800 - 0x4000 0BFF	1KB	TIM4	
	0x4000 0C00 - 0x4000 27FF	7KB	Reserved	
	0x4000 2800 - 0x4000 2BFF	1KB	RTC	
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG	
	0x4000 3000 - 0x4000 33FF	1KB	IWWDG	
	0x4000 3400 - 0x4000 37FF	1KB	Reserved	
	0x4000 3800 - 0x4000 3BFF	1KB	SPI2	
	0x4000 3C00 - 0x4000 43FF	2KB	Reserved	
	0x4000 4400 - 0x4000 47FF	1KB	UART2	
	0x4000 4800 - 0x4000 4BFF	1KB	UART3	
	0x4000 4C00 - 0x4000 53FF	2KB	Reserved	
	0x4000 5400 - 0x4000 57FF	1KB	I2C1	
	0x4000 5800 - 0x4000 5BFF	1KB	I2C2	
	0x4000 5C00 - 0x4000 5FFF	1KB	USB	

Bus	Address range	Size	Peripheral	Notes
APB1	0x4000 6000 - 0x4000 63FF	1KB	Reserved	
	0x4000 6400 - 0x4000 67FF	1KB	CAN	
	0x4000 6800 - 0x4000 6BFF	1KB	Reserved	
	0x4000 6C00 - 0x4000 6FFF	1KB	Backup register (BKP)	
	0x4000 7000 - 0x4000 73FF	1KB	Power control (PWR)	
	0x4000 7400 - 0x4000 77FF	34KB	Reserved	
	0x4000 7800 - 0x4000 FFFF	34KB	Reserved	
APB2	0x4001 0000 - 0x4001 03FF	1KB	AFIO	
	0x4001 0400 - 0x4001 07FF	1KB	EXTI	
	0x4001 0800 - 0x4001 0BFF	1KB	GPIOA	
	0x4001 0C00 - 0x4001 0FFF	1KB	GPIOB	
	0x4001 1000 - 0x4001 13FF	1KB	GPIOC	
	0x4001 1400 - 0x4001 17FF	1KB	GPIOD	
	0x4001 1800 - 0x4001 1BFF	1KB	Reserved	
	0x4001 1C00 - 0x4001 23FF	2KB	Reserved	
	0x4001 2400 - 0x4001 27FF	1KB	ADC1	
	0x4001 2800 - 0x4001 2BFF	1KB	ADC2	
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1	
	0x4001 3000 - 0x4001 33FF	1KB	SPI1	
	0x4001 3400 - 0x4001 37FF	1KB	Reserved	
	0x4001 3800 - 0x4001 3BFF	1KB	UART1	
	0x4001 3C00 - 0x4001 3FFF	1KB	Reserved	
	0x4001 4000 - 0x4001 43FF	1KB	Reserved	
	0x4001 4400 - 0x4001 47FF	1KB	Reserved	
	0x4001 4800 - 0x4001 4BFF	1KB	Reserved	
	0x4001 4C00 - 0x4001 7FFF	13KB	Reserved	
	0x4001 8000 - 0x4001 FFFF	32KB	Reserved	
AHB	0x4002 0000 - 0x4002 03FF	1KB	DMA	
	0x4002 0400 - 0x4002 0FFF	3KB	Reserved	
	0x4002 1000 - 0x4002 13FF	1KB	Reset and clock control (RCC)	
	0x4002 1400 - 0x4002 1FFF	3KB	Reserved	
	0x4002 2000 - 0x4002 23FF	1KB	Flash interface	
	0x4002 2400 - 0x4002 2FFF	3KB	Reserved	
	0x4002 3000 - 0x4002 33FF	1KB	CRC	
	0x4002 3400 - 0x4002 43FF	4KB	Reserved	

5 Electrical characteristics

Electrical characteristics

5.1 Test condition

All voltages are based on V_{SS} unless otherwise stated.

5.1.1 Minimum and maximum

Unless otherwise stated, the minimum and maximum performed at ambient temperature T_A = 25°C,V_{DD} = 3.3V.

5.1.2 Typical value

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and have not been tested.

5.1.3 Typical curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

5.1.4 Load capacitor

The load conditions when measuring the pin parameters are shown in the figure below.

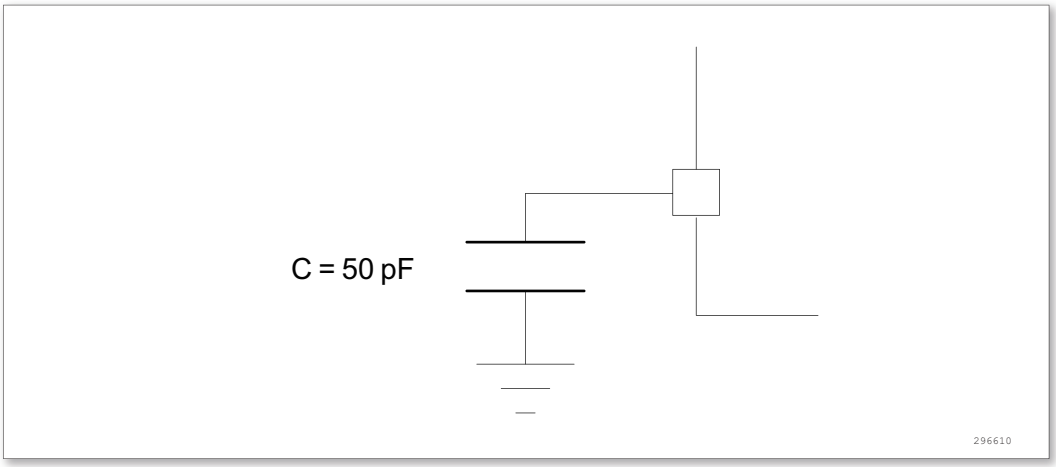

Figure 7. Load condition of the pin

5.1.5 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below.

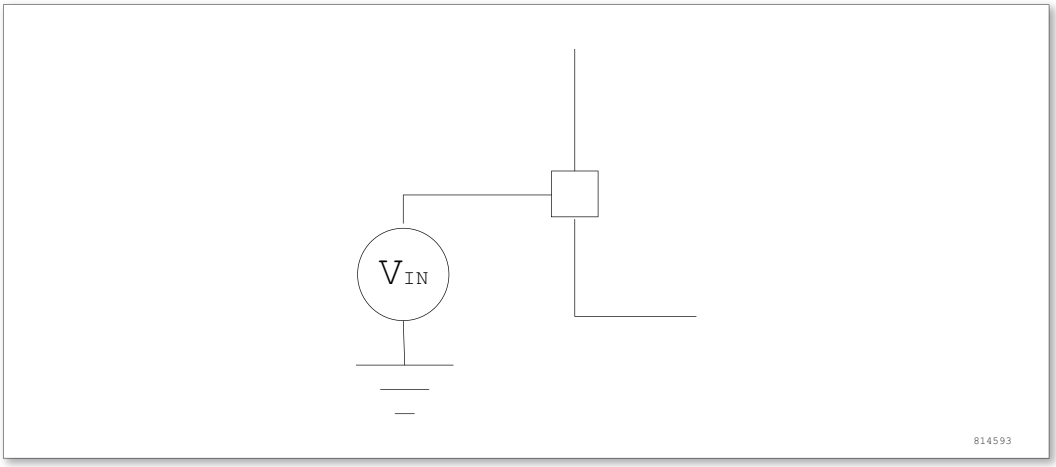

Figure 8. Pin input voltage

5.1.6 Power scheme

The power supply design scheme is shown in the figure below.

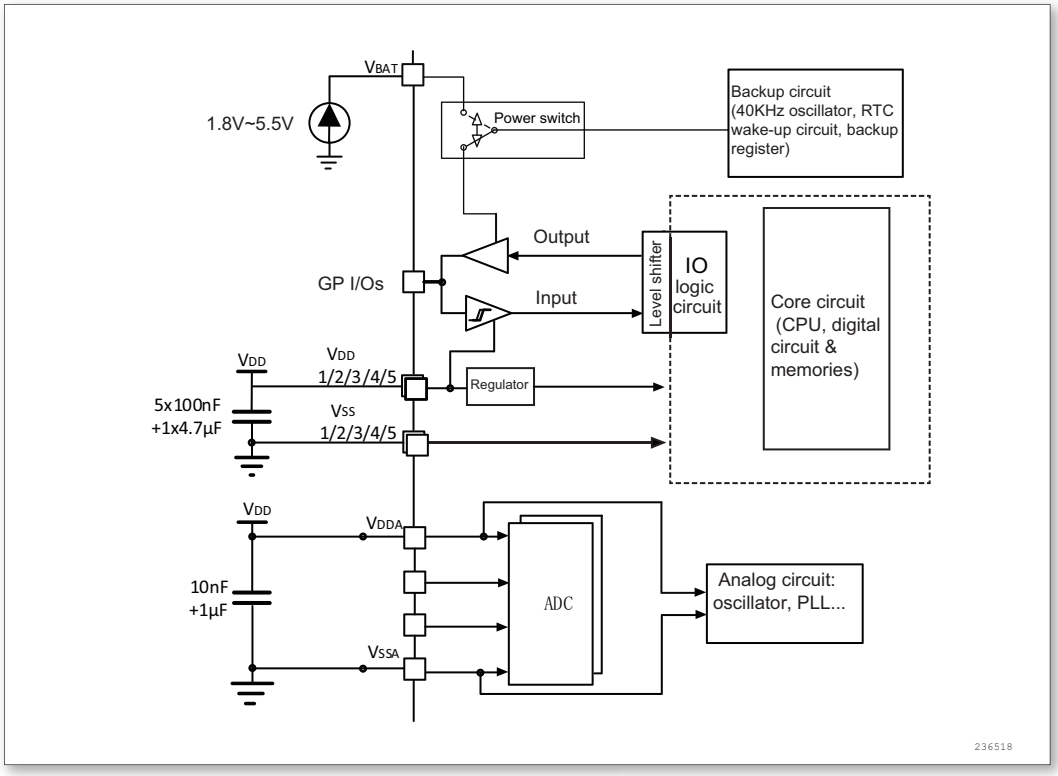

Figure 9. Powering scheme

5.1.7 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

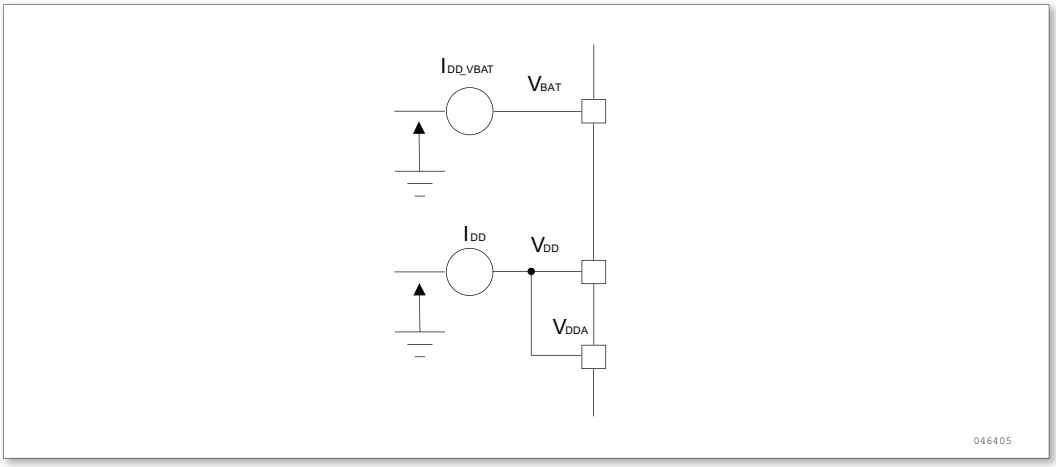

Figure 10. Current consumption measurement scheme

5.2 Absolute maximum rating

If the load applied to the device exceeds the value given in the ”Absolute Group Maximum Ratings” list (Table 6, Table 7), it may result in that the device is permanently damaged. This is just to give the maximum load that can be tolerated, and does not mean that the functional operation of the device is correct under these conditions. Long-term operation of the device under maximum conditions can affect device reliability.

Table 6. Voltage characteristics

Symbol	Description	min	max	units
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	- 0.3	5.8	V
V_{IN}	Input voltage on the 5 Vtolerant pin (2)	V_{SS} - 0.3	5.8	
	Input voltage on other pins (2)	V_{SS} - 0.3	5.8	
$\lvert \triangle V_{DDx} \rvert$	Voltage variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage variations between different ground pins		50	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. V_{IN} maximum must always be respected. For information about the maximum allowed injected current values, please see the table below.

Table 7. Current characteristics

Symbol	Description	Maximum	Units
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (supply current) (1)	120	mA
I_{VSS}	Total current out of V_{SS} wire (outflow current) (1)	120	
I_{IO}	Output sink current on any I/O and control pins	20	
	Output current on any I/O and control pins	-18	
$I_{INJ(PIN)}$ (2)(3)	Injection current on NRST pin	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injection current on OSC_IN pin of HSE and OSC_IN pin LSE	±5	mA
$I_{INJ(PIN)}$ (2)(3)	injection current on other pins (4)	±5	mA
$\Sigma I_{INJ(PIN)}$ (2)	Total injection current on all I/O and control pins (4)	±25	mA

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range.
2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/sourced between two consecutive power pins of the referenced high-pin LQFP package.
3. The reverse injection current can interfere with the analog performance of the device.
4. A positive injection current is induced by $V_{IN} > V_{DDA}$ while a negative injection current is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$must never be exceeded.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

Table 8. Temperature characteristics

Symbol	Description	Maximum	Units
T_{STG}	Storage Temperature Range	- 45 ~ + 150	°C
T_J	maximum junction temperature	125	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Standard operating voltage		2.0	5.5	V
V_{DDA} (1)	Analog operating voltage (ADC not used)	Must be the same voltage as V_{DD}	2.0	5.5	mW
	Analog operating voltage (ADC used)		2.0	5.5	
T_A (2)	T_A=25°C	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (See subsec 5.1).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (See subsec 5.1).

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 10. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{VDD} rise time rate	T_A = 25°C	300	∞	μS/V
	V_{VDD} fall time rate		300	∞	

1. All power-ups need to start at 0V, to ensure that the chip can be powered up reliably.

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 9.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)		1.82		V
		PLS[3：0]=0000 (Falling edge)		1.71		V
		PLS[3：0]=0001 (Rising edge)		2.12		V
		PLS[3：0]=0001 (Falling edge)		2.00		V
		PLS[3：0]=0010 (Rising edge)		2.41		V
		PLS[3：0]=0010 (Falling edge)		2.30		V
		PLS[3：0]=0011 (Rising edge)		2.71		V
		PLS[3：0]=0011 (Falling edge)		2.60		V
		PLS[3：0]=0100 (Rising edge)		3.01		V
		PLS[3：0]=0100 (Falling edge)		2.90		V
		PLS[3：0]=0101 (Rising edge)		3.31		V
		PLS[3：0]=0101 (Falling edge)		3.19		V
		PLS[3：0]=0110 (Rising edge)		3.61		V
		PLS[3：0]=0110 (Falling edge)		3.49		V
		PLS[3：0]=0111 (Rising edge)		3.91		V
		PLS[3：0]=0111 (Falling edge)		3.79		V
		PLS[3：0]=1000 (Rising edge)		4.21		V
		PLS[3：0]=1000 (Falling edge)		4.09		V
		PLS[3：0]=1001 (Rising edge)		4.51		V
		PLS[3：0]=1001 (Falling edge)		4.39		V
		PLS[3：0]=1010 (Rising edge)		4.81		V
		PLS[3：0]=1010 (Falling edge)		4.69		V
$V_{PVDhyst}$ (2)	PVD hysteresis			110		mV
$V_{POR/PDR}$ (1)	Power on/down reset threshold			1.66		V
$T_{RSTTEMPO}$ (2)	Reset duration			0.61		ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

5.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting period).
- The instruction prefetching function is on. When the peripherals are enabled：f_{HCLK} = f_{PCLK1}= f_{PCLK2}.

Note：The instruction prefetching function must be set before setting the clock and bus divider.

Table 12. Typical current consumption in Stop and Standby mode(2)

Symbol	Parameter	Conditions	Typical	Unit
			T_A=25°C	
I_{DD}	Supply current in Stop mode	Enter the stop mode after reset	402	μA
	Supply current in Standby mode	Enter the standby mode after reset	0.4	

1. The maximum value is tested at T_A = 25°C.
2. Drawn from comprehensive evaluation, not tested in production. IO status is analog input.

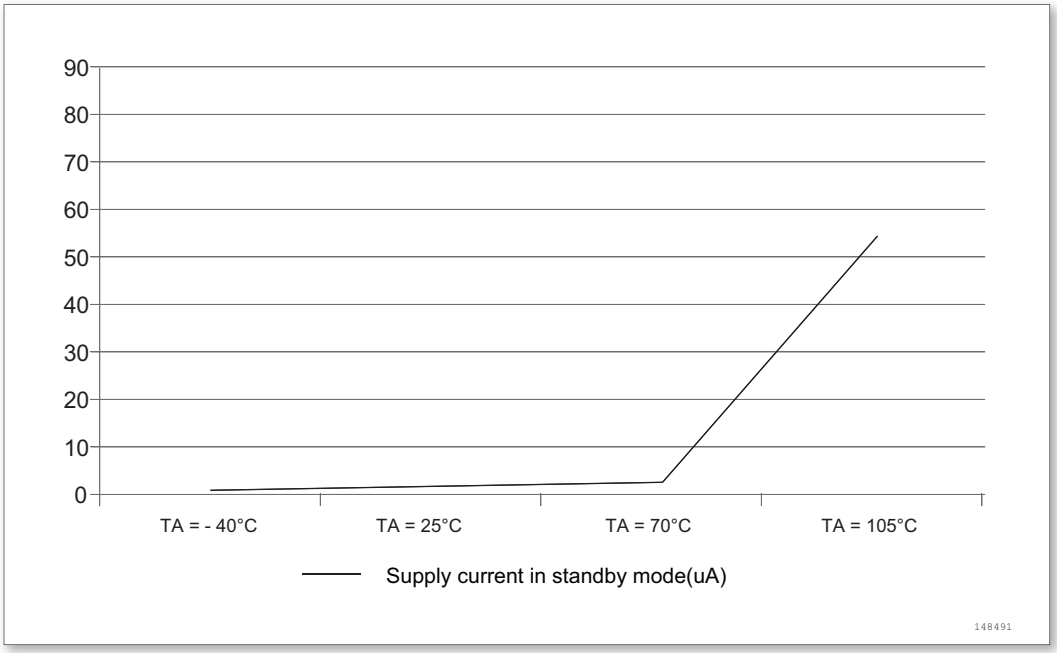

Figure 11. Typical current consumption in standby mode vs. temperature at V_{DD} = 3.3V

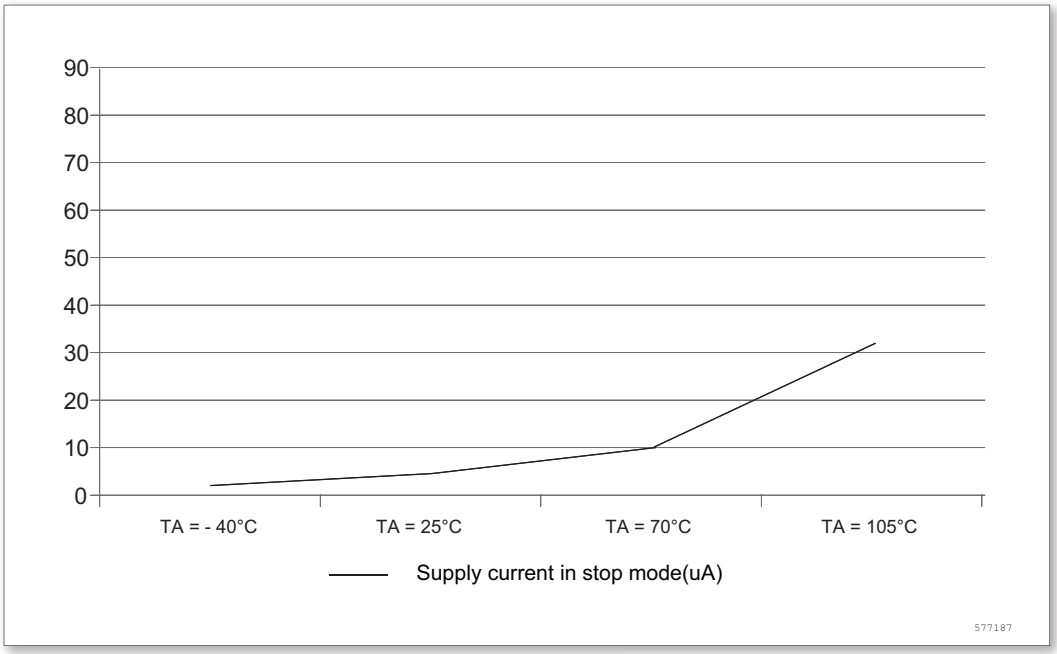

Figure 12. Typical current consumption in stop mode vs. temperature at V_{DD} = 3.3V

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration, and are connected to a static level —- V_{DD} or V_{SS} (no load).
- All the peripherals are closed, unless otherwise specified.
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHzis 2 waiting period).

- The ambient temperature and V_{DD} supply voltage conditions are summarized in Table 9.
- The instruction prefetching function is on. When the peripherals are enabled：
  $f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetch function must be set before the clock is set and the bus is divided.

Table 13. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(2)	96MHz	26.23	15.2	mA
			72MHz	20.52	12.19	
			48MHz	14.71	9.13	
			36MHz	11.76	7.58	
			24MHz	8.84	6.03	
			8MHz	4.1	3.14	

1. The typical value is tested at T_A = 25°C, V_{DD}=3.3V.

Table 14. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(2)	96MHz	22.41	10.92	mA
			72MHz	17.57	8.96	
			48MHz	12.68	6.96	
			36MHz	10.29	5.95	
			24MHz	7.79	4.9	
			8MHz	3.46	2.8	

1. The typical value is tested at T_A = 25°C.
2. External clock is 8MHz, when f_{HCLK} > 8MHz, choose HSI 48MHz or HSI 72MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 15. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load) .
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
  - With all peripherals clocked OFF
  - With only one peripheral clocked on

- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 9.

Table 15. On-chip peripheral current consumption(1)

On-chip Peripheral		Typical power consumption at 25 °C	Unit	On-chip Peripheral		Typical power consumption at 25 °C	Unit
APB1	TIM2	0.098	mA	APB2	GPIOA	0.045	mA
	TIM3	0.062			GPIOB	0.046	
	TIM4	0.055			GPIOC	0.052	
	SPI2	0.133			GPIOD	0.046	
	UART2	0.077			ADC1	0.051	
	UART3	0.078			ADC2	0.052	
	I2C1	0.132			TIM1	0.121	
	I2C2	0.134			SPI1	0.122	
	USB	0.058			UART1	0.078	
	CAN	0.033					

1. f_{HCLK} = 96MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescale coefficient for each device is the default value.

5.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of general operating conditions.

Table 16. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3V_{DD}	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$	OSC_IN rise time(1)				20	ns
$t_{f(HSE)}$	OSC_IN fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	μA

1. Guaranteed by design, not tested in production.

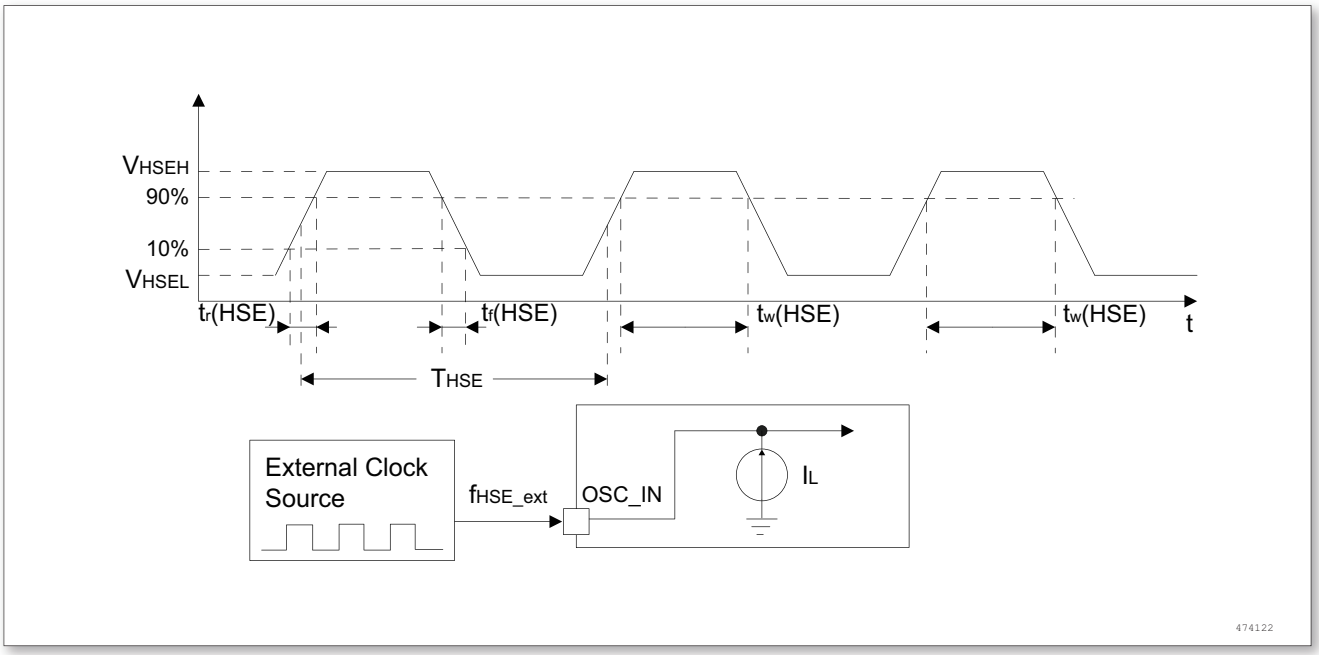

Figure 13. High-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 2 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 17. HSE 8~24MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	24	MHz
R_F	Feedback resistor			1000		kΩ
C_{L1}/ C_{L2}(3)	The proposed load capacitance corresponds to the crystal serial impedance (R_S) (4)	R_S = 30Ω		30		pF
I_2	HSE current consumption	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF load			4.5	mA
g_m	Oscillator transconductance	Startup		8.5		mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized		3		mS

1. The characteristic parameters of the resonator are given by the crystal/ceramic res-

onator manufacturer.

2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF (typical value) range, designed for high-frequency applications. A suitable crystal or resonator should also be carefully selected. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer typically specifies a load capacitance which is the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the combined pin and the PCB board capacitance can be roughly estimated as 10pF).
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment the software enables HSE to a stable 8MHz oscillation is obtained. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

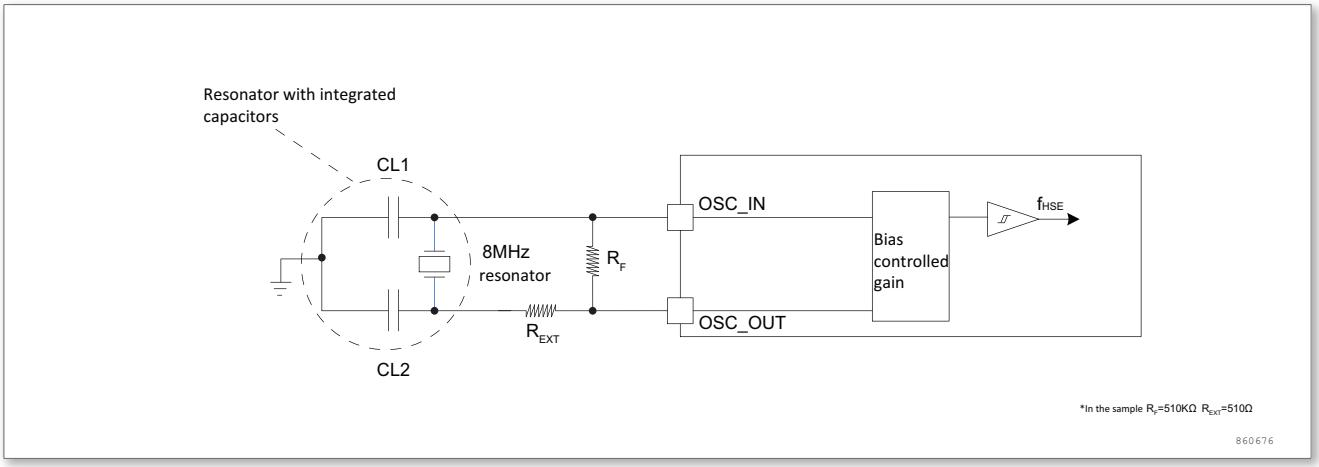

Figure 14. Typical application with an 8 MHz crystal

5.3.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 18. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency		40	48	64	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40°C ~ 105°C	-10		10	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -10°C ~ 85°C	-3		3	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 0°C ~ 70°C	-2		2	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25 °C	-1		1	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(HSI)}$	HSI oscillator startup time			2		μS
$I_{DD(HSI)}$	HSI oscillator power consumption		81	200		μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 19. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency		31	40	75	KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				100	μS
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1.1	1.7	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, Unless otherwise stated
2. Drawn from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 20. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	HSI clock wakeup	4.2	μS
t_{WUSTOP}(1)	Wakeup from Stop mode (The regulator is in run mode)	HSI clock wakeup < 2μS	12	

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI clock wakeup < 2μS The regulator wakes up from the off mode < 38μS	230	mS

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

5.3.7 Memory characteristics

Flash memory

Table 21. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	8-bit programming time	T_A = -40°C ~ 125°C	4			μS
t_{ERASE}	Page (512K bytes) erase time	T_A = -40°C ~ 125°C		4	5	mS
t_{ME}	Mass erase time	T_A = -40°C ~ 125°C	20		40	mS

Table 22. Flash memory endurance and data retention(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (erase time)		20			K cycle
t_{RET}	Data retention	T_A = 105°C	20			Year
		T_A = 25°C	100			

1. Guaranteed by design, not tested in production.
2. Cycle tests are carried out in the whole temperature range.

5.3.8 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC61000-4-2 standard.
- FTB：A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table. They are based on the EMS levels and classes defined in application note.

Table 23. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V, T_A=25°C, f_{HCLK}=48MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.9 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are

applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JEDECJS-001-2017/JS-002-2018standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 24. ESD characteristics

Symbol	Parameter	Conditions	Type	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, Conforming to JS-001 -2017		±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, Conforming to JS-002-2018		±500	
I_{LU}	Latch-up current	T_A = 25°C, Conforming to JESD78E		±200	mA

5.3.10 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 6 are derived from tests. All I/O ports are compatible with CMOS.

Table 25. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	2.5V< V_{DD} < 5.5V			0.3*V_{DD}	V
V_{IH}	Input high level voltage	2.5V< V_{DD} < 5.5V	0.7*V_{DD}			V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis(1)	2.5V< V_{DD} < 5.5V		0.1*V_{DD}		V
I_{lkg}	Input leakage current (2)	2.5V< V_{DD} < 5.5V	-1		1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	2.5V< V_{DD} < 5.5V	10		50	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	2.5V< V_{DD} < 5.5V	10		100	kΩ
C_{IO}	I/O pin capacitance	2.5V< V_{DD} < 5.5V			10	pF

1. Schmitt Trigger switching hysteresis voltage level. Data drwan from comprehensive evaluation, not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
3. Pull-up and pull-down resistors are MOS resistors.

All I/Os are CMOS (no software configuration required). Their characteristics cover more than the strict CMOS-technology.

- For V_{IH}:
  - If V_{DD} is between [2.50V~ 3.08V]; use CMOS features.
  - If V_{DD} is between [3.08V~ 3.60V]; include CMOS.
- For V_{IL}:
  - Use CMOS features.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 5.2:

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition Table 6. All I/O ports are CMOS compatible.

Table 26. Output voltage characteristics

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)(3)	Output high level voltage		2.60			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			0.8	V
	V_{OH} (2)(3)	Output high level voltage		2.00			V
10	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.60	V
	V_{OH} (2)	Output high level voltage		2.40			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.80	V
	V_{OH} (2)(3)	Output high level voltage		2.20			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			3.00	V
	V_{OH} (2)(3)	Output high level voltage					V
01	V_{OL} (1)	Output low level voltage	$\|I_{IO}\|$ = 6mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)	Output high level voltage		2.80			V
	V_{OL} (1)(3)	Output low level voltage	$\|I_{IO}\|$ = 8mA V_{DD} = 3.3V			0.40	V
	V_{OH} (2)(3)	Output high level voltage		2.60			V
	V_{OL} (2)(3)	Output low level voltage	$\|I_{IO}\|$ = 20mA V_{DD} = 3.3V			0.80	V
	V_{OH} (2)(3)	Output high level voltage		2.00			V

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 15

and Table 27, respectively.

Unless otherwise stated, the parameters listed in Table 27 are measured using the ambient temperature and supply voltage in accordance with the condition Table 6.

Table 27. I/O AC characteristics (1)

SPEED[1：0]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	tf	Fall time from high level output to low level output	C_L=50pF, V_{DD}=3.3V		4.0		ns
	tr	Rise time from low level output to high level output			7.4		ns
10	tf	Fall time from high level output to low level output			10.1		ns
	tr	Rise time from low level output to high level output			16.9		ns
01	tf	Fall time from high level output to low level output			9.7		ns
	tr	Rise time from low level output to high level output			13.4		ns

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.
2. The maximum frequency is defined in figure 15.

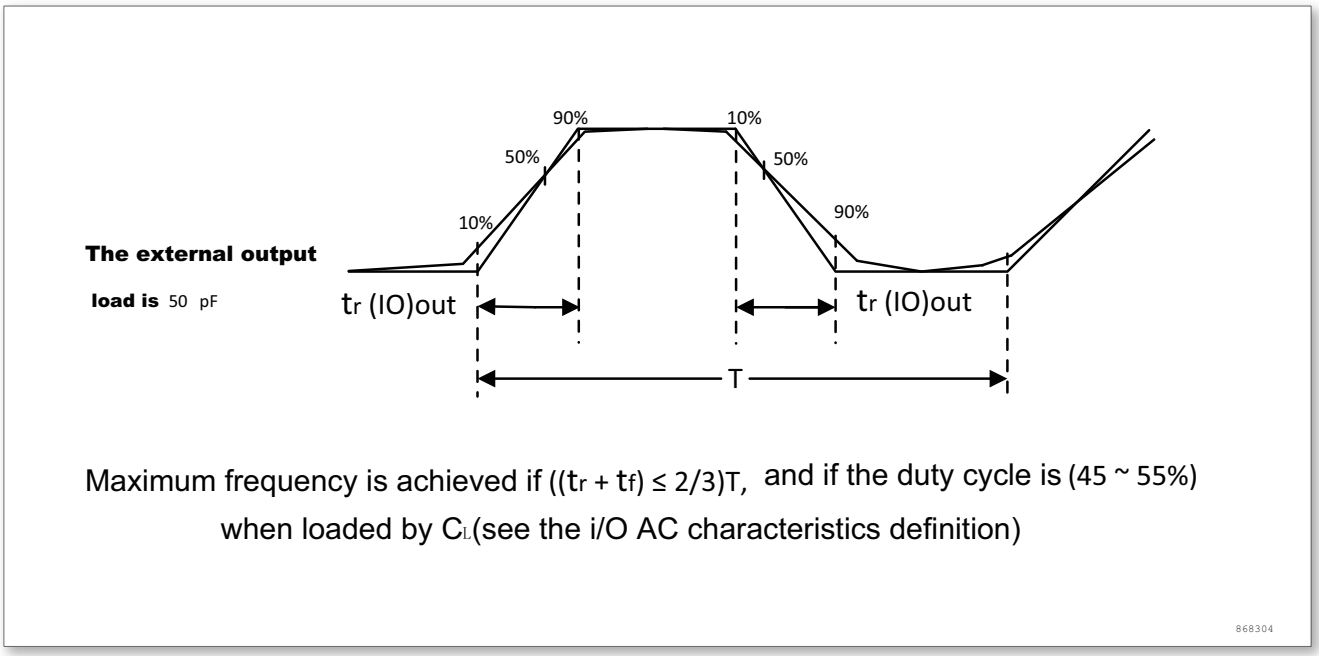

Figure 15. I/O AC characteristics

5.3.11 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition Table 6.

Table 28. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.3		0.3*V_{DD}	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		0.7*V_{DD}		V_{DD}	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			0.1*V_{DD}		V
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN} = V_{SS}		15		kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse				100	ns
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor

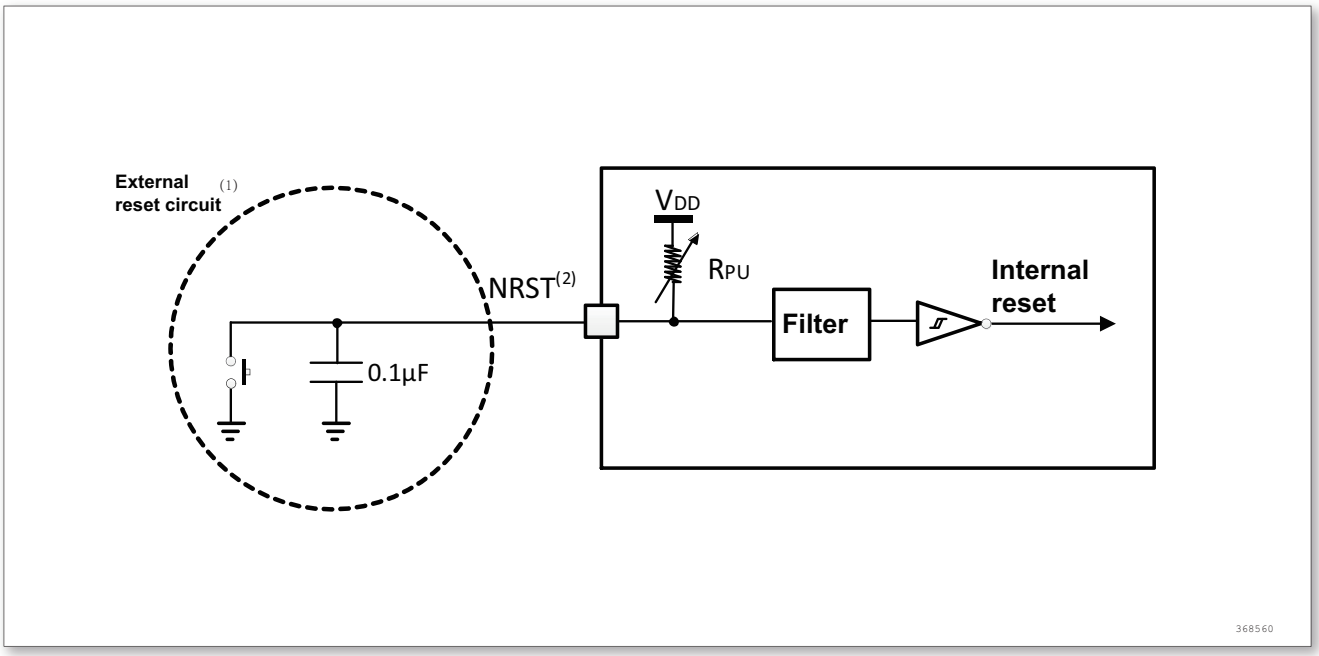

Figure 16. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 28, otherwise the MCU cannot be reset.

5.3.12 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 5.3.10.

Table 29. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24MHz	10.4		nS
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 24MHz	0	72	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16 bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24MHz	0.0139	910	µS
t_{MAX_COUNT}	The maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24MHz		59.6	S

1. TIMx is a generic name.

5.3.13 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 30 are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 9: General operating conditions.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} Was closed but still exists.

The I2C I/Os characteristics are listed in Table 30, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 5.3.10.

Table 30. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock fall time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock rise time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Repeated start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	4.7		1.3		
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300nS.

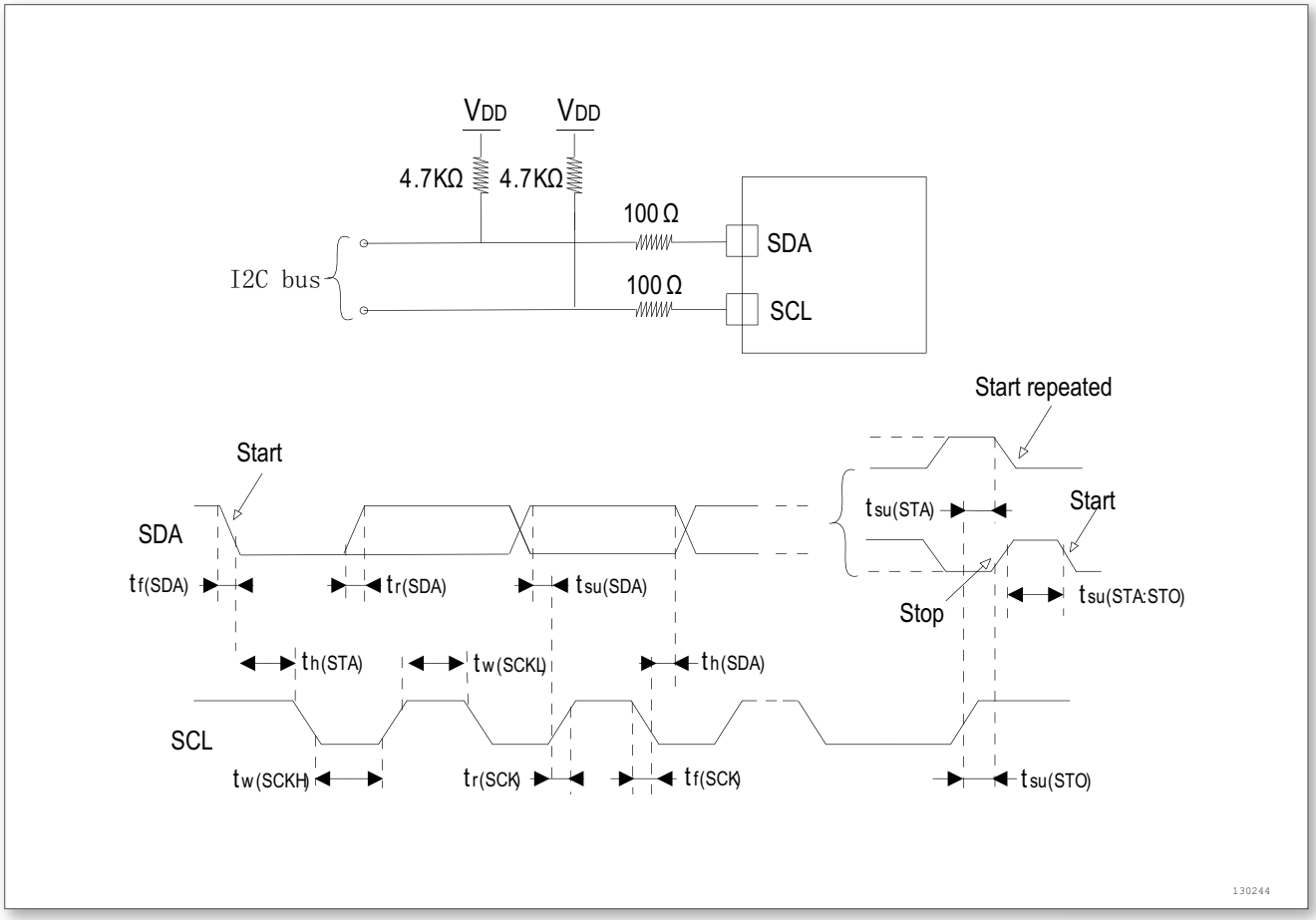

Figure 17. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 31 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 9.

Refer to subsubsec 5.3.10 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 31. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	73		ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{su(SI)}$ (2)	Data input setup time	Slave mode	1		ns
$t_{h(SI)}$ (2)	Data input hold time	Slave mode	3		ns
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	ns
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	ns
$t_{dis(SO)}$ (2)(4)	Data output disable time	Slave mode	10		ns
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	ns
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		3	ns
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	25		ns
$t_{h(MO)}$ (2)		Master mode (after enable edge)	4		ns

1. Guaranteed by design, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

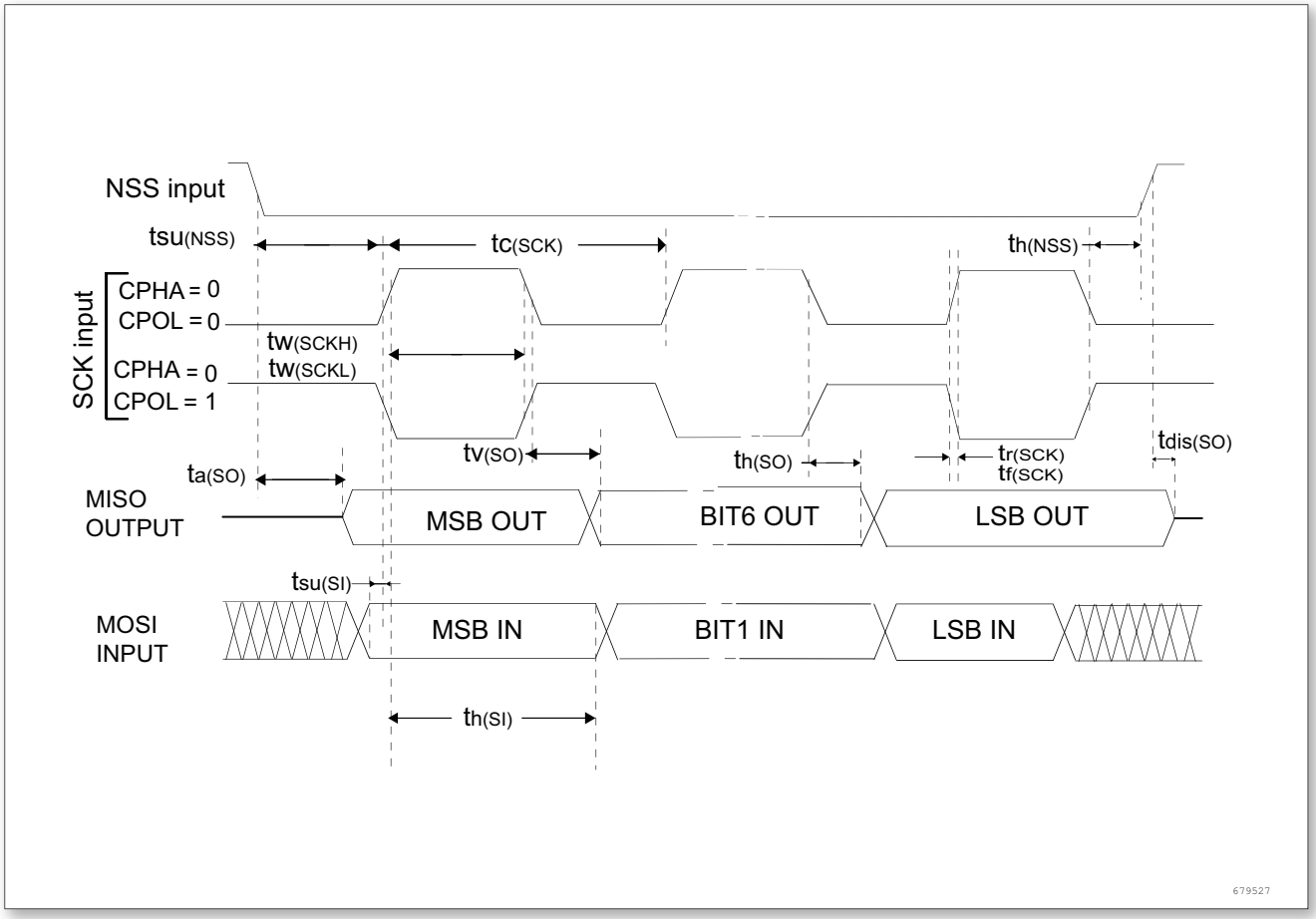

Figure 18. Slave mode and CPHA = 0,SPI_CCTL.CPHASEL=1 waveform diagram

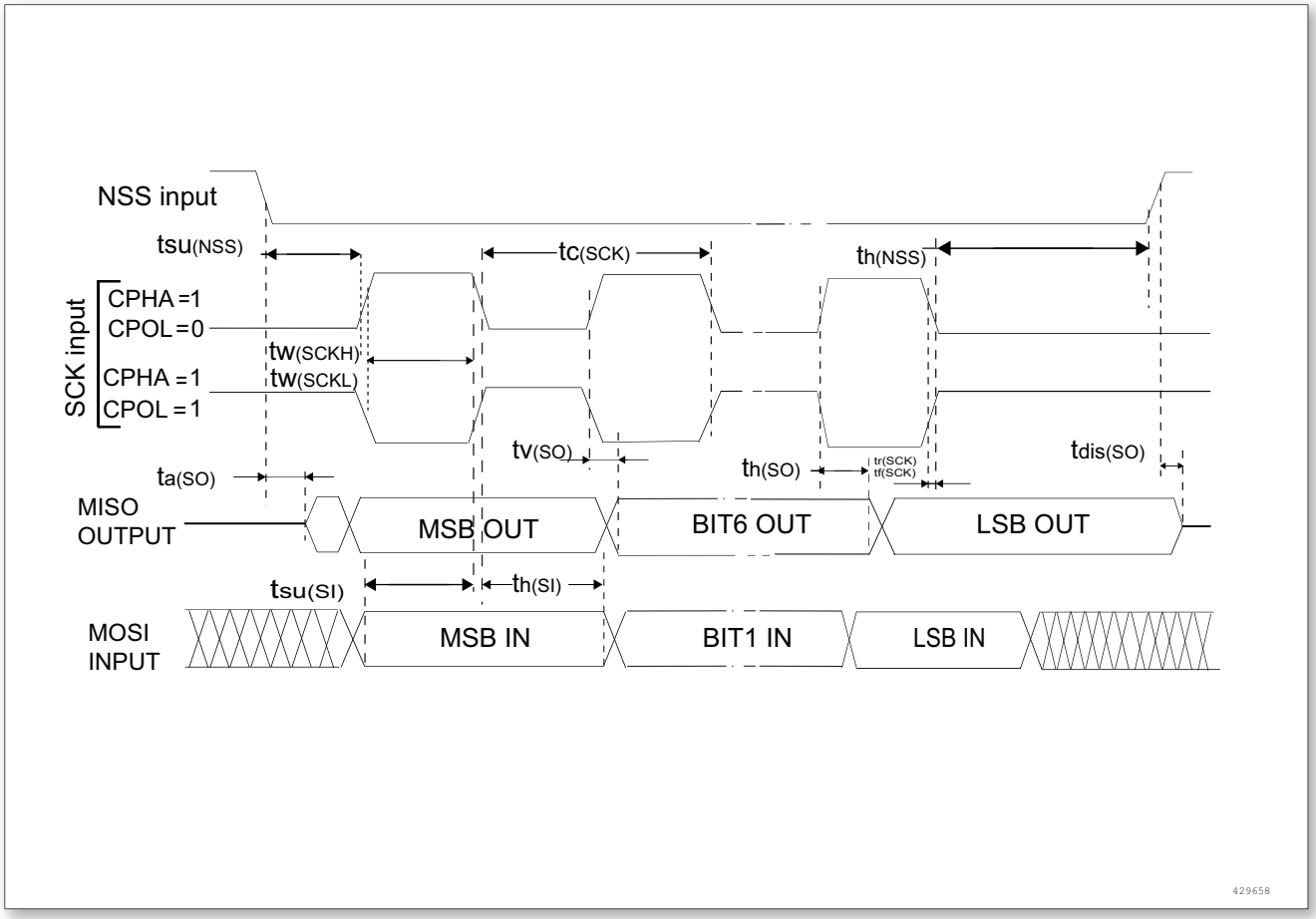

Figure 19. SPI timing diagram-slave mode and CPHA = 1[(1)], SPI_CCTL.CPHASEL=1 waveform diagram

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

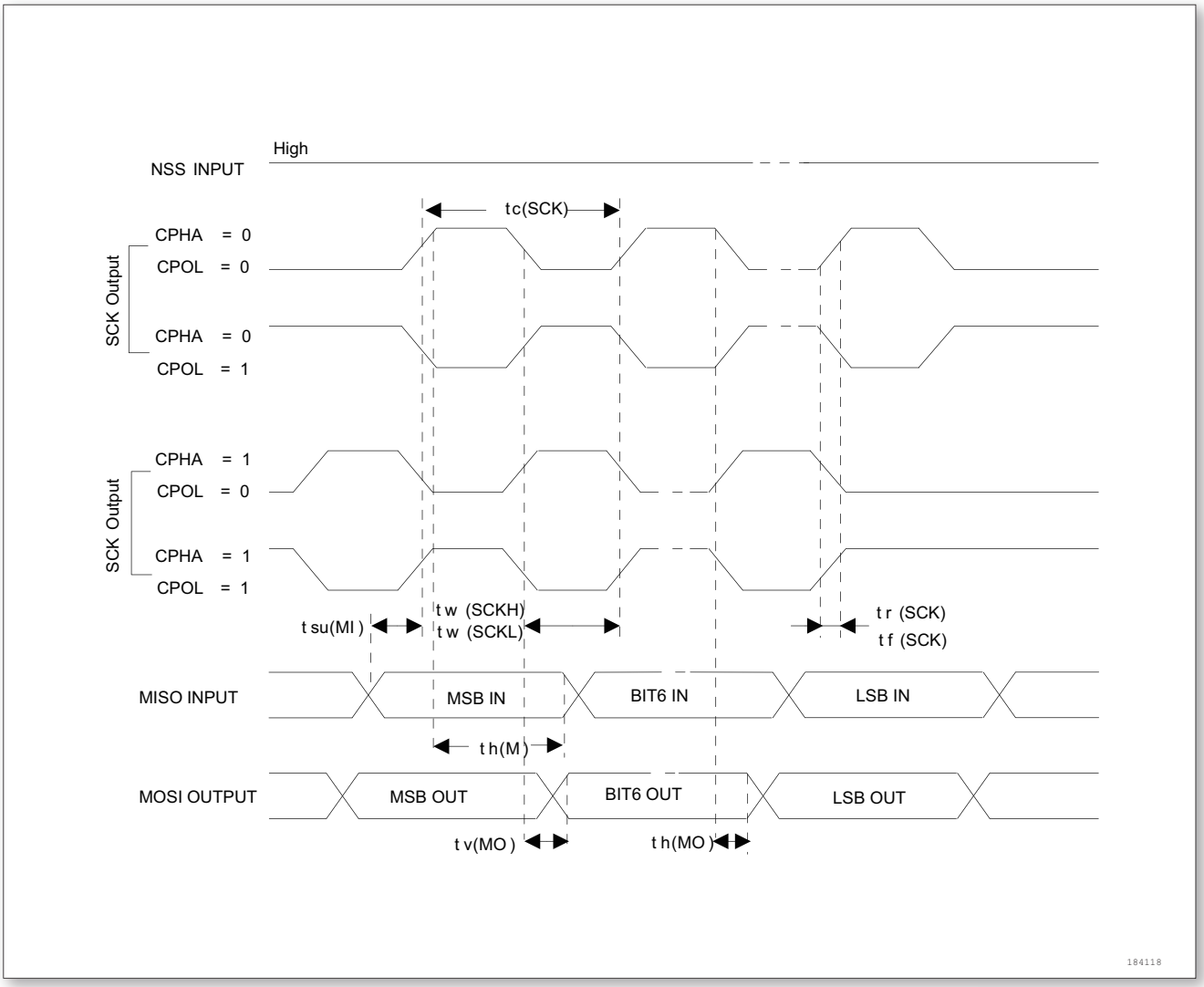

Figure 20. SPI timing diagram-master mode(1), CPHASEL=1

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

Table 32. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP, USBDM)	0.2		
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	V
V_{SE}(4)	Single ended receiver threshold		1.3	2	

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Output levels					
V_{OL}	Static output level low	R_L of 1.5kΩ to 3.6V(5)		0.3	V
V_{OH}	Static output level high	R_L of 15kΩ to V_{SS} (5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, USBDP (D +) pin has a built-in 1.5kΩ resistor connected to the V_{DD}, no more external connections.
3. The USB functionality is ensured down to 2.7V but not the full USB electrical characteristics which are degraded in the 2.7V ~ 3.0V voltage range.
4. Guaranteed by comprehensive evaluation, not tested in production.
5. R_L is the load connected on the USB drivers

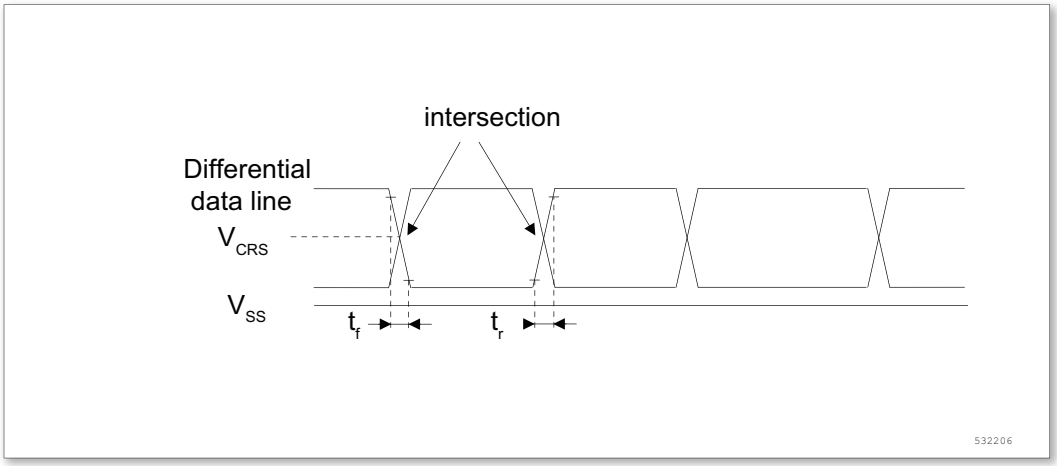

Figure 21. USB timing: definition of data signal rise and fall time

5.3.14 CAN (controller area network) interface

Refer to subsubsec 5.3.10 for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.15 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 9.

Note: It is recommended to perform a calibration after each power-up

Table 33. ADC characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2.5	3	5.5	V
V_{REF+}	Positive reference voltage		2.5		V_{DDA}	V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
f_{ADC}	ADC clock frequency				15(1)	MHz
f_S(2)	Sampling rate				1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 15MHz			833	KHz
					1/17	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} connected to ground)		V_{DDA}	V
R_{AIN}(2)	External sample and hold capactor		See Formulas 1 and Table 34			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor			10		pF
t_S(2)	Sampling time	f_{ADC} = 15MHz	0.1		16	μs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Stabilization time			1		μs
t_{conv}(2)	Total conversion time (including Sampling time)	f_{ADC} = 15MHz	1		16.99	μs
			15 ~ 253 (sampling t_{S+}) stepwise approximation 13.5			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. In this series of products, V_{REF+} is internally connected to $_{DDA}$，V_{REF-} is internally connected to $_{SSA}$.
3. f_{ADC} supports up to 15MHz，f_S supports up to 1MHz (f_{PCLK2} = 60MHz，ADC Prescaler = 4，f_{ADC} = 15MHz, TS = 1.5)

Formula 1: Maximum R_{AIN} Formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times (N+3) \times ln(2)} - R_{ADC}$$

The above formula (Equation 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N = 12 (representing 12-bit resolution) . In(2) = 0.69314718.

Table 34. Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.1	1.2
7.5	0.5	30
13.5	0.9	57
28.5	1.9	123
41.5	2.76	180

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
55.5	3.7	240
71.5	4.77	312
239.5	16.0	1050

1. Guaranteed by design. Not tested in production.

Table 35. ADC Accuracy - Limit Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit
ET	Comprehensive error	f_{PCLK2} = 60MHz, f_{ADC} = 15MHz, R_{AIN} < 10KΩ, V_{DDA} = 3.3V, T_A = 25°C	±10	±14	LSB
EO	Offset error		±4	±10	
EG	Gain error		±6	±8	
ED	Differential linearity error		±2	±4	
EL	Integral linearity error		±4	±6	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in sub-subsec 5.3.11 does not affect the ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

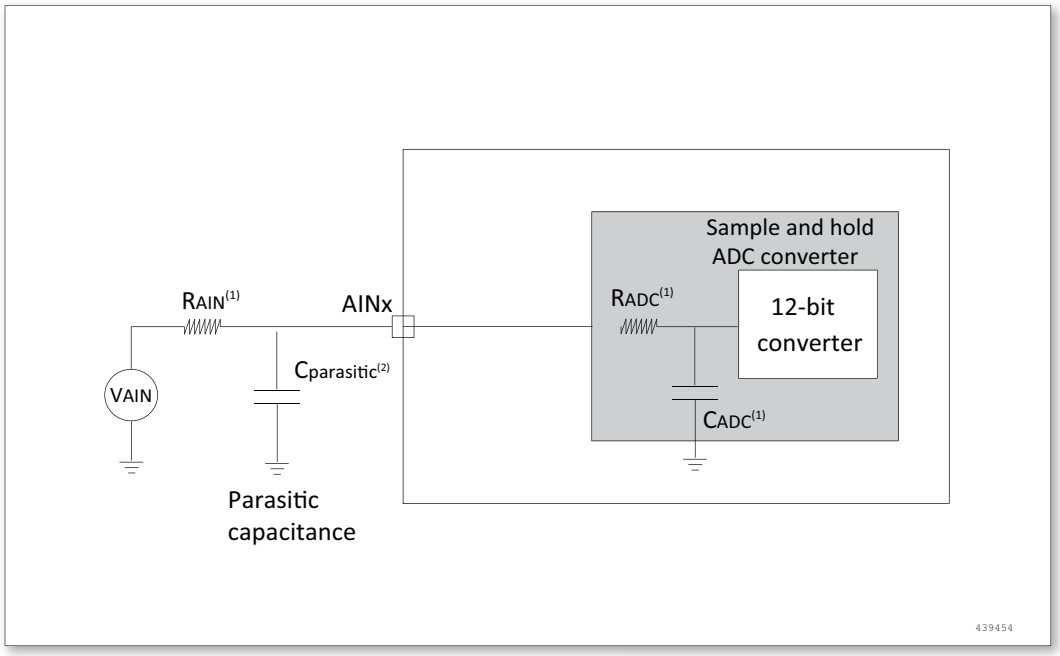

Figure 22. Typical connection diagram using the ADC

1. See Table 35 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly $7pF$) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The $10nF$capacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

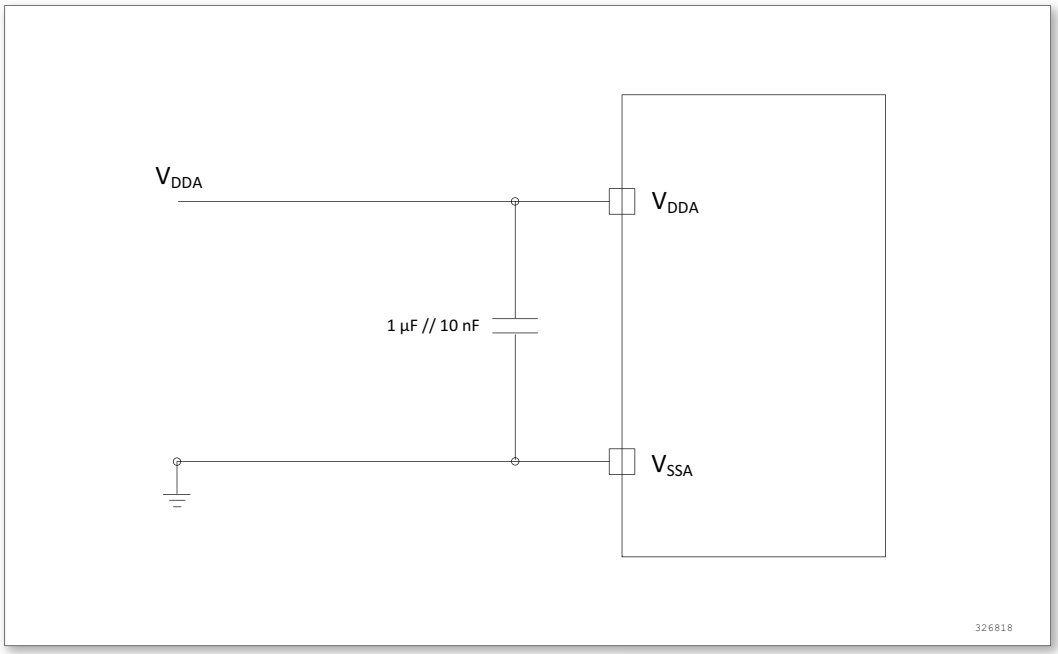

Figure 23. Power supply and reference power supply decoupling circuit

5.3.16 Temperature sensor characteristics

Table 36. Temperature sensor characteristics(3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25} (1)	Voltage at 25°C	1.433	1.451	1.467	V
t_{start} (2)	Setup time			10	µs
T_{S_temp} (2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

5.3.17 DAC characteristics

Table 37. DAC characteristics

Symbol	Parameter	Comment	Min	Type	Max	Unit
V_{DDA}	Analog supply voltage		2	5	5.5	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		V_{DDA}		V
V_{SSA}	Ground			0		V

Symbol	Parameter	Comment	Min	Type	Max	Unit
R_{LOAD}(1)	V_{SSA} Aresistive load with buffer ON					kΩ
	V_{DDA} Aresistive load with buffer ON					kΩ
R_O	Impedance output with buffer OFF	When the Buffer is OFF, the Minimum impedance between DAC_OUT and V_{DD} is 1.5 MΩ			20	kΩ
C_{LOAD}(1)	Capacitive load	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).			50	pF
DAC_OUTmin(1)	Lower DAC_OUT voltage with buffer ON	Giving the DAC a maximum output offset, which is equivalent to giving a 12-bit input between 0x0E0 and 0xF1C at V_{REF+} = 2.4V or a 12-bit input between 0x155 and 0xEAB at V_{REF+} = 2.4V			0.2	V
DAC_OUTmax(1)	Higher DAC_OUT voltage with buffer ON				V_{DDA}-0.2	V
DAC_OUTmin(1)	Lower DAC_OUT voltage with buffer ON	It gives the maximum output excursion of the DAC.			0.5	mV
DAC_OUTmax(1)	Higher DAC_OUT voltage with buffer ON				V_{DDA}-0.01	V
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	No load, V_{REF+} = 3.6V, Enter the DC loss for worst case value 0x0E4		50		μA
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	No load, enter the median value of 0x800		630		μA
		No load, V_{REF+} = 3.6V, Enter the DC loss at worst-case value 0xF1C		703		μA
DNL(2)	Differential linearity, the difference between two consecutive values (LSBs)	Given for the DAC in 12-bit configuration			±3	LSB
INL(2)	Integral nonlinearity	Given for the DAC in 12-bit configuration			±4	LSB
offset(2)	Offset error (difference between measured value at Code(0x800) and the ideal value = VREF+/2)	Given for the DAC in 12-bit configuration			±10	
		Given for the DAC in 12-bit configuration，V_{REF+} = 5.5V			±12	

Symbol	Parameter	Comment	Min	Type	Max	Unit
Gain error(2)	Gain error	Given for the DAC in 12-bit configuration			±0.5	%
$t_{SETTLING}$(2)	Settling time	$C_{LOAD} \leqslant 50pF.R_{LOAD} \geqslant 5k\Omega$			4	μs
Updata rate(2)	Max frequency for acorrect DAC_OUT change when small variation in the input code(from code i to i+1LSB)	$C_{LOAD} \leqslant 50pF.R_{LOAD} \geqslant 5k\Omega$			1	MS/s
t_{WAKEUP}(2)	Wake-up Time in Shutdown (ENx is Configured in DAC Control Register)	$C_{LOAD} \leqslant 50pF.R_{LOAD} \geqslant 5k\Omega$			10	μs
PSRR+(1)	Power Supply Rejection Ratio V_{DDA} (Static DC Measurement)	No R_{LOAD}, C_{LOAD} = 50pF			-40	dB

1. Guaranteed by design, not tested in production.
2. Preliminary data.

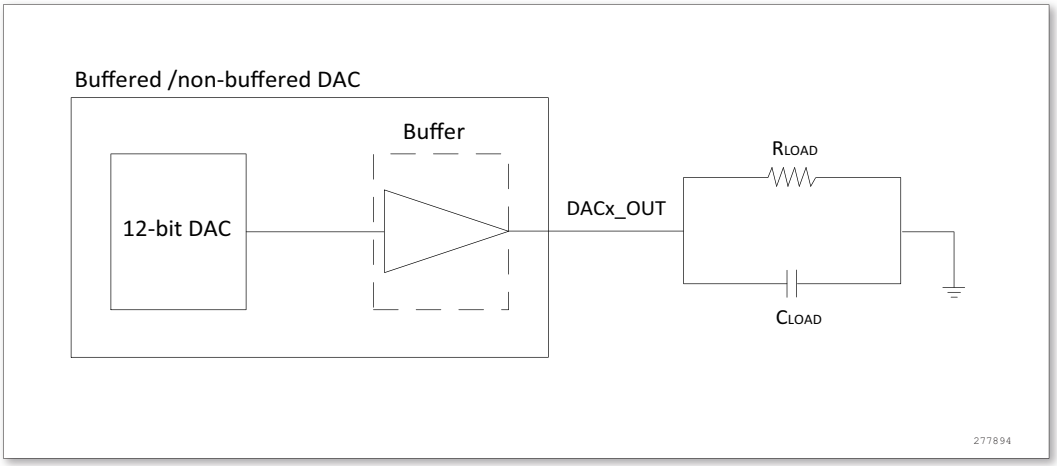

Figure 24. 12Bit buffered /non-buffered DAC

6 Package information

Package information

6.1 Package LQFP64

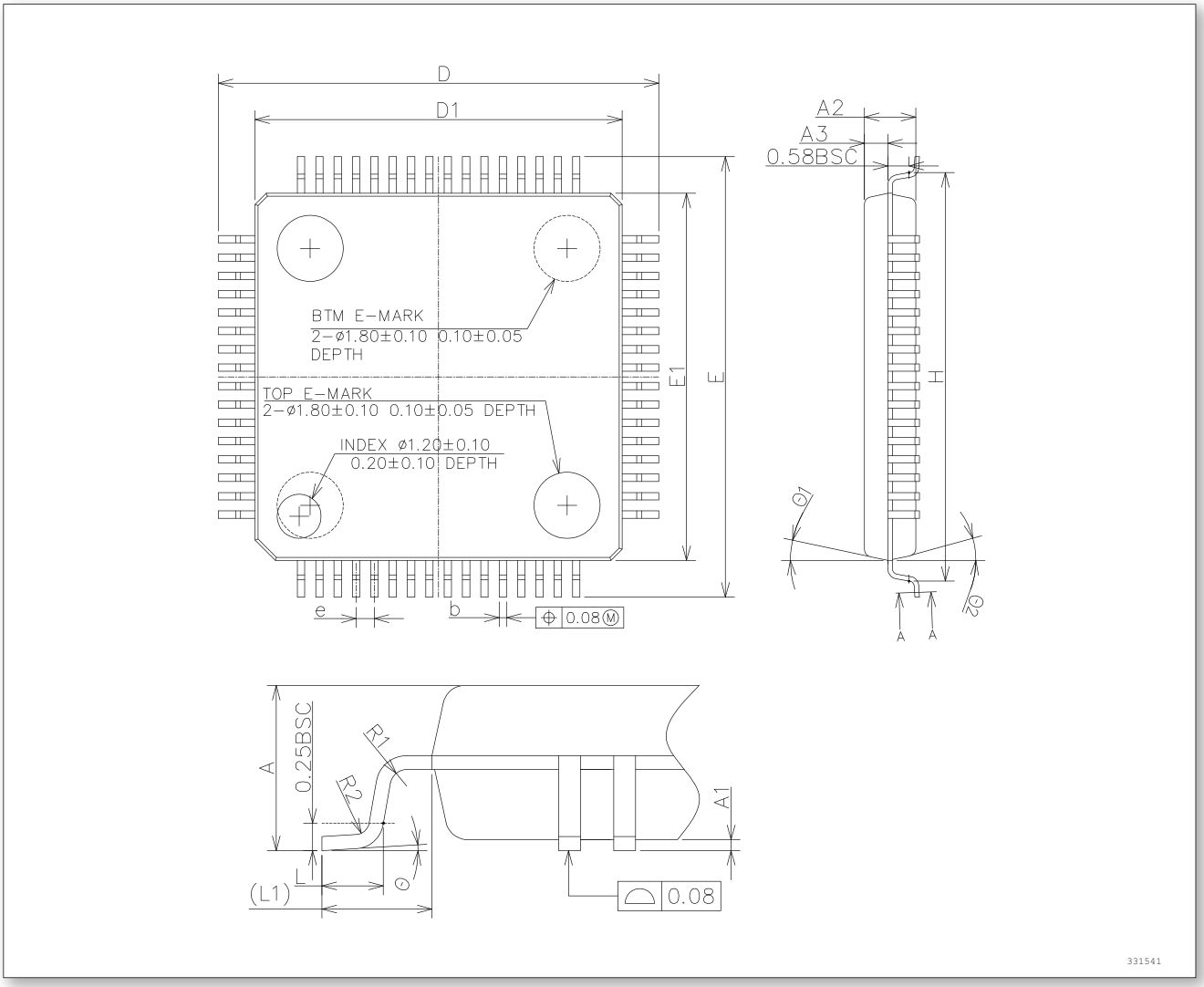

Figure 25. LQFP64, 64-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 38. LQFP64 dimensions

Label	Milimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.2 Package LQFP48

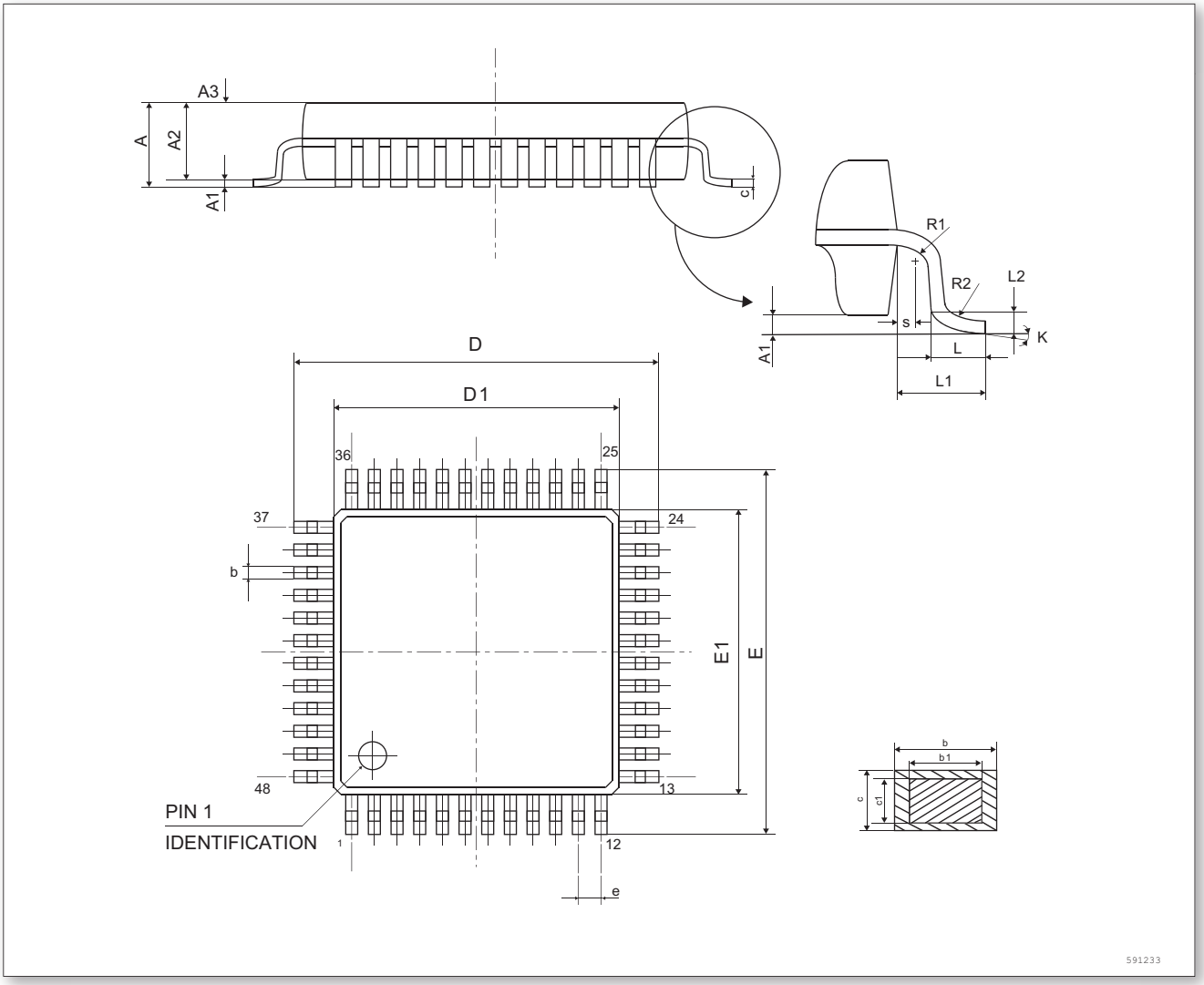

Figure 26. LQFP48, 48-pin low-profile quad square flat package outline

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 39. LQFP48 dimensions

Label	Milimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20

Label	Milimeter		
	Minimum	Typical	Maximum
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0 °	3.5 °	7 °
θ 1	11 °	12 °	13 °
θ 2	11 °	12 °	13 °

6.3 Package LQFP32

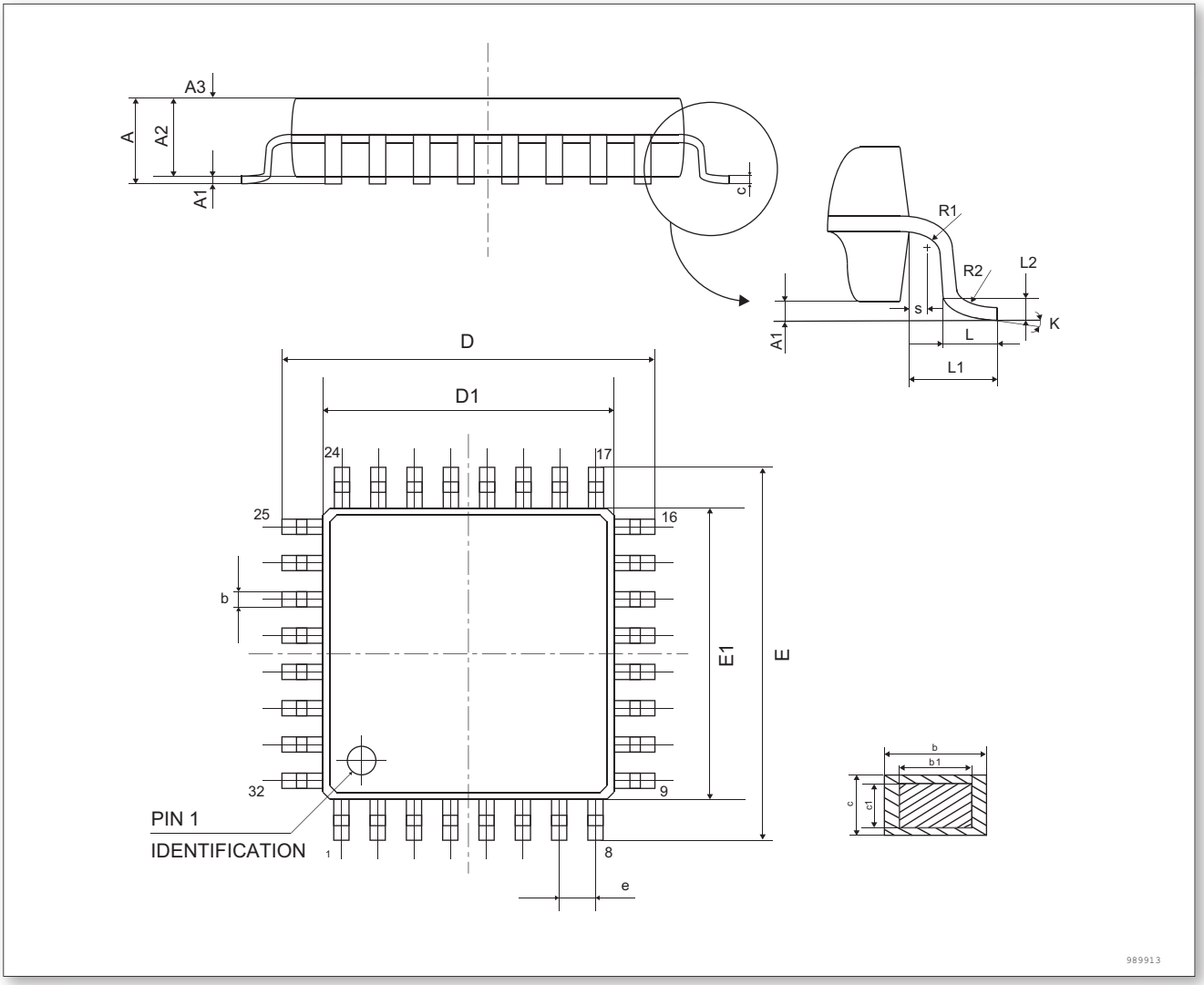

Figure 27. LQFP32, 32-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 40. LQFP32 dimensions

Label	Milimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20

Label	Milimeter		
	Minimum	Typical	Maximum
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08		
R2	0.08		0.20
S	0.20		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.4 Package QFN32

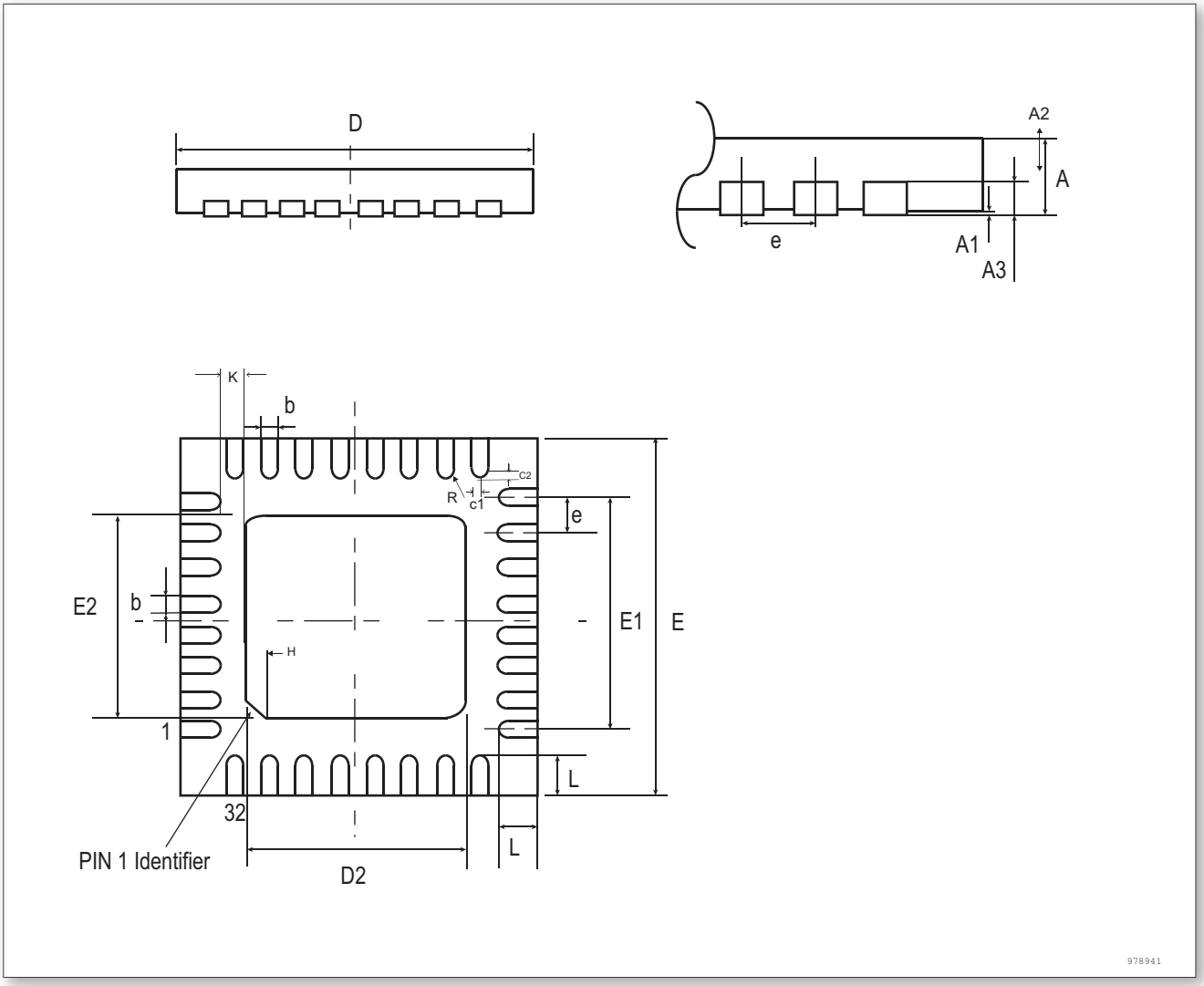

Figure 28. QFN32, 32-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 41. QFN32 dimensions

Label	Milimeter		
	Minimum	Typical	Maximum
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60

Label	Milimeter		
	Minimum	Typical	Maximum
e		0.5	
H		0.30REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.09		
c1		0.08	
c2		0.08	
N		Number of pins = 32	

7 Ordering information

Ordering information

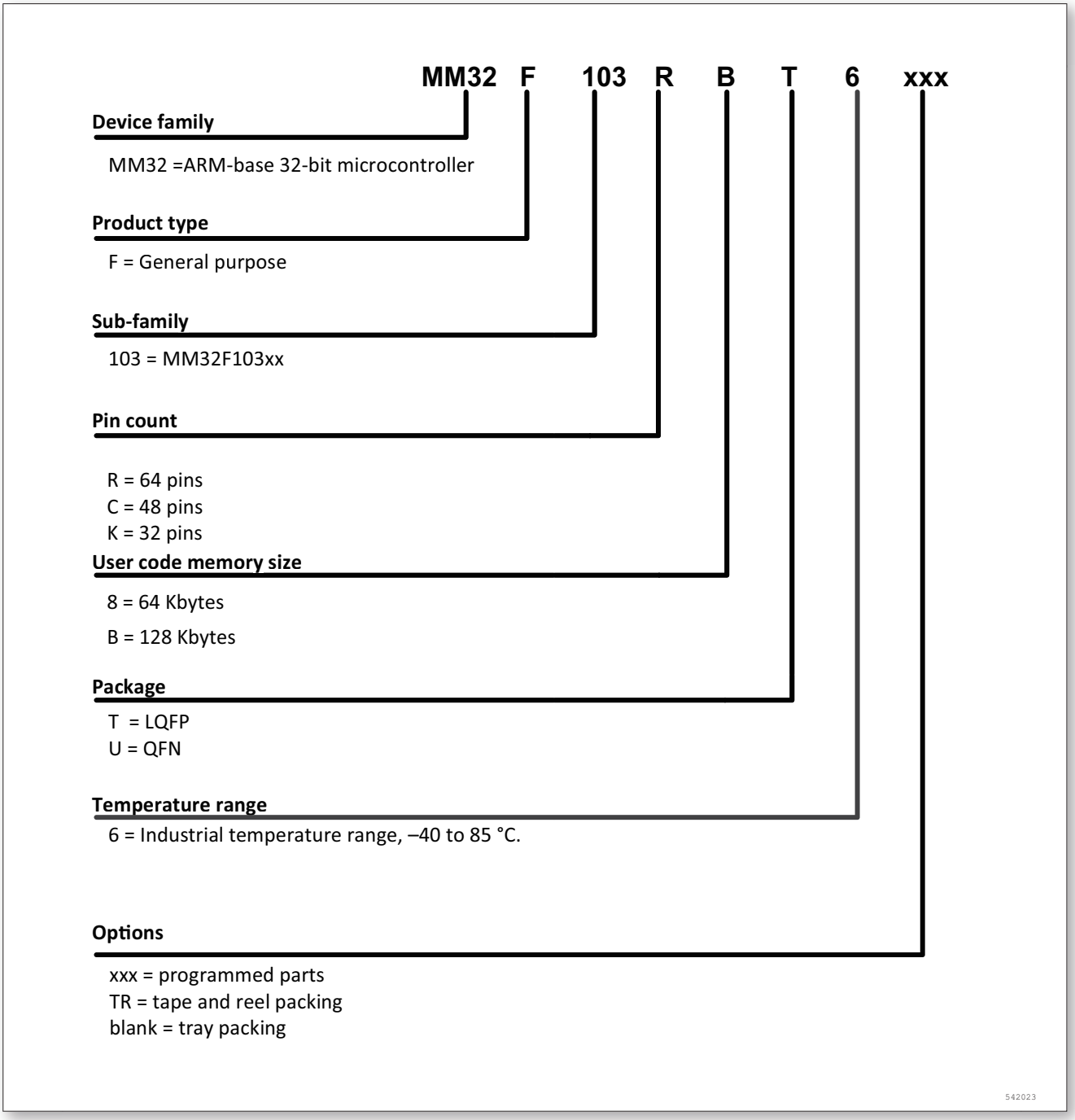

Figure 29. Ordering information scheme

8 Revision history

Revision history

Table 42. Revision history

Date	Version	Content
2022/07/27	Rev1.11	1.Add annotation in table 10 and 0.1uF capacitance in NRST figure is changed into 1uF; 2.Update IO parameters.
2021/11/18	Rev1.10	Add DAC characteristics, etc.
2020/04/07	Rev1.09	Modify the high-speed internal oscillator characteristic parameters.
2020/02/13	Rev1.08	Modify the MCO clock source of the clock tree .
2019/09/24	Rev1.07	Modify model naming data.
2019/06/11	Rev1.06	Modify memory charcateristic parameters.
2019/03/11	Rev1.05	Modify package parameters.
2019/01/07	Rev1.04	Modify ADC voltage parameter characteristics.。
2018/11/21	Rev1.03	Modify parameters.
2018/10/11	Rev1.02	Modify electrical characteristics.
2018/09/14	Rev1.01	Modify electrical characteristics/product parameters.
2018/04/12	Rev1.00	Initial release.