Data Sheet

MM32F3270

Arm® Cortex®-M3 based 32-bit Microcontrollers

Revision：1.45

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1 Introduction

1.1 Overview

The MM32F3270 microcontrollers are based on Arm® Cortex®-M3 core. These devices have a maximum clocked frequency of 120MHz, built-in 512KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain three 12-bit ADC, two analog comparators, two 16-bit advanced timer, two 16-bit and two 32-bit general purpose timers and two 16-bit basic timers, as well as communication interfaces including two I2C, three I2S, three SPI, one USB OTG full-speed interface, one CAN interface, one SDIO interface and eight UART.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) includes the industrial tier -40°C to 85°C and the extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Industrial IoT devices
- Alarm systems, video intercom systems, heating, ventilation, and air conditioning systems
- Medical and handheld devices
- Motor drive and application control
- PC game peripherals and GPS platforms
- Programmable logic controllers (PLC), frequency converters, printers, and scanners, etc.

This product series is available in LQFP144, LQFP100, LQFP64, LQFP48 and QFN40 packages.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M3.
  - Standard operating frequency up to 96MHz
  - Maximum operating frequency up to 120MHz
- Memory
  - Up to 512KB embedded Flash storage.
  - Up to 128KB SRAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
  - FSMC interface, supporting external SRAM/PSRAM/NOR Flash, compatible with the 8080/6800 communication bus mode

- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.
  - Support multiple PLL and frequency division mode, for USB clock source
  - PLL supports CPU operating at a frequency of up to 120MHz
  - Internal 40KHz low speed oscillator
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
- Low power
  - Several low-power modes, including Lower Power Run, Sleep, Low Power Sleep, Stop, Deep Stop, and Standby modes
  - V_{BAT} supplies power to the RTC and backup registers
- Three 12-bit analog-to-digital converters, 1μS of conversion time (up to 21 input channels and 3 internal input channels)
  - Conversion range: 0 ~ V_{DDA}
  - Support the configuration of sampling time and resolution
  - On-chip temperature sensor
  - On-chip voltage sensor
  - V_{BAT} voltage sensor
- Two DACs
- Two analog comparators
- Two DMA controllers, with 12 channels in total
  - Supported peripherals include Timer, ADC, DAC, UART, I2C, SPI, USB OTG
- Up to 116 fast I/O ports:
  - Group A~G I/O ports can be connected to 16 external interrupt lines (Group H I/O ports don't support external interrupt).
  - All ports are capable of inputting and outputting signals lower than V_{DD}.
- 11 timers
  - Two 16-bit 4-channel advanced control timers providing 4-channel PWM output, with dead zone generation and emergency stop functions
  - Two 16-bit general-purpose timers and two 32-bit general-purpose timers providing up to 4 input captures/output comparisons, usable for IR control decoding
  - Two 16-bit general-purpose timers providing one input capture/output comparison and one set of complementary outputs, with functions of dead zone generation, emergency stop and modulator gate circuit for IR control

  - Two watchdog timers (independent type and window type)
  - One SysTick timer: 24-bit down counter
- Debug mode
  - Serial wire debug (SWD) port and JTAG interface
- Up to 16 digital peripheral interfaces
  - Eight UART interfaces
  - Two I2C interfaces
  - Three SPI interfaces (three I2S interfaces)
  - One CAN interface
  - One USB OTG interface
  - One SDIO interface
- CRC calculation unit
- 96-bit unique ID (UID) of the chip
- Adopts LQFP144, LQFP100, LQFP64, LQFP48 and QFN40 packages.

2 Specification

2.1 Model list

2.1.1 Ordering information

Table 2-1 Ordering information

Part numbers		MM32 F3273 GAQ	MM32 F3273 E6P	MM32 F3273 G6P	MM32 F3273 E7P	MM32 F3273 G7P	MM32 F3273 E8P	MM32 F3273 G8P	MM32 F3273 E9P	MM32 F3273 G9P(V)
CPU frequency		120 MHz								
Flash - KB		512	256	512	256	512	256	512	256	512
SRAM - KB		128	128	128	128	128	128	128	128	128
Timers	16-bit GP	2	2	2	2	2	2	2	2	2
	32-bit GP	2	2	2	2	2	2	2	2	2
	Basic	2	2	2	2	2	2	2	2	2
	Advanced	2	2	2	2	2	2	2	2	2
Interfaces	UART	4	7	7	7	7	8	8	8	8
	I2C	2	2	2	2	2	2	2	2	2
	SPI	2	2	2	2	2	2	2	3	3
	I2S	2	2	2	2	2	2	2	3	3
	CAN	1	1	1	1	1	1	1	1	1
	SDIO	-	-	-	1	1	1	1	1	1
	USB-OTG FS	1	1	1	1	1	1	1	1	1
GPIO		27	38	38	52	52	84	84	116	116
12-bit ADC	Modules	3	3	3	3	3	3	3	3	3
	Channels	10	10	10	16	16	16	16	21	21
FSMC		-	-	-	-	-	√	√	√	√
Comparators		2	2	2	2	2	2	2	2	2
DAC		2	2	2	2	2	2	2	2	2
RTC		√	√	√	√	√	√	√	√	√
Supply voltage		2.0V ~ 5.5V								
Temperature range		-40°C to +85°C / -40°C to +105°C (Suffix V)								
Package		QFN40	LQFP48		LQFP64		LQFP100		LQFP144	

2.1.2 Marking information

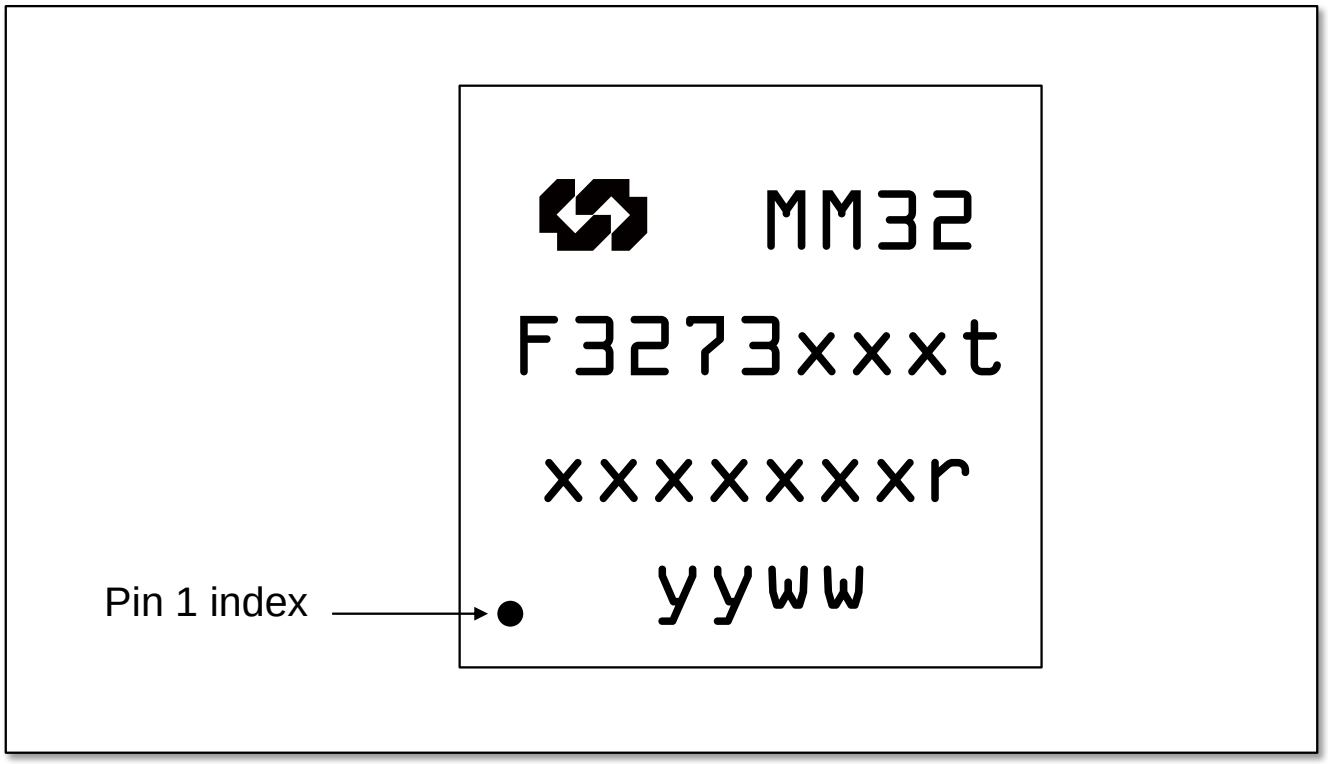

Figure 2-1 LQFP and QFN package marketing

LQFP and QFN package have the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: F3273xxxt
  - Second part of product name, “t” means temperature range, “t” = (blank) means temperature range is -40°C to 85°C, “t” = “V” means temperature range is -40°C to 105°C.
- 3rd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

2.1.3 Block diagram

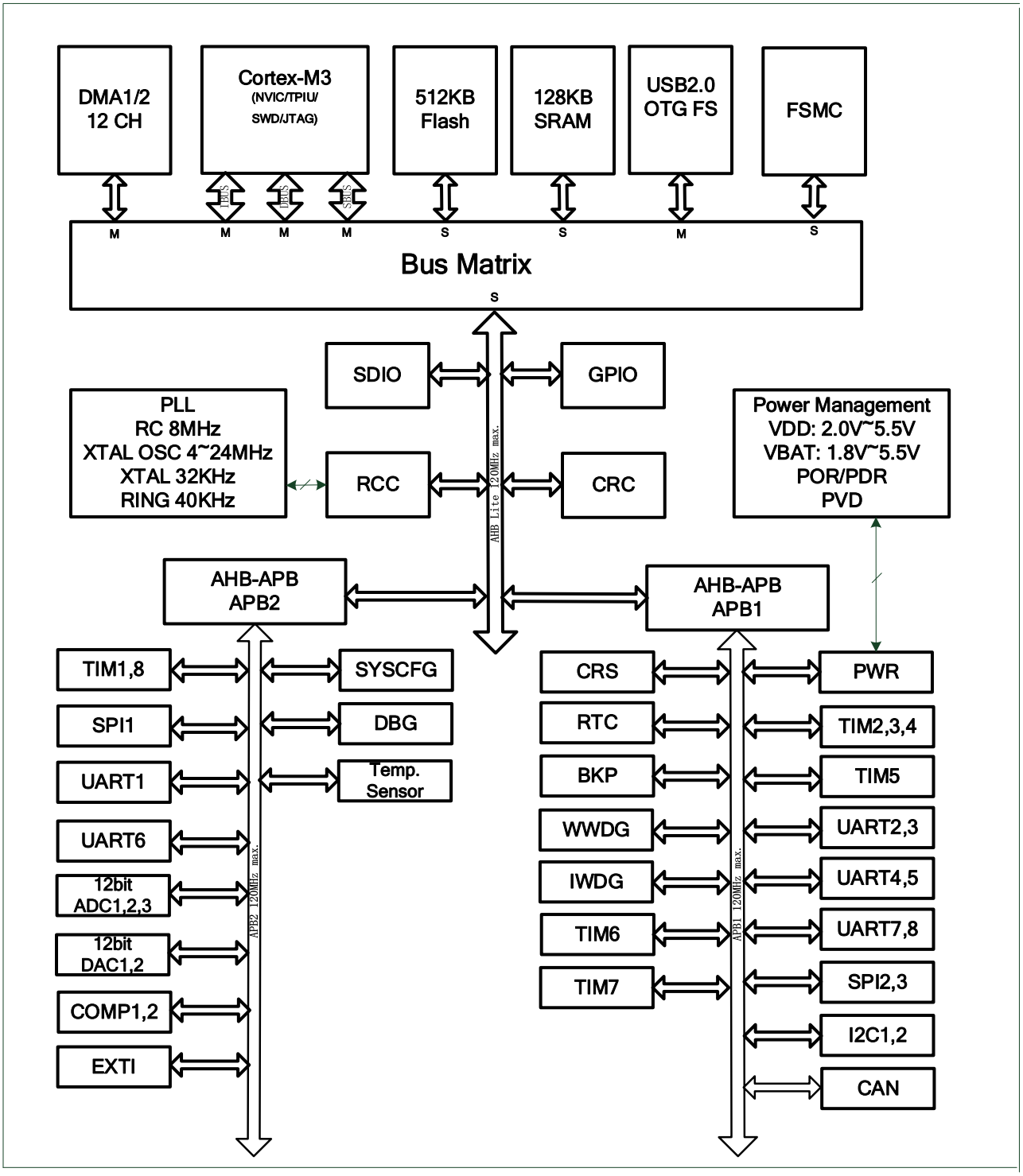

Figure 2-2 System block diagram

2.2 Functional description

2.2.1 Core introduction

The Arm® Cortex®-M3 microcontroller is a configurable 32-bit RISC (Reduced Instruction Set Computing) processor featuring a multistage pipelined architecture, thus having high performance and low power consumption.

2.2.2 Bus introduction

The bus matrix connects the processor and debug ports to the external bus matrix which includes:

- Instruction bus, a 32-bit AHB-Lite bus, usable for fetching instructions and vectors from the code space.
- Data bus, a 32-bit AHB-Lite bus, usable for data loading/storing as well as debugging/accessing in the code space.
- System bus, a 32-bit AHB-Lite bus, usable for instructions and vector fetches, data loading/storing, and debugging/accessing in the system space.

2.2.3 Memory map

Table 2-2 Memory map

Bus	Address	Size	Peripherals
Flash	0x0000 0000 - 0x0007 FFFF	512 KB	Mapped to one of the embedded Flash memory, SRAM, and system memory, depending on the level of the BOOT0/1 pin
	0x0008 0000 - 0x07FF FFFF	~127 MB	Reserved
	0x0800 0000 - 0x0807 FFFF	512 KB	Embedded Flash memory
	0x0808 0000 - 0x080F FFFF	512 KB	Reserved
	0x0810 0000 - 0x0810 0FFF	4 KB	Reserved
	0x0810 1000 - 0x0FFF FFFF	~127 MB	Reserved
	0x1000 0000 - 0x1FFD FFFF	~255 MB	Reserved
	0x1FFE 0000 - 0x1FFE 0FFF	4 KB	Reserved
	0x1FFE 1000 - 0x1FFE 1FFF	4 KB	Security memory
	0x1FFE 2000 - 0x1FFF E7FF	114 KB	Reserved
	0x1FFF E800 - 0x1FFF F7FF	4 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5 KB	Option bytes
	0x1FFF FA00 - 0x1FFF FFFF	1.5 KB	Reserved
SRAM	0x2000 0000 - 0x2000 3FFF	16 KB	SRAM-2
	0x2000 4000 - 0x2001 FFFF	112 KB	SRAM-1
	0x2002 0000 - 0x3FFF FFFF	~511 MB	Reserved

Bus	Address	Size	Peripherals
AHB3	0x6000 0000 - 0x63FF FFFF	64 MB	FSMC Bank
	0x6400 0000 - 0x67FF FFFF	64 MB	FSMC Bank
	0x6800 0000 - 0x6BFF FFFF	64 MB	FSMC Bank
	0x6C00 0000 - 0x6FFF FFFF	64 MB	FSMC Bank
	0x7000 0000 - 0x9FFF FFFF	768 MB	Reserved
	0xA000 0000 - 0xA000 0FFF	4 KB	FSMC Register
	0xA000 1000 - 0xA000 13FF	1 KB	Reserved
AHB2	0x5000 0000 - 0x5003 FFFF	256 KB	USB OTG FS
	0x5006 0000 - 0x5006 03FF	1 KB	Reserved
	0x5006 0800 - 0x5006 0BFF	1 KB	Reserved
AHB1	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 3400 - 0x4002 7FFF	19 KB	Reserved
	0x4002 8000 - 0x4002 9FFF	8 KB	Reserved
	0x4002 A000 - 0x4003 FFFF	88 KB	Reserved
	0x4004 0000 - 0x4004 03FF	1 KB	Port A
	0x4004 0400 - 0x4004 07FF	1 KB	Port B
	0x4004 0800 - 0x4004 0BFF	1 KB	Port C
	0x4004 0C00 - 0x4004 0FFF	1 KB	Port D
	0x4004 1000 - 0x4004 13FF	1 KB	Port E
	0x4004 1400 - 0x4004 17FF	1 KB	Port F
	0x4004 1800 - 0x4004 1BFF	1 KB	Port G
	0x4004 1C00 - 0x4004 1FFF	1 KB	Port H
	0x4004 1C00 - 0x47FF FFFF	~127 MB	Reserved
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC1
	0x4001 2800 - 0x4001 2BFF	1 KB	ADC2
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8

Bus	Address	Size	Peripherals
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	UART6
	0x4001 4000 - 0x4001 43FF	1 KB	COMP
	0x4001 4400 - 0x4001 4BFF	2 KB	Reserved
	0x4001 4C00 - 0x4001 4FFF	1 KB	ADC3
	0x4001 5000 - 0x4001 5FFF	4 KB	Reserved
	0x4001 6000 - 0x4001 63FF	1 KB	Reserved
	0x4001 6400 - 0x4001 7FFF	7 KB	Reserved
	0x4001 8000 - 0x4001 83FF	1 KB	SDIO
	0x4001 8400 - 0x4001 FFFF	31 KB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1800- 0x4000 27FF	4 KB	Reserved
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC_BKP
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 4800 - 0x4000 4BFF	1 KB	UART3
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5C00 - 0x4000 63FF	2 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7800 - 0x4000 7BFF	1 KB	UART7
	0x4000 7C00 - 0x4000 7FFF	1 KB	UART8

2.2.4 Embedded Flash

Up to 512K bytes of embedded Flash memory available for storing programs and data.

2.2.5 Embedded SRAM

The embedded SRAM is up to 128KB.

2.2.6 Nested vectored interrupt controller (NVIC)

This product embeds a nested vectored interrupt controller, which can handle multiple maskable interrupting channels (excluding 16 Cortex®-M3 interrupt lines) with 8 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the kernel
- Tightly coupled NVIC interfaces
- Allows early processing of interrupts
- Handles higher-priority interrupts that arrive late
- Supports tail-chaining of interrupts
- Automatically saves the processor state
- Offers automatic recovery when an interrupt returns without extra instruction overhead
  This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of multiple edge detectors, used to generate interrupt/event requests by capturing the level variation of IO ports. Group A~G I/O ports can be connected to 16 external interrupt lines (Group H I/O ports don't support external interrupt). Each interrupt line can be independently turned on/off or enable its own trigger mode (rising edge, falling edge or both). A pending register maintains the status of all interrupt requests.

The EXTI can detect the level variation with a pulse width shorter than the internal AHB clock period.

2.2.8 Clock and startup

The system clock is selected after startup. The internal 8MHz oscillator is selected as the default system clock after reset, and then the external 8 ~ 24MHz clock source can be selected. If an external clock failure is detected, the system will mask the external clock source automatically, turn off PLL, and switch back to the internal oscillator. At that point, if a relevant interrupt monitoring switch is enabled, the software can receive the corresponding interrupt request.

Several prescalers are used to generate clocks for AHB bus and high-speed APB (APB1 and APB2) bus in the clock system. The maximum clock frequency of AHB and high-speed APB is 120MHz. The clock tree of the clock system is shown in the Figure 2-3.

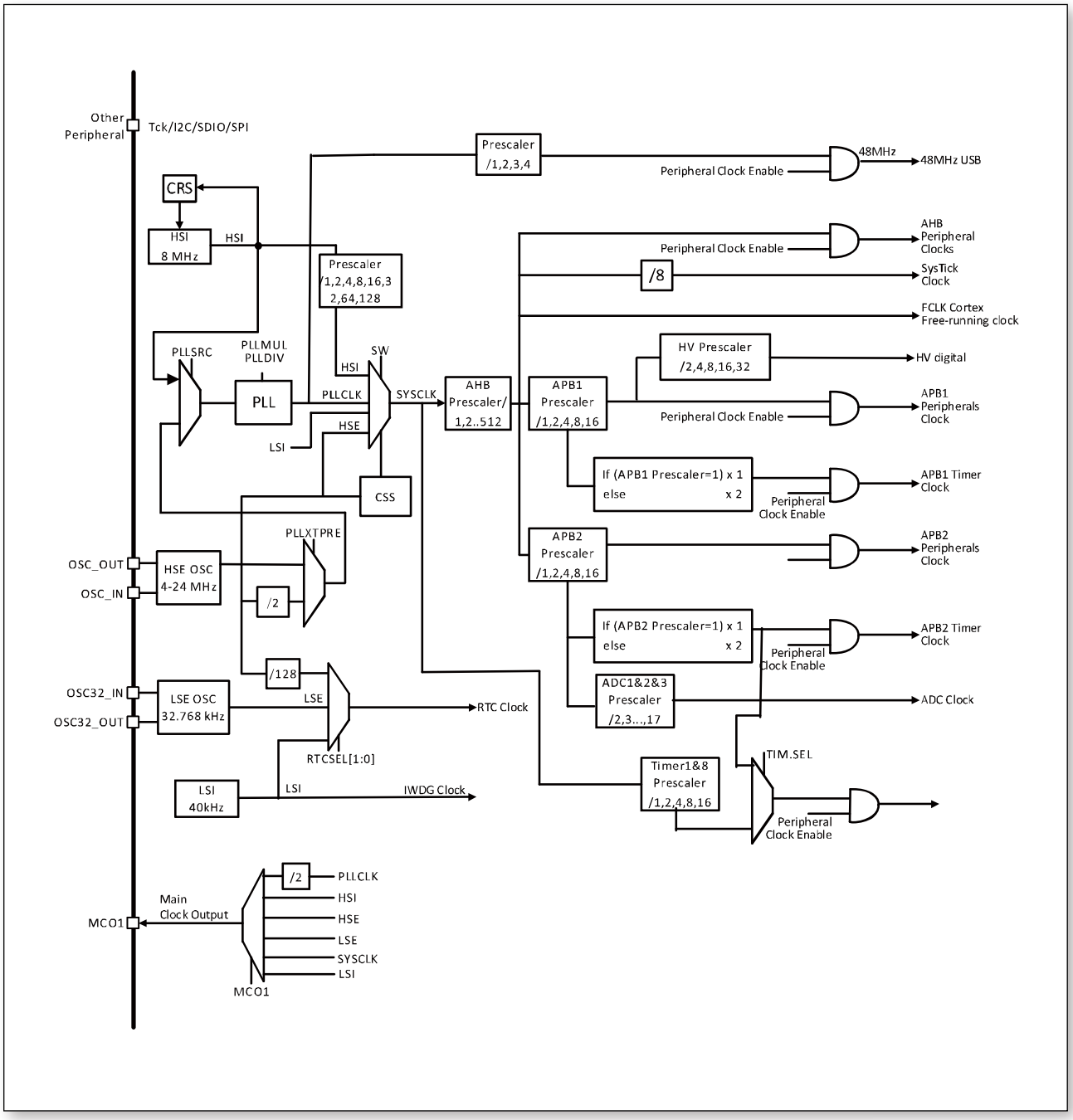

Figure 2-3 Clock tree

2.2.9 Boot modes

At startup, BOOT0/1 pins are used to select one of three boot options:

- Boot from the embedded Flash
- Boot from the system memory
- Boot from the embedded SRAM

The Bootloader program resides in the system memory. After the Bootloader is launched from the system memory, it is used to reprogram the embedded Flash memory through UART1.

Note: Products with QFN40 package do not have BOOT1 pin and only support booting from on-chip Flash.

2.2.10 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator through V_{DD} pins.
- V_{DDA} = 2.0V ~ 5.5V: It supplies power to the ADC, the reset module, the oscillator, and the analog part of PLL. V_{DDA} and V_{SSA} can be connected to V_{DD} and V_{SS} respectively or be supplied independently (the voltage should be consistent with V_{DD} and V_{SS}).
- V_{BAT} = 1.8V ~ 5.5V: When V_{DD} is turned off, it supplies power to the RTC, the external 32KHz oscillator and the backup register (through the internal power switcher). When there's no backup battery in the application system, the V_{BAT} pin can be either connected to V_{DD} or floating.

2.2.11 Power supply supervisors

This product has integrated power-on reset (POR)/power-down reset (PDR) circuit. The circuit remains in the working state and ensures proper operation above a threshold of 2.0V. When VDD is below a specified threshold ($V_{POR/PDR}$), the device will be placed in the reset state, without the need for an external reset circuit.

Additionally, the device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} / V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, an interrupt can be generated. The interrupt handler will send a warning message or switch the microcontroller to the safe mode. The PVD function should be enabled by a program.

2.2.12 Voltage regulator

The embedded voltage regulator converts the external voltage into the internal logic circuit operating voltage. The voltage regulator remains in the working state after reset.

2.2.13 Low-power mode

The product support six low-power modes to achieve the best compromise between low power consumption, short startup time and multiple wake-up events.

Table 2-3 Overview of low-power modes

Mode	Entry	Wakeup	Effect on 1.5V domain clocks	Effect on V_{DD} domain clocks	Voltage regulator
Low Power Run	PWR_CR1.LPR=1	Clear PWR_CR1.LPR	PLL and HSE oscillator is powered off, HSI, LSI and LSE keep working. Chip frequency should not exceed 2MHz.	Low power mode	
SLEEP NOW or SLEEP ON EXIT	WFI (Wait for Interrupt)	Any interrupt	CPU clock is powered off, no influence on other clock and ADC clock	N/A	On
	WFE (Wait for Event)	Wake-up event			
Low Power Sleep	PWR_CR1.LPR=1 WFI or WFE	Any interrupt or external event	PLL and HSE oscillators OFF. HSI, LSI and LSE keep working. The operating clock frequency of the chip should not be higher than 2MHz.		Low-power mode
Stop	PWR_CR1.PDDS=0 PWR_CR1.LPDS=0 SLEEPDEEP bit WFI or WFE	Any interrupt or external event	All 1.5V domain clocks OFF		Low-power mode
Deep Stop	PWR_CR1.PDDS=0 PWR_CR1.LPDS=1 SLEEPDEEP bit WFI or WFE	Any interrupt or external event	All 1.5V domain clocks OFF		Deep low-power mode
Standby	PWR_CR1.PDDS=1 SLEEPDEEP bit WFI or WFE	WKUP pin rising edge, RTC alarm event, external reset in NRST pin, IWDG reset.	All 1.5V domain clocks OFF		OFF

Low Power Run mode

The Low Power Run mode is enabled through the VCORE provided by the low-power voltage regulator to minimize the operating current of the regulator. This code is executed from the SRAM or Flash and the CPU frequency is limited to 2MHz.

Sleep mode

In the Sleep mode, only the CPU stops working. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Low power sleep mode

The system enters the mode from the Low Power Run mode. Only the CPU stops working. The system returns to the Low Power Run mode when it is woken up by an event or an interrupt.

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers.

The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the signals configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Deep stop mode

This mode has the same status as the Stop mode, although less power is consumed.

Standby mode

The Standby mode allows to achieve the lowest power consumption. It is based on the CPU deep sleep mode, with the voltage regulator disabled. The entire 1.5V power supply domain is disconnected. PLL, HSI and HSE oscillators are also turned off. The device exits Standby mode when a rising edge on the WKUP pin, an external reset of NRST pin, or an IWDG reset occurs. The device also can be woken up and reset by the watchdog timer. After entering the Standby mode, the contents of SRAM and registers will be lost. Only backup registers and standby circuits remain powered.

2.2.14 DMA

The flexible 12-way universal DMA can manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The DMA controller supports the management of the ring buffer, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, with support for software trigger on each channel. The length, the source address and the destination address of the transfer can be set separately by the software.

The DMA can be used with major peripherals: UART, I2C, SPI, ADC, SDIO and general-purpose/basic/advanced control timer TIMx.

2.2.15 Timers and watchdog (TIM & WDG)

The product includes two advanced timer, four general-purpose timers, two basic timers, two watchdog timers and one SysTick timer. The following table compares the features of the advanced control timer, general-purpose timers and basic timers:

Table 2-4 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1 /TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2 /TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
	TIM3 /TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
Basic	TIM6 /TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

Advanced control timer (TIM1/TIM8)

The advanced control timer is composed of one 16-bit counter, four capture/comparison channels and a three-phase complementary PWM generator. It has complementary PWM outputs with dead zone insertion and can be used as a complete general-purpose timer. Four independent channels can be used for the followings:

- Input capture
- Output compare
- PWM generation (edge or center alignment mode)
- Single pulse output

If configured as a 16-bit general-purpose timer, it has the same features as a TIM2 timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In the debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of general-purpose TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

Four synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) are built into the product.

The general-purpose timer has one 16/32-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output comparison, PWM and single pulse mode output.

General-purpose timer_32-bit

The general-purpose timer has one 32-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output comparison, PWM and single pulse mode output.

General-purpose timer_16-bit

The general-purpose timer has one 16-bit auto-load up-down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output comparison, PWM and single pulse mode output.

The general-purpose timers can work together with the advanced control timer via the

Timer Link feature for synchronization or event chaining. Their counters can be frozen in the debug mode. Any of the general-purpose timers can be used to produce PWM outputs. Each timer has independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1~4 Hall sensors. Each timer can produce PWM outputs or be seen as a simple time reference.

Basic Timer (TIM6/TIM7)

Each timer contains one 16-bit auto-load up counter and one 16-bit prescaler. Their counters can be frozen in the debug mode.

Independent watchdog (IWDG)

The independent watchdog contains one 12-bit down counter and one 8-bit prescaler. There is an internal independent 40KHz clock oscillator. This oscillator operates independently from the master clock, so it can work in the Stop and Standby modes. It can be used to reset the entire system in the event of system failure or used as a free timer to provide timeout management for applications. The option bytes can be configured to boot watchdog via software or hardware. Their counters can be frozen in the debug mode.

Window watchdog (WWDG)

The window watchdog has one 7-bit down counter that can be set to run freely. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. Its counter can be frozen in the debug mode.

SysTick timer (Systick)

This timer is dedicated to the real-time operating system, but could also be used as a standard down counter. It features:

- A 24-bit downcounter
- Automatic reloading capability
- A maskable system interrupt can be produced when the counter is 0
- Programmable clock source

2.2.16 Real time clock (RTC)

The real time clock is a separate timer. RTC module has a set of counters that count continuously, which can provide the function of clock calendar in the corresponding software configuration. The current time and date of the system can be reset by changing values of the counters. The RTC module and the clock configuration system (RCC_BDCR register) resides in the backup area, which means RTC settings and time remain the same after the system is reset or the standby mode is awakened.

2.2.17 Backup registers

Backup registers include twenty 16-bit registers that are used to store user application data. They reside in the backup area and remain powered by VBAT even when the VDD is cut off. They will not be reset even when the system is woken up in the standby mode, or when the system is reset or when the power is reset.

2.2.18 GPIO

Each GPIO pin can be configured by software as an output port (push-pull or open-drain), an input port (with or without pull-up/pull-down), or an alternate peripheral port. Most GPIO pins are shared with alternate digital or analog peripherals.

If required, the peripheral function of the I/O pins can be locked with a specific operation to avoid accidental writing into the I/O register.

2.2.19 UART

UART interfaces support LIN master-slave capability, and they are compatible with the ISO7816 smart card mode. The supported lengths of output data from UART interfaces can be 5 bits, 6 bits, 7 bits, 8 bits and 9 bits, which are all configurable.

All UART interfaces can be served by the DMA controller.

2.2.20 I2C

I2C bus interfaces operate in the multi-master mode or slave mode and they support the standard mode and fast mode.

I2C interfaces support 7-bit or 10-bit addressing.

2.2.21 SPI

SPI interfaces can be configured to 1~32 bits per frame in the slave or master mode. The maximum rate is 24Mbps in the master mode and 12Mbps in the slave mode.

All the SPI interfaces can be served by the DMA controller.

2.2.22 I2S

Sharing three pins with SPI interfaces, the I2S interfaces operate in master or slave mode with half-duplex communication. There are three flags for I2S: the underrun flag in the Tx mode (Slave only), the overrun flag in the Rx mode (Master and Slave) and the frame error flag in the Rx/Tx mode (Slave only).

An 8-bit programmable prescaler is provided to reach accurate audio sampling frequency (8KHz to 192KHz).

The data can be in the 16-bit, 24-bit or 32-bit format. The packet frame is fixed to the 16-

bit format (16-bit data frame) or 32-bit format (16-bit, 24-bit or 32-bit data frame).

2.2.23 CAN

The CAN interface is compatible with specifications 2.0A and 2.0B (active), with bit rate up to 1 Mbps. It can receive and send standard frames with 11-bit identifiers or extended frames with 29-bit identifiers.

2.2.24 USB FS OTG

A device controller compatible with full-speed USB OTG is built into the product, following the full-speed USB (12Mbps) standard. The endpoints can be configured by the software. The controller is allowed to be used as a master or a slave.

Note: when USB function is enabled, the pins that USB_VBUS, USB_ID, USBDM and USBDP locate must be used as USB function, refer to Table 3-1 for detail pin assignment table.

2.2.25 SDIO

A device controller compatible with SD/SDIO/MMC is built into the product, usable for controlling the external SD/SDIO/MMC card and communicating with them as a master.

- Compatible with the SD memory card 1.0/1.1 (high speed)/2.0 (SDHC)
- Compatible with the SDIO memory card 1.1.0
- Compatible with the MMC system 2.0 ~ 4.2

2.2.26 FSMC

FSMC supports several types of external memories, including SRAM, PSRAM and NOR Flash. FSMC connects with most graphic LCD controllers seamlessly. It supports the 8080/6800 mode and adapts to specific LCD interfaces flexibly.

2.2.27 ADC

The product is embedded with three 12-bit analog-to-digital converters (ADCs) which has up to 21 external channels and is available for single-shot, one-cycle and continuous scan conversions. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs. All ADCs can be served by the DMA controller.

The analog watchdog function allows very precise monitoring of one or all selected channels. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timers (TIMx) and advanced control timers can be cascaded internally to the trigger of the ADC respectively. The application can synchronize the ADC conversion with the clock.

Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.28 DAC

The DAC module is a 12-bit digital-to-analog converter with digital input and voltage output.

The DAC can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller. In 12-bit mode, the data could be left- or right-aligned. The DAC has two output channels, each with an independent converter, to operate in the dual DAC mode.

2.2.29 COMP

The product has two built-in comparators, which can be used independently (suitable for I/O ports on all terminals) or in combination with the timer. COMPs are used for a variety of functions, including:

- Trigger wake-up events in the low-power modes by analog signals
- Adjust the analog signal
- Combine with PWM outputs from timers to form a cycle-by-cycle current control loop
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Alternate I/O pins
  - The internal comparison voltage CRV can be VDDA or the partial voltage value of the internal reference voltage
- Alternate I/O pins
- The internal comparison voltage CRV can be VDDA or the partial voltage value of the internal reference voltage
  - Capture event
  - OCref_clr event (cycle-by-cycle current control)
- Break event to shut off PWM rapidly

2.2.30 CRC

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. Within the scope of EN/IEC60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps calculate the software signature in real time and compare it to the signature generated when linking to and generating the software.

2.2.31 SWD and JTAG

The Arm-standard JTAG interface and two-wire serial debug port (SW-DP) are embedded.

3 Pinout and assignment

3.1 Pinout diagram

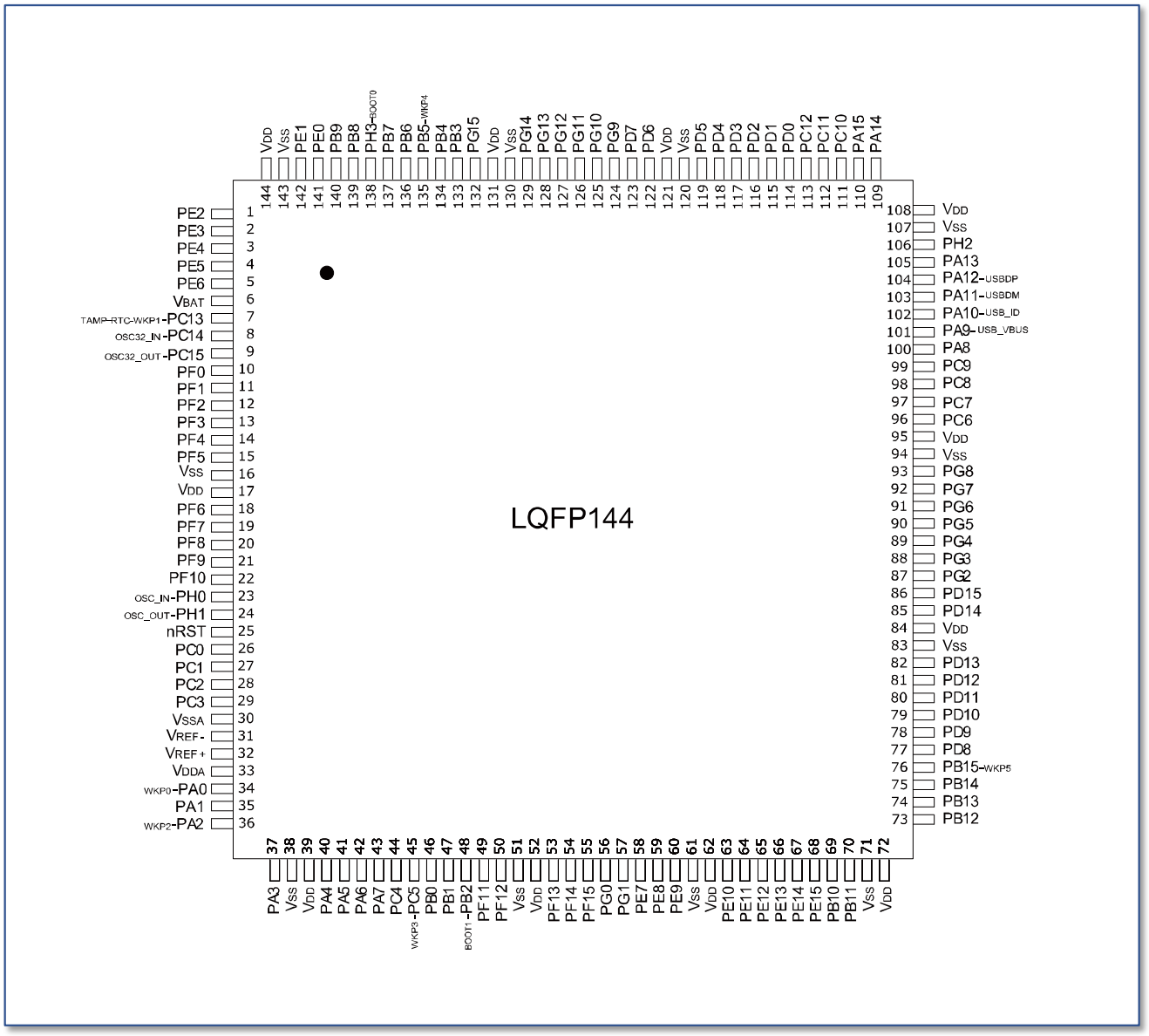

Figure 3-1 LQFP144 pinout diagram

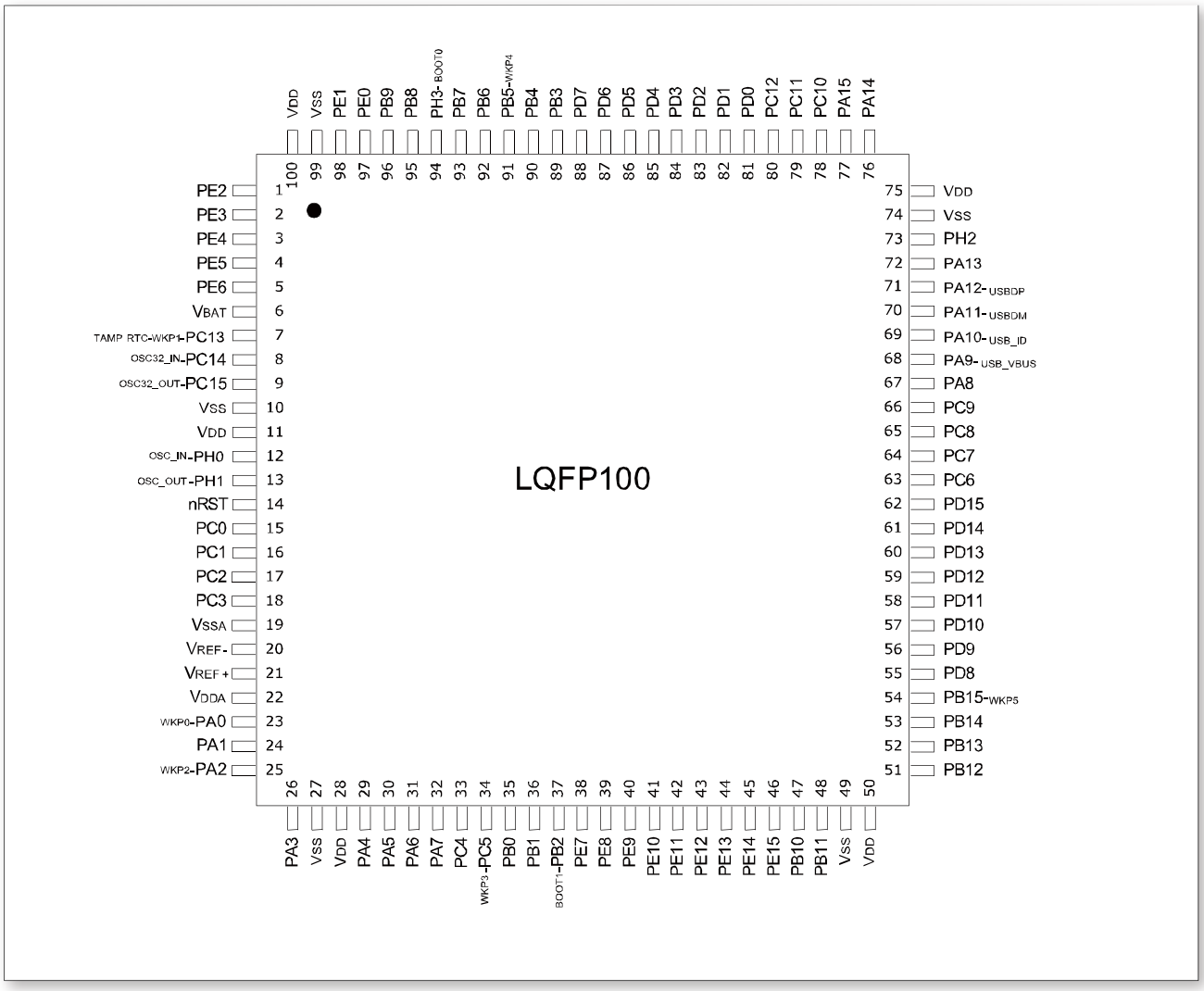

Figure 3-2 LQFP100 pinout diagram

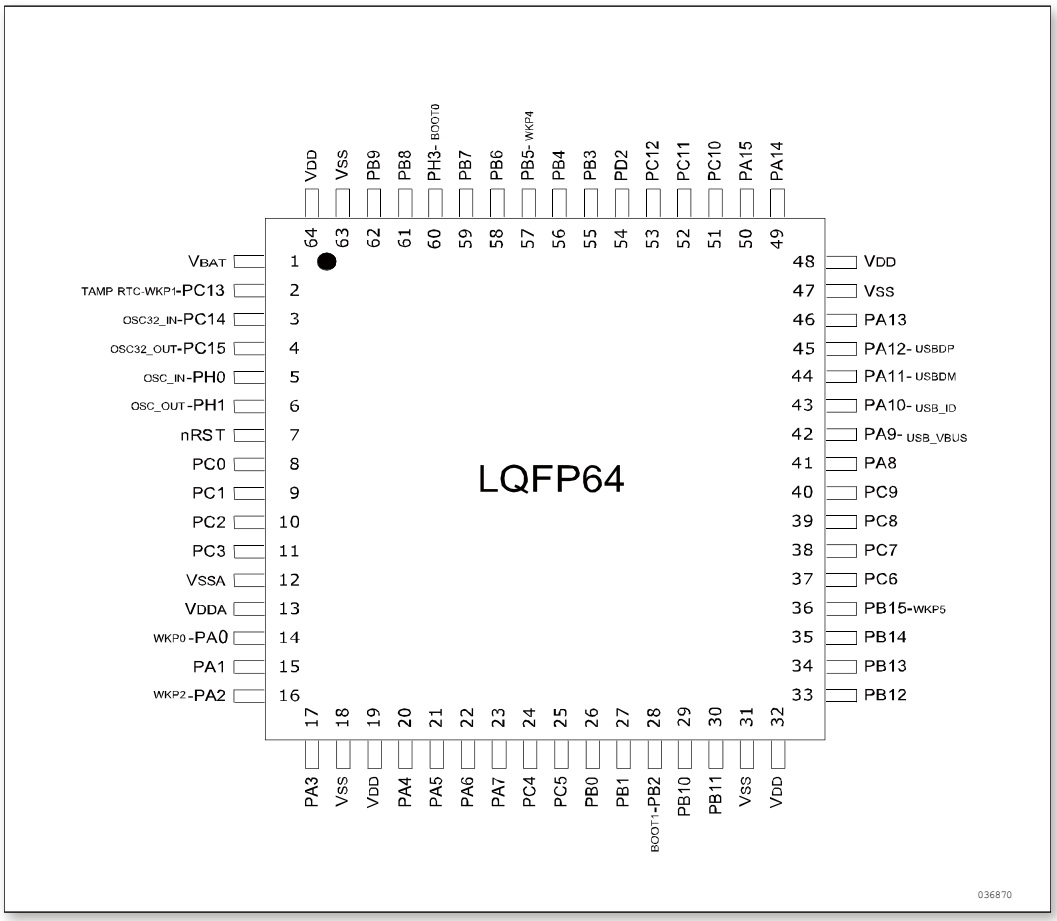

Figure 3-3 LQFP64 pinout diagram

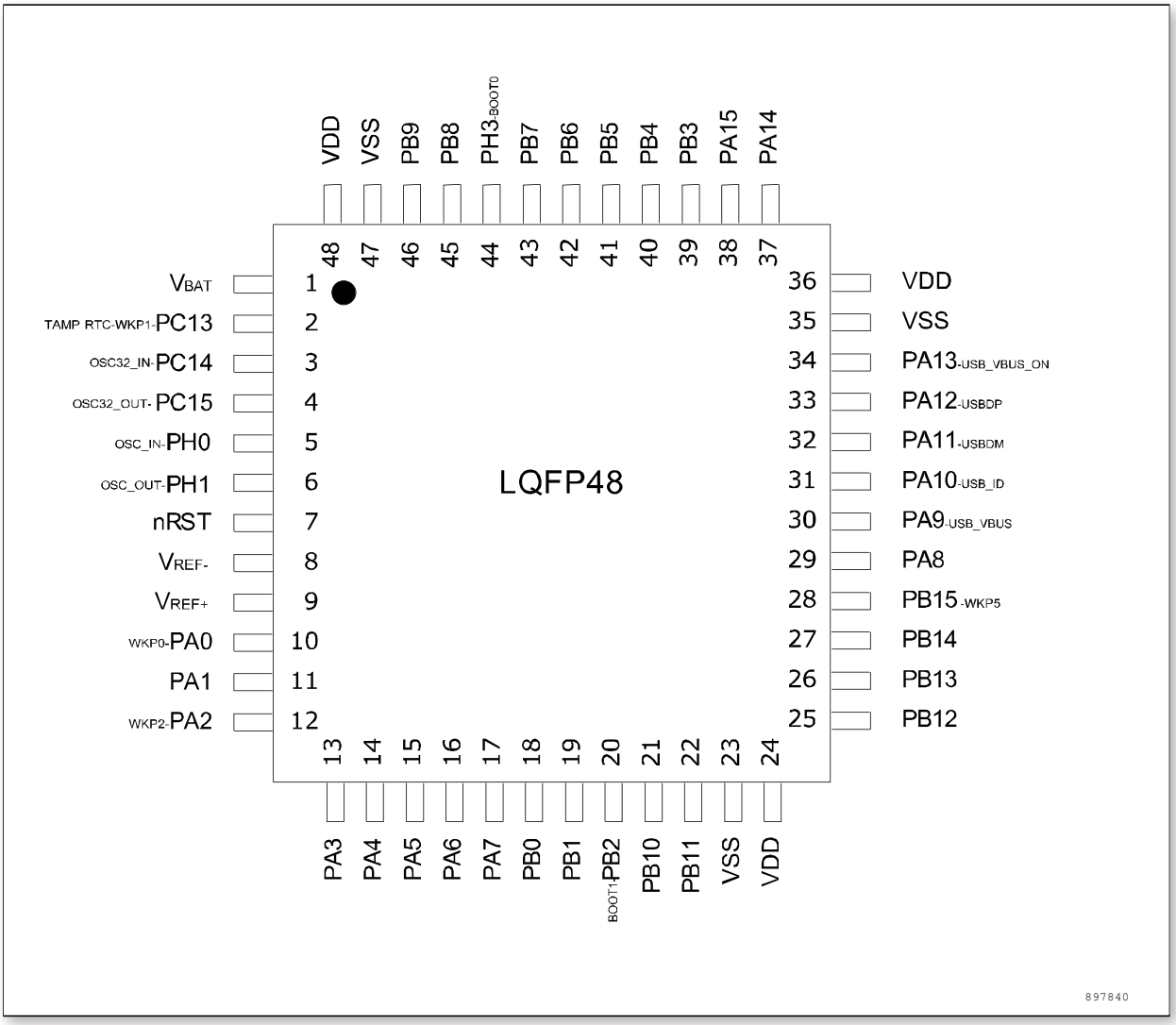

Figure 3-4 LQFP48 pinout diagram

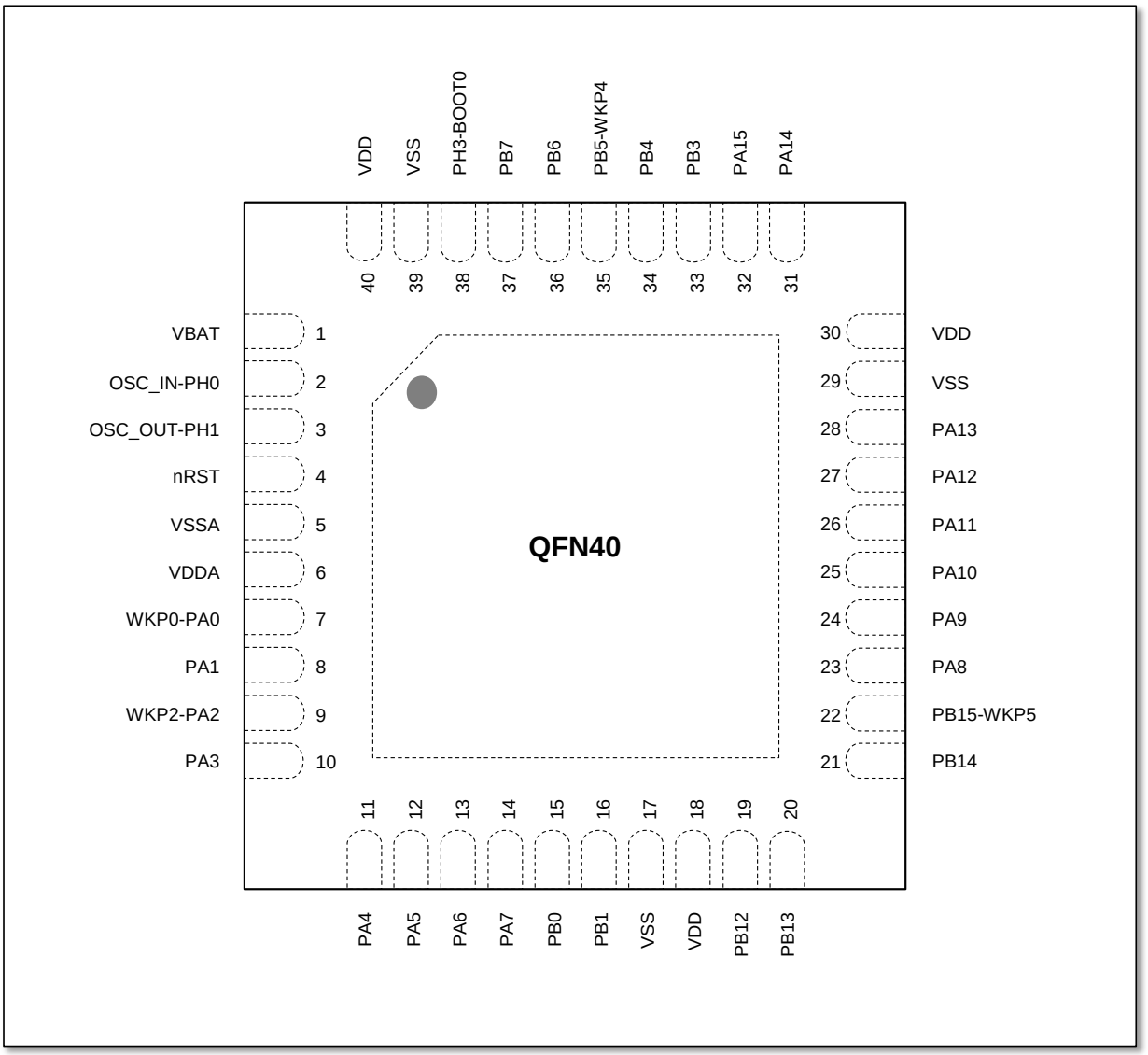

Figure 3-5 QFN40 pinout diagram

3.2 Pin assignment

Table 3-1 Pin assignment table

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
1	1	-	-	-	PE2	I/O	TC	PE2	SPI2_SCK I2S2_CK FMC_A23	-
2	2	-	-	-	PE3	I/O	TC	PE3	SPI2_NSS I2S2_WS FMC_A19	-
3	3	-	-	-	PE4	I/O	TC	PE4	SPI2_NSS I2S2_WS FMC_A20	-
4	4	-	-	-	PE5	I/O	TC	PE5	I2C2_SCL SPI2_MISO I2S2_MCK FMC_A21	-
5	5	-	-	-	PE6	I/O	TC	PE6	I2C2_SDA SPI2_MOSI I2S2_SD FMC_A22	-
6	6	1	1	1	VBAT	S	-	VBAT	-	-
7	7	2	2	-	PC13 WKP1	I/O	TC	PC13	-	TAMP-RTC
8	8	3	3	-	PC14	I/O	TC	PC14	-	OSC32_IN
9	9	4	4	-	PC15	I/O	TC	PC15	-	OSC32_OUT
10	-	-	-	-	PF0	I/O	TC	PF0	FMC_A0	-
11	-	-	-	-	PF1	I/O	TC	PF1	FMC_A1	-
12	-	-	-	-	PF2	I/O	TC	PF2	FMC_A2	-
13	-	-	-	-	PF3	I/O	TC	PF3	FMC_A3	-
14	-	-	-	-	PF4	I/O	TC	PF4	FMC_A4	-
15	-	-	-	-	PF5	I/O	TC	PF5	FMC_A5	-
16	10	-	-	-	VSS	S	-	VSS		-
17	11	-	-	-	VDD	S	-	VDD		-
18	-	-	-	-	PF6	I/O	TC	PF6		ADC3_IN4
19	-	-	-	-	PF7	I/O	TC	PF7		ADC3_IN5
20	-	-	-	-	PF8	I/O	TC	PF8		ADC3_IN6
21	-	-	-	-	PF9	I/O	TC	PF9		ADC3_IN7
22	-	-	-	-	PF10	I/O	TC	PF10		ADC3_IN8
23	12	5	5	2	PH0	I/O	TC	PH0		OSC_IN
24	13	6	6	3	PH1	I/O	TC	PH1		OSC_OUT
25	14	7	7	4	nRST	I/O	-	nRST		-
26	15	8	-	-	PC0	I/O	TC	PC0	I2C1_SCL	ADC123_IN10
27	16	9	-	-	PC1	I/O	TC	PC1	I2C1_SDA	ADC123_IN11
28	17	10	-	-	PC2	I/O	TC	PC2	I2C2_SCL SPI2_MISO I2S2_MCK	ADC123_IN12

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
29	18	11	-	-	PC3	I/O	TC	PC3	I2C2_SDA SPI2_MOSI I2S2_SD	ADC123_IN13
30	19	12	8	5	VSSA	S	-	VSSA		-
31	20	-	-	5	VREF−	S	-	VREF−		-
32	21	-	-	6	VREF+	S	-	VREF+		-
33	22	13	9	6	VDDA	S	-	VDDA		-
34	23	14	10	7	PA0 WKP0	I/O	TC	PA0	TIM2_CH1 TIM2_ETR TIM5_CH1 TIM8_ETR UART2_CTS UART4_TX	ADC123_IN0 COMP12_INP0 COMP1_INM2
35	24	15	11	8	PA1	I/O	TC	PA1	TIM2_CH2 TIM5_CH2 UART2_RTS UART4_RX	ADC123_IN1 COMP12_INP1
36	25	16	12	9	PA2 WKP2	I/O	TC	PA2	TIM2_CH3 TIM5_CH3 UART2_TX CPT2_OUT	ADC123_IN2 COMP12_INP2 COMP2_INM2
37	26	17	13	10	PA3	I/O	TC	PA3	TIM2_CH4 TIM5_CH4 UART2_RX	ADC123_IN3 COMP12_INP3
38	27	18	-	-	VSS	S	-	VSS		-
39	28	19	-	-	VDD	S	-	VDD		-
40	29	20	14	11	PA4	I/O	TC	PA4	SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS UART5_TX	ADC12_IN4 DAC1_OUT COMP12_INM0
41	30	21	15	12	PA5	I/O	TC	PA5	TIM2_CH1 TIM2_ETR TIM8_CH1N SPI1_SCK I2S1_CK UART5_RX	ADC12_IN5 DAC2_OUT COMP12_INM1
42	31	22	16	13	PA6	I/O	TC	PA6	TIM1_BKIN TIM3_CH1 TIM8_BKIN SPI1_MISO I2S1_MCK CPT1_OUT	ADC12_IN6
43	32	23	17	14	PA7	I/O	TC	PA7	TIM1_CH1N TIM3_CH2 TIM8_CH1N SPI1_MOSI I2S1_SD CRS_SYNC	ADC12_IN7
44	33	24	-	-	PC4	I/O	TC	PC4	-	ADC23_IN14
45	34	25	-	-	PC5 WKP3	I/O	TC	PC5	-	ADC23_IN15
46	35	26	18	15	PB0	I/O	TC	PB0	TIM1_CH2N TIM3_CH3 TIM8_CH2N UART6_TX	ADC12_IN8

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
47	36	27	19	16	PB1	I/O	TC	PB1	TIM1_CH3N TIM3_CH4 TIM8_CH3N UART6_RX	ADC123_IN9
48	37	28	20	-	PB2	I/O	TC	PB2		BOOT1
49	-	-	-	-	PF11	I/O	TC	PF11		-
50	-	-	-	-	PF12	I/O	TC	PF12	FMC_A6	-
51	-	-	-	-	VSS	S	-	VSS		-
52	-	-	-	-	VDD	S	-	VDD		-
53	-	-	-	-	PF13	I/O	TC	PF13	FMC_A7	-
54	-	-	-	-	PF14	I/O	TC	PF14	FMC_A8	-
55	-	-	-	-	PF15	I/O	TC	PF15	FMC_A9	-
56	-	-	-	-	PG0	I/O	TC	PG0	FMC_A10	-
57	-	-	-	-	PG1	I/O	TC	PG1	FMC_A11	-
58	38	-	-	-	PE7	I/O	TC	PE7	TIM1_ETR UART7_RX FMC_DA4	-
59	39	-	-	-	PE8	I/O	TC	PE8	TIM1_CH1N UART7_TX FMC_DA5	-
60	40	-	-	-	PE9	I/O	TC	PE9	TIM1_CH1 FMC_DA6	-
61	-	-	-	17	VSS	S	-	VSS		-
62	-	-	-	-	VDD	S	-	VDD		-
63	41	-	-	-	PE10	I/O	TC	PE10	TIM1_CH2N FMC_DA7	-
64	42	-	-	-	PE11	I/O	TC	PE11	TIM1_CH2 SPI1_NSS I2S1_WS FMC_DA8	-
65	43	-	-	-	PE12	I/O	TC	PE12	TIM1_CH3N SPI1_SCK I2S1_CK FMC_DA9	-
66	44	-	-	-	PE13	I/O	TC	PE13	TIM1_CH3 SPI1_MISO I2S1_MCK FMC_DA10	-
67	45	-	-	-	PE14	I/O	TC	PE14	TIM1_CH4 SPI1_MOSI I2S1_SD FMC_DA11	-
68	46	-	-	-	PE15	I/O	TC	PE15	TIM1_BKIN FMC_DA12	-
69	47	29	21	-	PB10	I/O	TC	PB10	TIM2_CH3 I2C2_SCL SPI2_SCK I2S2_CK UART3_TX	-
70	48	30	22	-	PB11	I/O	TC	PB11	TIM2_CH4 I2C2_SDA UART3_RX	-
71	49	31	23	-	VSS	S	-	VSS		-

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
72	50	32	24	18	VDD	S	-	VDD		-
73	51	33	25	19	PB12	I/O	TC	PB12	TIM1_BKIN SPI2_NSS I2S2_WS	-
74	52	34	26	20	PB13	I/O	TC	PB13	TIM1_CH1N SPI2_SCK I2S2_CK UART3_CTS	-
75	53	35	27	21	PB14	I/O	TC	PB14	TIM1_CH2N TIM8_CH2N SPI2_MISO I2S2_MCK UART3_RTS	-
76	54	36	28	22	PB15 WKP5	I/O	TC	PB15	TIM1_CH3N TIM8_CH3N SPI2_MOSI I2S2_SD	-
77	55	-	-	-	PD8	I/O	TC	PD8	UART3_TX FMC_DA13	-
78	56	-	-	-	PD9	I/O	TC	PD9	UART3_RX FMC_DA14	-
79	57	-	-	-	PD10	I/O	TC	PD10	I2C1_SCL FMC_DA15	-
80	58	-	-	-	PD11	I/O	TC	PD11	I2C1_SDA UART3_CTS FMC_A16	-
81	59	-	-	-	PD12	I/O	TC	PD12	TIM4_CH1 SPI3_SCK I2S3_CK UART3_RTS FMC_A17	-
82	60	-	-	-	PD13	I/O	TC	PD13	TIM4_CH2 SPI3_MISO I2S3_MCK FMC_A18	-
83	-	-	-	-	VSS	S	-	VSS		-
84	-	-	-	-	VDD	S	-	VDD		-
85	61	-	-	-	PD14	I/O	TC	PD14	TIM4_CH3 SPI3_MOSI FMC_DA0	-
86	62	-	-	-	PD15	I/O	TC	PD15	TIM4_CH4 SPI3_NSS I2S3_WS FMC_DA1	-
87	-	-	-	-	PG2	I/O	TC	PG2	FMC_A12	-
88	-	-	-	-	PG3	I/O	TC	PG3	FMC_A13	-
89	-	-	-	-	PG4	I/O	TC	PG4	FMC_A14	-
90	-	-	-	-	PG5	I/O	TC	PG5	FMC_A15	-
91	-	-	-	-	PG6	I/O	TC	PG6		-
92	-	-	-	-	PG7	I/O	TC	PG7		-
93	-	-	-	-	PG8	I/O	TC	PG8		-
94	-	-	-	-	VSS	S	-	VSS		-
95	-	-	-	-	VDD	S	-	VDD		-

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
96	63	37	-	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM8_CH1 I2C1_SCL SPI2_MISO I2S2_MCK UART6_TX	-
97	64	38	-	-	PC7	I/O	TC	PC7	TIM3_CH2 TIM8_CH2 I2C1_SDA SPI3_MISO I2S3_MCK UART6_RX	-
98	65	39	-	-	PC8	I/O	TC	PC8	TIM3_CH3 TIM8_CH3 I2C2_SCL SDIO_D0	-
99	66	40	-	-	PC9	I/O	TC	PC9	MCO2 TIM3_CH4 TIM8_CH4 I2C2_SDA SDIO_D1	-
100	67	41	29	23	PA8	I/O	TC	PA8	MCO1 TIM1_CH1	-
101	68	42	30	24	PA9	I/O	TC	PA9	TIM1_CH2 I2C1_SCL UART1_TX	USB_VBUS(3)
102	69	43	31	25	PA10	I/O	TC	PA10	TIM1_CH3 I2C1_SDA UART1_RX	USB_ID(3)
103	70	44	32	26	PA11	I/O	TC	PA11	TIM1_CH4 UART1_CTS CPT1_OUT CAN1_RX	USBDM(3)
104	71	45	33	27	PA12	I/O	TC	PA12	TIM1_ETR UART1_RTS CPT2_OUT CAN1_TX	USBDP(3)
105	72	46	34	28	PA13	I/O (5)	TC	PA13	JTMS_SWDIO USB_VBUS_ON	-
106	73	-	-	-	PH2	I/O	TC	PH2		-
107	74	47	35	29	VSS	S	-	VSS		-
108	75	48	36	30	VDD	S	-	VDD		-
109	76	49	37	31	PA14	I/O (5)	TC	PA14	JTCK_SWCLK I2C1_SDA	-
110	77	50	38	32	PA15	I/O (5)	TC	PA15	JTDI TIM2_CH1 TIM2_ETR I2C1_SCL SPI1_NSS I2S1_WS SPI3_NSS I2S3_WS	-
111	78	51	-	-	PC10	I/O	TC	PC10	SPI3_SCK I2S3_CK UART3_TX UART4_TX SDIO_D2	-
112	79	52	-	-	PC11	I/O	TC	PC11	SPI3_MISO I2S3_MCK UART3_RX UART4_RX SDIO_D3	-

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
113	80	53	-	-	PC12	I/O	TC	PC12	SPI3_MOSI UART5_TX SDIO_CK	-
114	81	-	-	-	PD0	I/O	TC	PD0	UART8_TX CAN1_RX FMC_DA2	-
115	82	-	-	-	PD1	I/O	TC	PD1	UART8_RX CAN1_TX FMC_DA3	-
116	83	54	-	-	PD2	I/O	TC	PD2	TIM3_ETR UART5_RX SDIO_CMD	-
117	84	-	-	-	PD3	I/O	TC	PD3	SPI2_SCK I2S2_CK UART2_CTS FMC_CLK	-
118	85	-	-	-	PD4	I/O	TC	PD4	SPI3_SCK I2S3_CK UART2_RTS FMC_NOE	-
119	86	-	-	-	PD5	I/O	TC	PD5	SPI3_MISO I2S3_MCK UART2_TX FMC_NWE	-
120	-	-	-	-	VSS	S	-	VSS	-	-
121	-	-	-	-	VDD	S	-	VDD	-	-
122	87	-	-	-	PD6	I/O	TC	PD6	SPI3_MOSI I2S3_SD UART2_RX FMC_NWAIT	-
123	88	-	-	-	PD7	I/O	TC	PD7	SPI3_NSS I2S3_WS FMC_NE1	-
124	-	-	-	-	PG9	I/O	TC	PG9	FMC_NE2	-
125	-	-	-	-	PG10	I/O	TC	PG10	FMC_NE3	-
126	-	-	-	-	PG11	I/O	TC	PG11	-	-
127	-	-	-	-	PG12	I/O	TC	PG12	FMC_NE4	-
128	-	-	-	-	PG13	I/O	TC	PG13	FMC_A24	-
129	-	-	-	-	PG14	I/O	TC	PG14	FMC_A25	-
130	-	-	-	-	VSS	S	-	VSS	-	-
131	-	-	-	-	VDD	S	-	VDD	-	-
132	-	-	-	-	PG15	I/O	TC	PG15	-	-
133	89	55	39	33	PB3	I/O (5)	TC	PB3	JTDO TIM2_CH2 SPI1_SCK I2S1_CK SPI3_SCK I2S3_CK	-
134	90	56	40	34	PB4	I/O (5)	TC	PB4	NJTRST TIM3_CH1 SPI1_MISO I2S1_MCK SPI3_MISO I2S3_MCK	-

Pin ID					Name	Type (1)(4)	I/O level (2)	Main function	Multiplex function	Additional function
LQFP144	LQFP100	LQFP64	LQFP48	QFN40						
135	91	57	41	35	PB5 WKP4	I/O	TC	PB5	TIM3_CH2 SPI1_MOSI I2S1_SD SPI3_MOSI I2S3_SD	-
136	92	58	42	36	PB6	I/O	TC	PB6	TIM4_CH1 I2C1_SCL UART1_TX UART7_TX	-
137	93	59	43	37	PB7	I/O	TC	PB7	TIM4_CH2 I2C1_SDA UART1_RX UART7_RX FMC_NADV	-
138	94	60	44	38	PH3	I/O (6)	TC	PH3	-	BOOT0
139	95	61	45	-	PB8	I/O	TC	PB8	TIM4_CH3 I2C1_SCL CPT1_OUT CAN1_RX	-
140	96	62	46	-	PB9	I/O	TC	PB9	TIM4_CH4 I2C1_SDA SPI2_NSS I2S2_WS CPT2_OUT CAN1_TX	-
141	97	-	-	-	PE0	I/O	TC	PE0	TIM4_ETR UART8_RX FMC_NBL0	-
142	98	-	-	-	PE1	I/O	TC	PE1	UART8_TX FMC_NBL1	-
143	99	63	47	39	VSS	S	-	VSS	-	-
144	100	64	48	40	VDD	S	-	VDD	-	-

1. I = Input, O = Output, S = Power Supply, HiZ = High Resistance
2. TC: Standard IO, input signal does not exceed VDD voltage.
3. When USB function is enabled, the pins that USB_VBUS, USB_ID, USBDM and USBDP locate can only be used as USB function.
4. Unless otherwise noted, I/O type pins other than the NRST and JTAG related pin are in a floating input state after power-up with no internal pull-up or pull-down enabled, and if there is no external pull-up or pull-down, the pin level is floating.
5. After reset, for JTAG related pins, the internal pull-up resistors of the PA13/JTMS_SWDIO, PB4/NJTRST, PA15/JTDI pins and the internal pull-down resistor of the PA14/JTCK_SWCLK pin are enabled, and if there is no external pull-up or pull-down, the pin level is pulled up to VDD voltage or pulled down to VSS voltage. The PB3/JTDO pin is floating.
6. After reset, the internal pull-down resistor of the BOOT0 pin keeps the pin in the VSS voltage state.

3.3 Pin multiplexing

Table 3-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	TIM2_CH1 TIM2_ETR	TIM5_CH1	TIM8_ETR		-	-	UART2_CTS
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	UART2_RTS
PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	UART2_TX
PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	UART2_RX
PA4	-	-	-	-	-	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-
PA5		TIM2_CH1 TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK I2S1_CK	-	-
PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO I2S1_MCK	-	-
PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI I2S1_SD	-	-
PA8	MCO1	TIM1_CH1	-	-	-	-	-	-
PA9	-	TIM1_CH2	-	-	I2C1_SCL	-	-	UART1_TX
PA10	-	TIM1_CH3	-	-	I2C1_SDA	-	-	UART1_RX
PA11	-	TIM1_CH4	-	-	-	-	-	UART1_CTS
PA12	-	TIM1_ETR	-	-	-	-	-	UART1_RTS
PA13	JTMS_SWDIO	-	-	-	-	-	-	-
PA14	JTCK_SWCLK	-	-	-	I2C1_SDA	-	-	-
PA15	JTDI	TIM2_CH1 TIM2_ETR	-	-	I2C1_SCL	SPI1_NSS I2S1_WS	SPI3_NSS I2S3_WS	-

Table 3-3 PA port multiplexing AF8-AF12

Pin	AF8	AF9	AF10	AF11	AF12
PA0	UART4_TX	-	-	-	-
PA1	UART4_RX	-	-	-	-
PA2	CPT2_OUT	-	-	-	-
PA3	-	-	-	-	-
PA4	UART5_TX	-	-	-	-
PA5	UART5_RX	-	-	-	-
PA6	CPT1_OUT	-	-	-	-
PA7	-	-	CRS_SYNC	-	-
PA8	-	-	-	-	-
PA9	-	-	-	-	-
PA10	-	-	-	-	-
PA11	CPT1_OUT	CAN1_RX	-	-	-
PA12	CPT2_OUT	CAN1_TX	-	-	-
PA13	-	-	USB_VBUS_ON	-	-
PA14	-	-	-	-	-
PA15	-	-	-	-	-

Table 3-4 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-
PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-
PB2	-	-	-	-	-	-	-	-
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK I2S1_CK	SPI3_SCK I2S3_CK	-
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO I2S1_MCK	SPI3_MISO I2S3_MCK	-
PB5	-	-	TIM3_CH2	-	-	SPI1_MOSI I2S1_SD	SPI3_MOSI I2S3_SD	-
PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	UART1_TX
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	UART1_RX
PB8	-	-	TIM4_CH3	-	I2C1_SCL	-	-	-
PB9	-	-	TIM4_CH4	-	I2C1_SDA	SPI2_NSS I2S2_WS	-	-
PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	UART3_TX
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	UART3_RX
PB12	-	TIM1_BKIN	-	-	-	SPI2_NSS I2S2_WS	-	-
PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_CK	-	UART3_CTS
PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO I2S2_MCK	-	UART3_RTS
PB15	-	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-

Table 3-5 PB port multiplexing AF8-AF12

Pin	AF8	AF9	AF10	AF11	AF12
PB0	UART6_TX	-	-	-	-
PB1	UART6_RX	-	-	-	-
PB2	-	-	-	-	-
PB3	-	-	-	-	-
PB4	-	-	-	-	-
PB5	-	-	-	-	-
PB6	UART7_TX	-	-	-	-
PB7	UART7_RX	-	-	-	FMC_NADV
PB8	CPT1_OUT	CAN1_RX	-	-	-
PB9	CPT2_OUT	CAN1_TX	-	-	-
PB10	-	-	-	-	-
PB11	-	-	-	-	-
PB12	-	-	-	-	-
PB13	-	-	-	-	-
PB14	-	-	-	-	-
PB15	-	-	-	-	-

Table 3-6 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	-	-	-	I2C1_SCL	-	-	-
PC1	-	-	-	-	I2C1_SDA	-	-	-
PC2	-	-	-	-	I2C2_SCL	SPI2_MISO I2S2_MCK	-	-
PC3	-	-	-	-	I2C2_SDA	SPI2_MOSI I2S2_SD	-	-
PC4	-	-	-	-	-	-	-	-
PC5	-	-	-	-	-	-	-	-
PC6	-	-	TIM3_CH1	TIM8_CH1	I2C1_SCL	SPI2_MISO I2S2_MCK	-	-
PC7	-	-	TIM3_CH2	TIM8_CH2	I2C1_SDA	SPI3_MISO I2S3_MCK	-	-
PC8	-	-	TIM3_CH3	TIM8_CH3	I2C2_SCL	-	-	-
PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C2_SDA	-	-	-
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	UART3_TX
PC11	-	-	-	-	-	-	SPI3_MISO I2S3_MCK	UART3_RX
PC12	-	-	-	-	-	-	SPI3_MOSI	-
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 3-7 PC port multiplexing AF8-AF12

Pin	AF8	AF9	AF10	AF11	AF12
PC0	-	-	-	-	-
PC1	-	-	-	-	-
PC2	-	-	-	-	-
PC3	-	-	-	-	-
PC4	-	-	-	-	-
PC5	-	-	-	-	-
PC6	UART6_TX	-	-	-	-
PC7	UART6_RX	-	-	-	-
PC8	-	-	-	-	SDIO_D0
PC9	-	-	-	-	SDIO_D1
PC10	UART4_TX	-	-	-	SDIO_D2
PC11	UART4_RX	-	-	-	SDIO_D3
PC12	UART5_TX	-	-	-	SDIO_CK
PC13	-	-	-	-	-
PC14	-	-	-	-	-
PC15	-	-	-	-	-

Table 3-8 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	-	-	-	-	-	-	-
PD1	-	-	-	-	-	-	-	-
PD2	-	-	TIM3_ETR	-	-	-	-	-
PD3	-	-	-	-	-	SPI2_SCK I2S2_CK	-	UART2_CTS
PD4	-	-	-	-	-	SPI3_SCK I2S3_CK	-	UART2_RTS
PD5	-	-	-	-	-	SPI3_MISO I2S3_MCK	-	UART2_TX
PD6	-	-	-	-	-	SPI3_MOSI I2S3_SD	-	UART2_RX
PD7	-	-	-	-	-	SPI3_NSS I2S3_WS	-	-
PD8	-	-	-	-	-	-	-	UART3_TX
PD9	-	-	-	-	-	-	-	UART3_RX
PD10	-	-	-	-	I2C1_SCL	-	-	-
PD11	-	-	-	-	I2C1_SDA	-	-	UART3_CTS
PD12	-	-	TIM4_CH1	-	-	-	SPI3_SCK I2S3_CK	UART3_RTS
PD13	-	-	TIM4_CH2	-	-	-	SPI3_MISO I2S3_MCK	-
PD14	-	-	TIM4_CH3	-	-	-	SPI3_MOSI	-
PD15	-	-	TIM4_CH4	-	-	-	SPI3_NSS I2S3_WS	-

Table 3-9 PD port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12
PD0	UART8_TX	CAN1_RX	-	-	FMC_DA2
PD1	UART8_RX	CAN1_TX	-	-	FMC_DA3
PD2	UART5_RX	-	-	-	SDIO_CMD
PD3	-	-	-	-	FMC_CLK
PD4	-	-	-	-	FMC_NOE
PD5	-	-	-	-	FMC_NWE
PD6	-	-	-	-	FMC_NWAIT
PD7	-	-	-	-	FMC_NE1
PD8	-	-	-	-	FMC_DA13
PD9	-	-	-	-	FMC_DA14
PD10	-	-	-	-	FMC_DA15
PD11	-	-	-	-	FMC_A16
PD12	-	-	-	-	FMC_A17
PD13	-	-	-	-	FMC_A18
PD14	-	-	-	-	FMC_DA0
PD15	-	-	-	-	FMC_DA1

Table 3-10 PE port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	-	-	TIM4_ETR	-	-	-	-	-
PE1	-	-	-	-	-	-	-	-
PE2	-	-	-	-	-	SPI2_SCK I2S2_CK	-	-
PE3	-	-	-	-	-	SPI2_NSS I2S2_WS	-	-
PE4	-	-	-	-	-	SPI2_NSS I2S2_WS	-	-
PE5	-	-	-	-	I2C2_SCL	SPI2_MIS O I2S2_MCK	-	-
PE6	-	-	-	-	I2C2_SDA	SPI2_MOS I I2S2_SD	-	-
PE7	-	TIM1_ETR	-	-	-	-	-	-
PE8	-	TIM1_CH1 N	-	-	-	-	-	-
PE9	-	TIM1_CH1	-	-	-	-	-	-
PE10	-	TIM1_CH2 N	-	-	-	-	-	-
PE11	-	TIM1_CH2	-	-	-	SPI1_NSS I2S1_WS	-	-
PE12	-	TIM1_CH3 N	-	-	-	SPI1_SCK I2S1_CK	-	-
PE13	-	TIM1_CH3	-	-	-	SPI1_MIS O I2S1_MCK	-	-
PE14	-	TIM1_CH4	-	-	-	SPI1_MOS I I2S1_SD	-	-
PE15	-	TIM1_BKI N	-	-	-	-	-	-

Table 3-11 PE port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12
PE0	UART8_RX	-	-	-	FMC_NBL0
PE1	UART8_TX	-	-	-	FMC_NBL1
PE2	-	-	-	-	FMC_A23
PE3	-	-	-	-	FMC_A19
PE4	-	-	-	-	FMC_A20
PE5	-	-	-	-	FMC_A21
PE6	-	-	-	-	FMC_A22
PE7	UART7_RX	-	-	-	FMC_DA4
PE8	UART7_TX	-	-	-	FMC_DA5
PE9	-	-	-	-	FMC_DA6
PE10	-	-	-	-	FMC_DA7
PE11	-	-	-	-	FMC_DA8
PE12	-	-	-	-	FMC_DA9
PE13	-	-	-	-	FMC_DA10
PE14	-	-	-	-	FMC_DA11
PE15	-	-	-	-	FMC_DA12

Table 3-12 PF port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12
PF0	-	-	-	-	FMC_A0
PF1	-	-	-	-	FMC_A1
PF2	-	-	-	-	FMC_A2
PF3	-	-	-	-	FMC_A3
PF4	-	-	-	-	FMC_A4
PF5	-	-	-	-	FMC_A5
PF6	-	-	-	-	-
PF7	-	-	-	-	-
PF8	-	-	-	-	-
PF9	-	-	-	-	-
PF10	-	-	-	-	-
PF11	-	-	-	-	-
PF12	-	-	-	-	FMC_A6
PF13	-	-	-	-	FMC_A7
PF14	-	-	-	-	FMC_A8
PF15	-	-	-	-	FMC_A9

Table 3-13 PG port multiplexing AF8-AF15

Pin	AF8	AF9	AF10	AF11	AF12
PG0	-	-	-	-	FMC_A10
PG1	-	-	-	-	FMC_A11
PG2	-	-	-	-	FMC_A12
PG3	-	-	-	-	FMC_A13
PG4	-	-	-	-	FMC_A14
PG5	-	-	-	-	FMC_A15
PG6	-	-	-	-	-
PG7	-	-	-	-	-
PG8	-	-	-	-	-
PG9	-	-	-	-	FMC_NE2
PG10	-	-	-	-	FMC_NE3
PG11	-	-	-	-	-
PG12	-	-	-	-	FMC_NE4
PG13	-	-	-	-	FMC_A24
PG14	-	-	-	-	FMC_A25
PG15	-	-	-	-	-

4 Electrical characteristics

4.1 Test condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

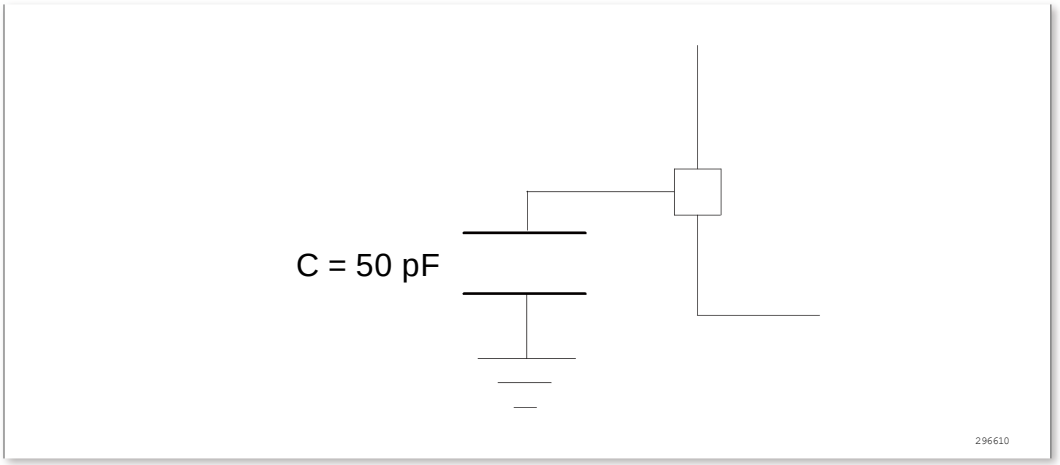

Figure 4-1 Load condition of the pin

4.1.2 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

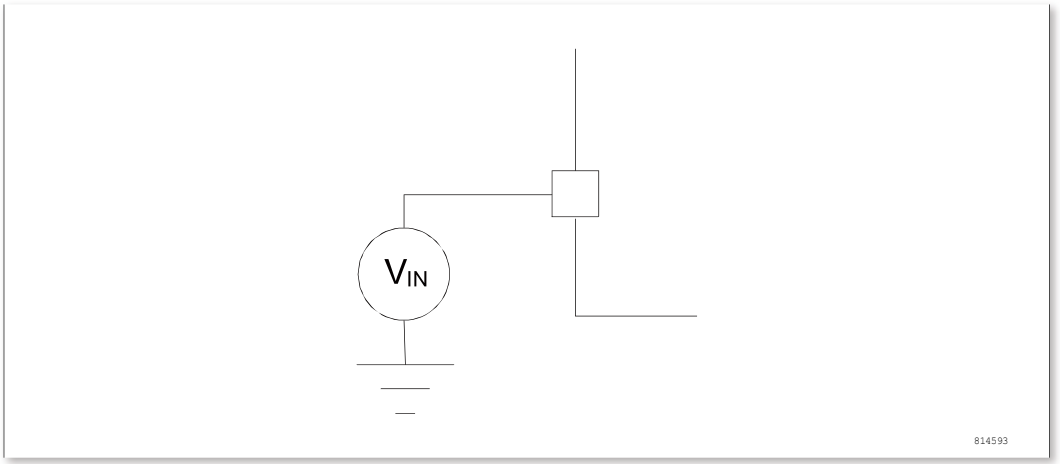

Figure 4-2 Pin input voltage

4.1.3 Power supply scheme

The power supply scheme is shown in the figure below.

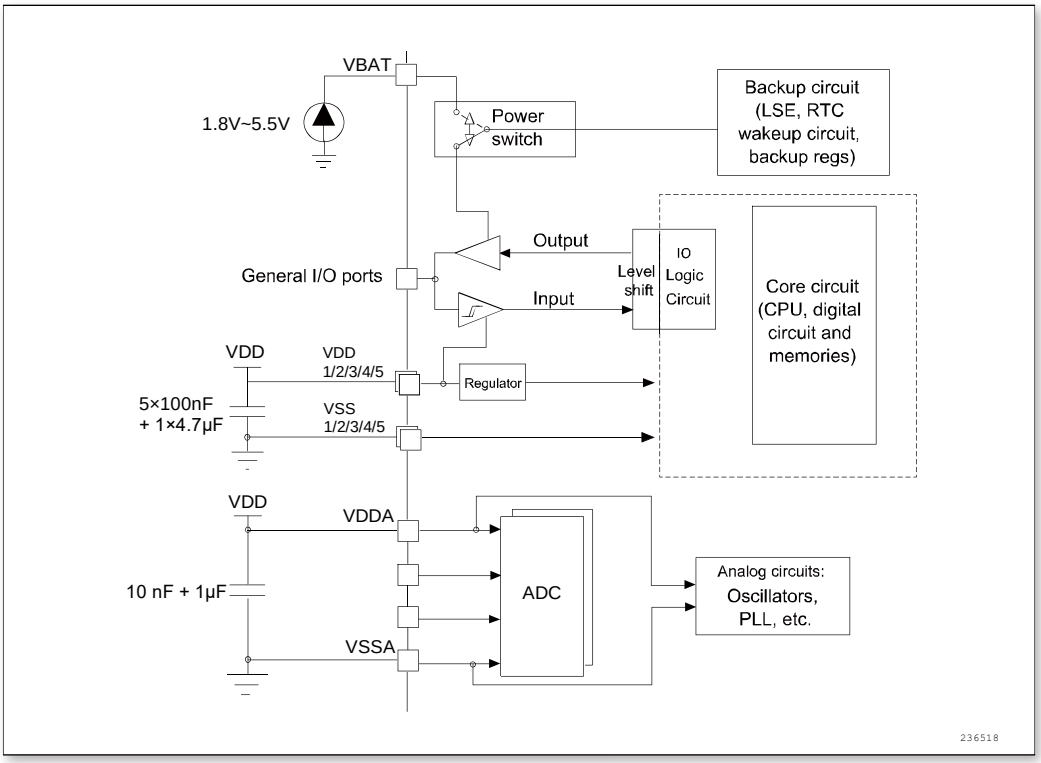

Figure 4-3 Power supply scheme

4.1.4 Current consumption measurement

The current consumption measurement on a pin is shown in the figure below

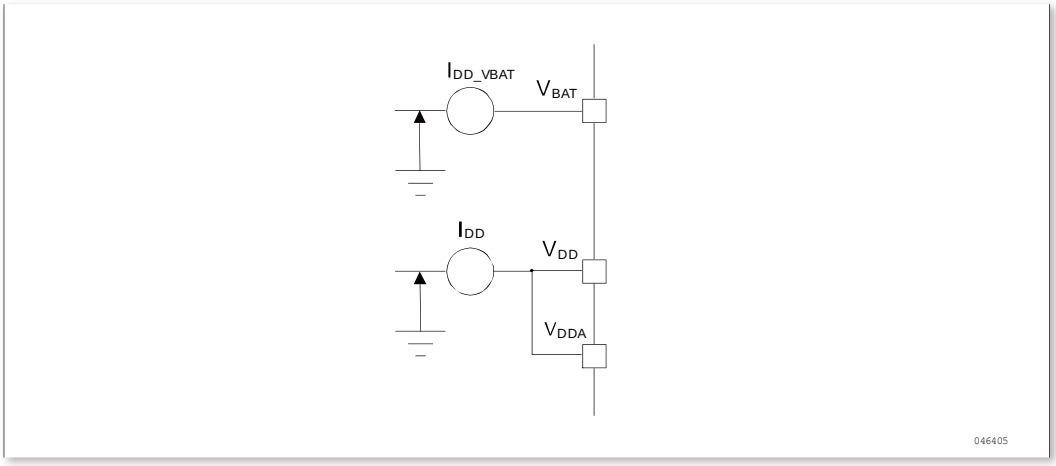

Figure 4-4 Current consumption measurement scheme

4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in (Table 4-1 and Table 4-2) may cause

permanent damage to the device. These are stress maximum ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Description	Min.	Max.	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	-0.3	5.8	V
V_{BAT}-V_{SSx}	Backup domain supply voltage	-0.3	5.8	
V_{IN}(2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to the table below for the maximum allowed injected current values.

Table 4-2 Current characteristics

Symbol	Description	Max.	Unit
$I_{VDD/VDDA}$(1)	Total current into sum of all V_{DD}/V_{DDA} power lines (source) (1)	+120	mA
$I_{VSS/VSSA}$(1)	Total current out of sum V_{SS}/V_{SSA} ground lines (sink) (1)	-120	
I_{IO}	Output current sunk by any I/O and control pins	+25	
	Output current sunk by any I/O and control pins	-25	
$I_{INJ(PIN)}$(2)(3)	Injected current on NRST pin	±5	
	Injected current on OSC_IN pin of HSE	±5	
$\sum I_{INJ(PIN)}$(6)	Total injected current on other pins (5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/pulled between two consecutive power supply pins referring to high pin count LQFP packages.
3. The negative injected current will interfere with the analog performance of the device.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When $V_{IN} > V_{DDA}$, a positive injected current is induced; when $V_{IN} < V_{SS}$, a negative injected current is induced. $I_{INJ(PIN)}$ must never be exceeded.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK3}	Internal AHB3 clock frequency	The core voltage should go up to 1.7V at 120M	-	96	120	MHz
f_{HCLK2}	Internal AHB2 clock frequency	The core voltage should go up to 1.7V at 120M	-	96	120	
f_{HCLK1}	Internal AHB1 clock frequency	The core voltage should go up to 1.7V at 120M	-	96	120	
f_{PCLK2}	Internal APB2 clock frequency	The core voltage should go up to 1.7V at 120M	-	96	120	
f_{PCLK1}	Internal APB1 clock frequency	The core voltage should go up to 1.7V at 120M	-	96	120	
V_{DD}	Digital operating voltage	-	2.0	3.3	5.5	V
V_{DDA}	Analog operating voltage (performance guaranteed)	Must be the same voltage as V_{DD} (1)	2.5	3.3	5.5	V
	Analog operating voltage (performance not guaranteed)		2.0		2.5	
V_{BAT}(4)	Operating voltage in the backup area	-	1.8	-	5.5	V
P_D	Power dissipation Temperature: T_A = 85°C (2) or temperature: T_A = 105°C (2)	LQFP144	-	-	571	mW
		LQFP100	-	-	444	
		LQFP64	-	-	339	
		LQFP48	-	-	357	
T_A	Ambient temperature (industrial level)	-	-40	-	85	°C
	Ambient temperature (extended industrial level)	-	-40	-	105	
T_J	Junction temperature(3) (industrial level)	-	-40	-	105	°C
	Junction temperature(3) (extended industrial level)	-	-40	-	125	

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.
4. When there's no backup battery in the application system, the V_{BAT} pin can be either connected to V_{DD} or floating.

4.3.2 Operating conditions at power-up/power-down

The parameters given in table below are derived from tests performed under the general operating conditions.

Table 4-4 Operating conditions at power-up/power-down

Symbol	Condition	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise speed t_r	10	-	500000	us
	V_{DD} fall speed t_f	50	-	∞	
V_{ft}(3)	Retention time below the threshold	-	0	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

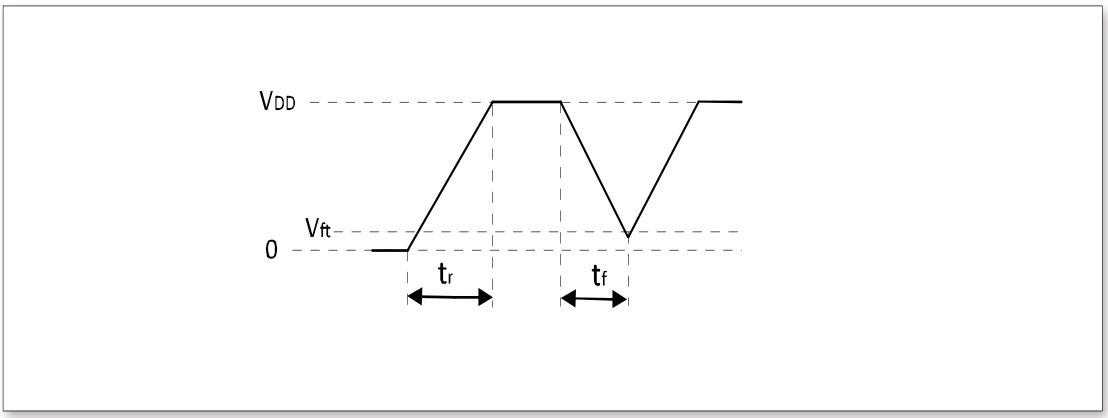

Figure 4-5 Power-up and power-down waveform

4.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions listed in Table 4-3.

Table 4-5 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Embedded reset and power control block characteristics	PLS[3:0]=0000 (rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (falling edge)	-	1.7	-	
		PLS[3:0]=0001 (rising edge)	-	2.1	-	
		PLS[3:0]=0001 (falling edge)	-	2.0	-	
		PLS[3:0]=0010 (rising edge)	-	2.4	-	
		PLS[3:0]=0010 (falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		PLS[3:0]=0100 (falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)	-	3.3	-	
		PLS[3:0]=0101 (falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	
		PLS[3:0]=0111 (falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	
		PLS[3:0]=1000 (falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	
		PLS[3:0]=1001 (falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (falling edge)	-	4.7	-	
$V_{POR/PDR}$	Power on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	30	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	-	3	-	ms

1. Product characteristics are guaranteed by design to be the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: Reset duration is measured from the power-on moment (POR reset) to the moment the first IO is read by the user's application code.

4.3.4 Embedded voltage reference

The parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage listed in Table 4-3.

Table 4-6 Internal reference voltage(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	-40°C < T_A < 105°C	-	1.2	-	V
$T_{s\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	11.8	-	us

1. The shortest sampling time can be determined in the application by multiple iterations.

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin switching rate, program location in memory and executed code.

All run-mode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level—VDD or VSS (no load).
- All peripherals are disabled, unless otherwise specified.
- The access time of the Flash memory is adjusted to the f_{HCLK} frequency (0 wait cycle from 0 to 24MHz, 1 wait cycle from 24 to 48 MHz, 2 wait cycles from 48 to 72MHz, 3 wait cycles from 72 to 96MHz).
- The instruction prefetch function is enabled. When the peripheral is enabled: $f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetch function must be set before clock setting and bus prescaling.

The parameters given in the Table 4-7, Table 4-8, Table 4-9, Table 4-10 are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-7 Typical current consumption in Run mode

Symbol	Parameter	Condition	f_{HCLK} (Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Supply current in Run mode	Internal clock	120M	83.64	84.68	85.71	87.17	42.55	42.59	42.62	43.02	mA
			96M	61.79	61.89	61.94	62.03	32.11	32.25	32.50	32.82	
			48M	32.31	32.39	32.51	32.66	18.96	19.09	19.30	19.56	
			24M	17.40	17.40	17.51	17.68	11.66	11.77	12.00	12.24	
			8M	7.35	7.33	7.41	7.59	5.80	5.79	5.88	6.09	
			4M	2.16	2.14	2.25	2.45	2.88	2.88	2.99	3.19	
			2M	4.71	4.74	4.88	5.11	2.34	2.33	2.43	2.63	
			1M	3.25	3.26	3.39	3.61	2.07	2.05	2.15	2.35	
			500K	2.52	2.52	2.63	2.84	1.93	1.91	2.01	2.21	
			125K	1.88	1.87	1.96	2.17	1.83	1.81	1.90	2.11	

Table 4-8 Typical current consumption in low-power Run mode

Symbol	Parameter	Condition	f_{HCLK} (Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Supply current in low-power Run mode	Internal clock	2M	3.11	3.85	3.91	4.11	2.21	2.88	2.92	3.10	mA
			1M	2.39	3.12	3.16	3.35	1.94	2.61	2.64	2.82	
			500K	2.04	2.75	2.79	2.97	1.81	2.47	1.83	2.35	

Symbol	Parameter	Condition	f_{HCLK} (Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
			125K	1.77	2.47	2.50	2.69	1.71	2.36	2.39	2.58	
			40K	0.24	0.27	0.40	0.62	0.22	0.25	0.38	0.59	
		HSI OFF	40K	0.06	0.09	0.21	0.42	0.05	0.07	0.19	0.40	

1. When HCLK frequency is lower than 8MHz, the system clock is HSI 8M, and AHB clock is drawn by frequency division

Table 4-9 Typical current consumption in Sleep mode

Symbol	Parameter	Condition	f_{HCLK} (Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Supply current in low- power Run mode	Internal clock	120M	63.53	63.69	63.82	64.5	21.99	22.39	22.70	23.3	mA
			96M	46.88	46.96	47.01	47.29	16.68	16.70	16.77	16.99	
			48M	24.77	24.84	24.93	25.17	9.53	9.51	9.58	9.78	
			24M	13.59	13.61	13.69	13.91	5.94	5.91	5.97	6.16	
			8M	6.09	6.06	6.13	6.33	3.53	3.49	3.55	3.74	
			4M	3.50	3.51	3.62	3.84	2.26	2.25	2.35	2.56	
			2M	2.65	2.64	2.74	2.96	2.03	2.01	2.11	2.32	
			1M	2.22	2.21	2.31	2.51	1.91	1.90	1.99	2.20	
			500K	2.00	1.99	2.09	2.29	1.85	1.84	1.93	2.13	
			125K	1.85	1.83	1.92	2.13	1.81	1.79	1.88	2.09	

1. When HCLK frequency is lower than 8MHz, the system clock is HSI 8M, and AHB clock is drawn by frequency division

Table 4-10 Typical current consumption in low-power Sleep mode

Symbol	Parameter	Condition	f_{HCLK} (Hz)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Supply current in low -power Sleep mode	Internal clock	2M	2.53	3.27	3.30	3.49	1.91	2.59	2.62	2.80	mA
			1M	2.10	2.82	2.85	3.04	1.79	2.46	2.49	2.68	
			500K	1.89	2.60	2.63	2.82	1.74	2.39	2.42	2.61	
			125K	1.73	2.43	2.47	2.65	1.69	2.34	2.38	2.56	
			40K	0.23	0.26	0.38	0.60	0.21	0.24	0.37	0.58	
		HSI OFF	40K	0.06	0.08	0.20	0.41	0.05	0.07	0.18	0.39	

Table 4-11 Typical and maximum current consumption in Stop and Standby mode (1)

Symbol	Parameter	Conditions	Typical				Maximum	Unit
			-40°C	25°C	85°C	105°C	25°C	
I_{DDx}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD} =3.3V	36.5	50.7	156.3	371.2	300	μA

Symbol	Parameter	Conditions	Typical				Maximum	Unit
			-40°C	25°C	85°C	105°C	25°C	
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD} =3.3V	1.4	8.7	97.5	264.7	35	
	Supply current in Standby mode	IWDG opens, RTC closes	-	1.44	-	-	-	
		IWDG closes, RTC opens, clock is LSE	-	1.94	-	-	-	
		IWDG closes, RTC closes	0.39	0.65	4.85	13.59	1.2	

1. I/O state is analog input.

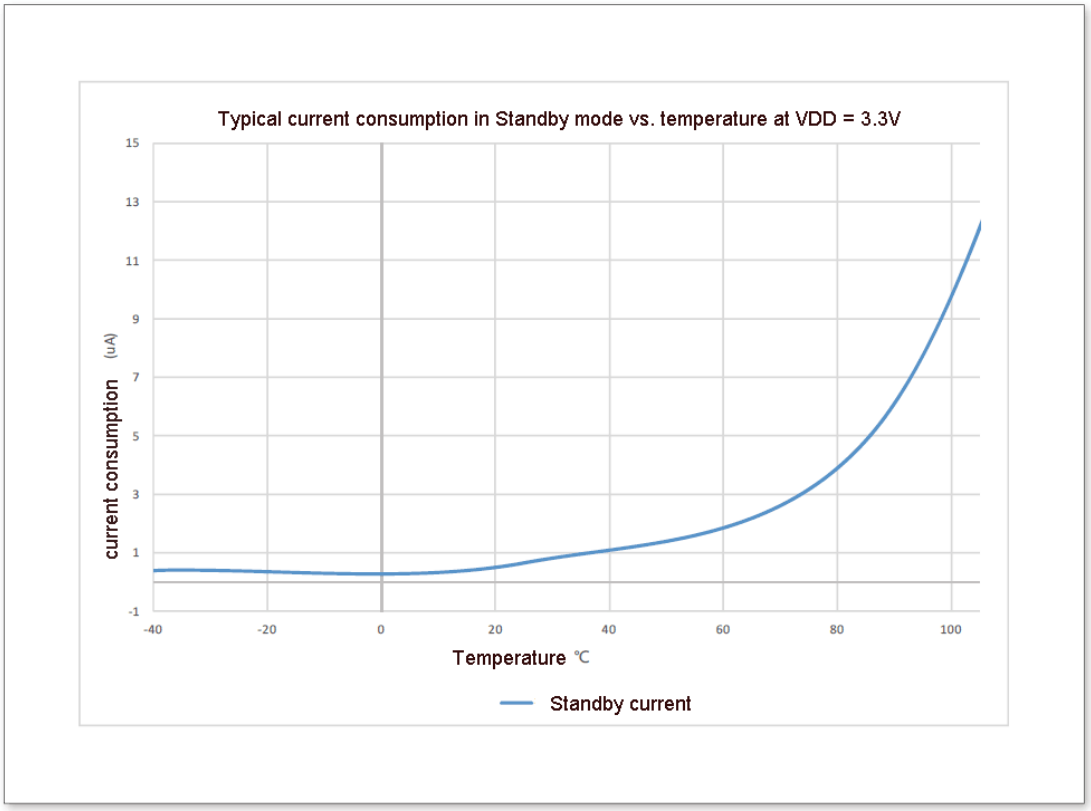

Figure 4-6 Typical current consumption vs. temperature at V_{DD} = 3.3V in Standby mode

Built-in peripheral current consumption

The built-in peripheral current consumption is presented in Table 4-12, The MCU is placed under the following working conditions:

- All I/O pins are in input mode and connected to a static level— V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The given value is calculated by measuring current consumptions
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient temperature and VDD supply voltage conditions are listed in Table 4-3.

Table 4-12 Built-in peripheral current consumption (1)

Symbol	Peripherals	Bus	Typical value	Unit
I_{DD}	FSMC	AHB3	14.9	uA/MHz
	OTG	AHB2	15.2	
	CRC	AHB1	1.7	
	GPIOA		1.5	
	GPIOB		1.5	
	GPIOC		1.3	
	GPIOD		2.1	
	GPIOE		1.6	
	GPIOF		1.4	
	GPIOG		1.6	
	GPIOH		1.1	
	SDIO		20.1	
	CRC		1.7	
	DMA1		6.0	
	DMA2		4.1	
	TIM1	APB2	13.2	
	TIM8		12.9	
	UART1		8.7	
	UART6		8.8	
	ADC1		6.3	
	ADC2		6.1	
	ADC3		6.0	
	SPI1		9.8	
	SYSCFG		0.7	
	COMP		1.3	
	TIM2	APB1	9.9	
	TIM3		7.2	
	TIM4		7.8	
	TIM5		9.8	
	TIM6		2.9	
	TIM7		2.7	
	WWDG		0.4	
	SPI2		10.1	
	SPI3		10.8	
	UART2		9.3	
	UART3		9.2	
	UART4		8.9	

Symbol	Peripherals	Bus	Typical value	Unit
	UART5		9.0	
	I2C1		11.2	
	I2C2		11.0	
	CRS		0.9	
	CAN		12.3	
	BKP		0.7	
	PWR		2.2	
	DAC		1.8	
	UART7		8.8	
	UART8		8.9	

1. f_{HCLK} = 96MHz, f_{APB1} = f_{HCLK} /2, f_{APB2} = f_{HCLK}; the prescale coefficient for each peripheral is the default value.

Wake-up time from low-power mode

The wake-up times listed in the following table are measured during the wake-up phase of the internal clock HSI. The clock source used to wake up the device depends on the current operating mode:

- Stop or Standby mode: the clock source is the oscillator.
- Sleep mode: the clock source is the clock that was set before entering Sleep mode. All times are measured when ambient temperature and supply voltage conform to the general operating conditions.

Table 4-13 Wake-up time from low-power mode

Symbol	Parameter	Condition	Typical	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	HSI is the system clock	14	cycles
t_{WUSTOP}	Wakeup from Stop mode (voltage regulator in operation)	HSI is the system clock	9.4	us
t_{WUSTOP}	Wakeup from Deep Stop mode (voltage regulator in low-power mode)	HSI is the system clock	7.5	us
$t_{WUSTDBY}$	Wakeup from Standby mode	PWR>CR[15:14] = 0x1	302	us
$t_{WUSTDBY}$	Wakeup from Standby mode	PWR>CR[15:14] = 0x2	319	us
$t_{WUSTDBY}$	Wakeup from Standby mode	PWR>CR[15:14] = 0x3	337	us

4.3.6 External clock source characteristics

High-speed external user clock generated from external oscillator source

The characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage conform to the general

operating conditions.

Table 4-14 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{HSE_ext}	User external clock frequency(1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	15	-	-	ns

1. Guaranteed by design, not tested in production.

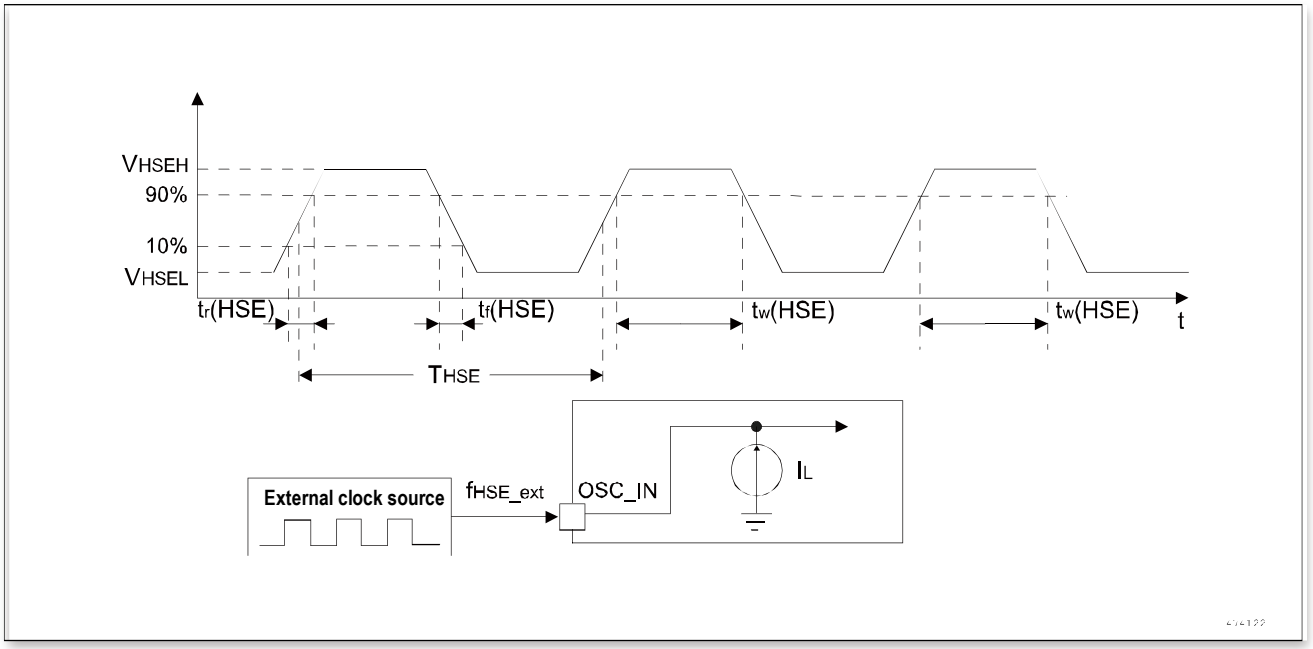

Figure 4-7 AC timing diagram of high-speed external clock source

Low-speed external user clock from external oscillator source

The characteristic parameter given in the following table is measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating condition.

Table 4-15 Low-speed external user clock characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{LSE_ext}	User external clock frequency (1)	-	-	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time (1)	-	250	-	-	ns

1. Guaranteed by design, not tested in production.

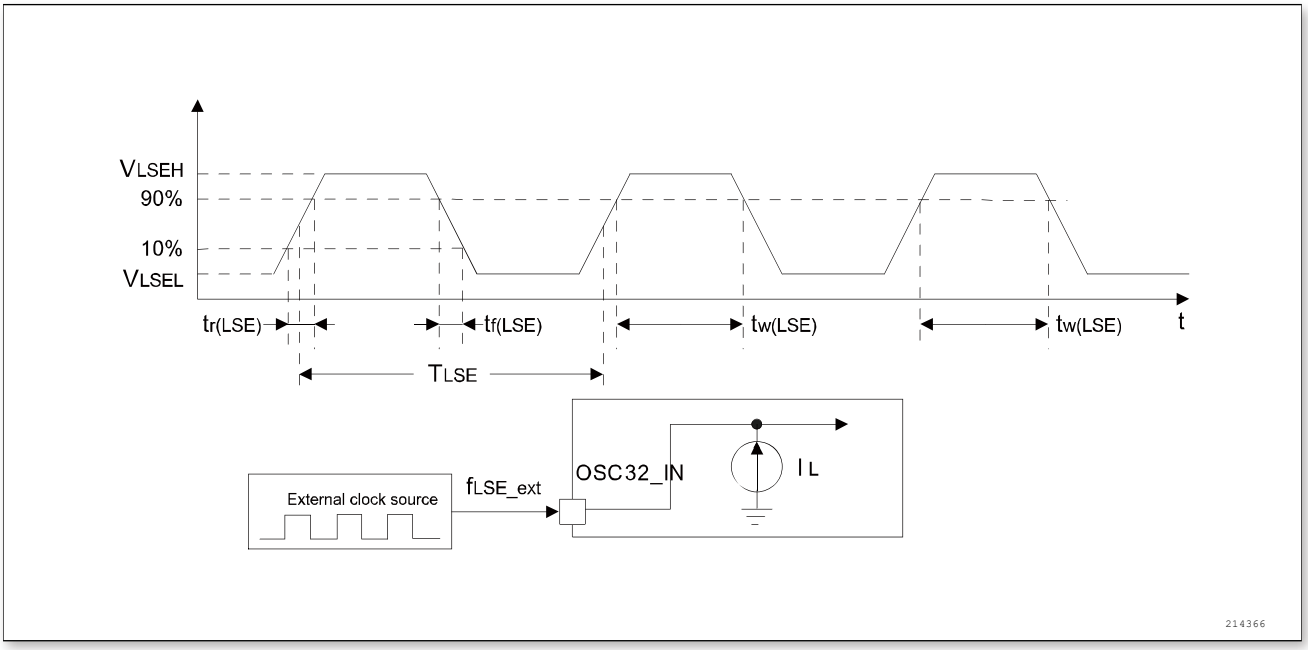

Figure 4-8 AC timing diagram of low-speed external clock source

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external clock (HSE) can be supplied with an 8 ~ 24MHz crystal/ceramic resonator oscillator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external components listed in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.).

Table 4-16 HSE 8 ~ 24MHz oscillator characteristics (1)(2)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{OSC_IN}	Oscillator frequency (2)	2V<V_{DD}<3.6V	2	8	12	MHz
		3.0V<V_{DD}<5.5V	8	16	24	MHz
R_F	Feedback resistor (4)	-	-	1000	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2}(3) is 16pF)	f_{OSC_IN} =24MHz, V_{DD}=3V	-	-	60	Ω
		f_{OSC_IN} =12MHz, V_{DD}=2V	-	-	150	Ω
I_2	HSE driving current	f_{OSC_IN} =24MHz, ESR=30 V_{DD} = 3.3V, C_{L1} C_{L2}(3) is 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Startup	-	9	-	mA/V

Symbol	Parameter	Condition	Min	Typical	Max	Unit
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized	-	3	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Drawn from comprehensive evaluation.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitor in the 5pF ~ 25pF (typical value) range, designed for high-frequency applications. A suitable crystal or resonator should also be carefully selected. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer typically specifies a load capacitance which is the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the combined pin and the PCB board capacitance can be roughly estimated as 10pF).
4. The relatively low value of the R_F resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time, measured from the moment the software enables HSE to a stable 8MHz oscillation is obtained. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

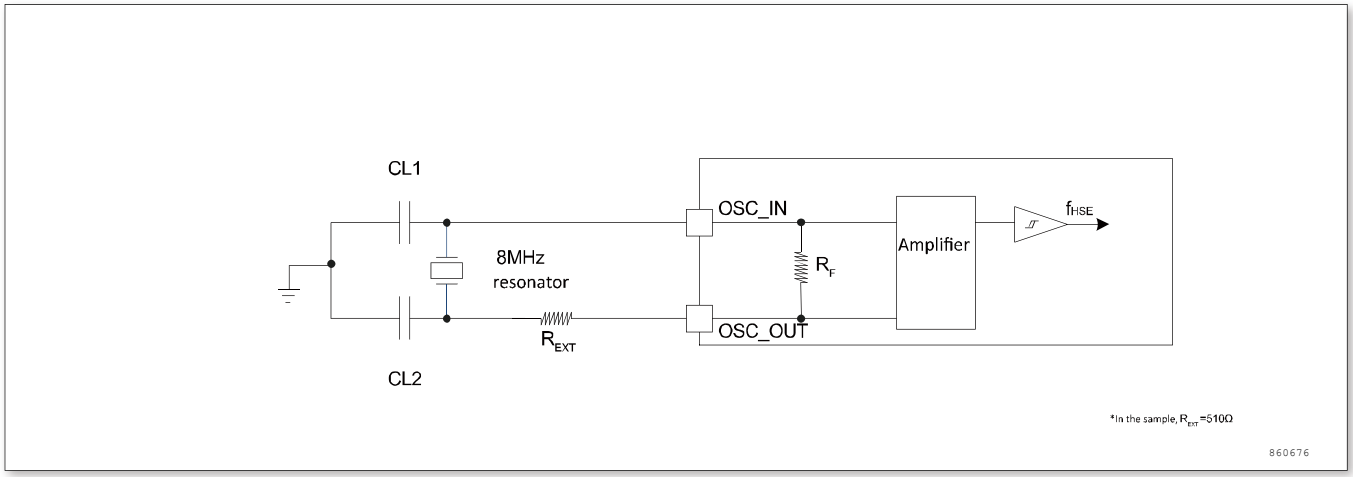

Figure 4-9 Typical application with an 8MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external clock (LSE) may be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external components listed in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.). (Note: The crystal resonator mentioned here refers to quartz crystal resonator by general speaking.)

Note: For C_{L1} and C_{L2}, it is recommended to use 5pF ~ 15pF high-quality ceramic capacitor,

as well as crystal or resonator that meets the requirements. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer typically

specifies a load capacitance which is the serial combination of C_{L1} and C_{L2}. Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2}/(C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and PCB board or PCB-related capacitance. Typically, it is between 2pF and 7pF. Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15pF), it is strongly recommended to use a resonator with a load capacitance $C_L \leqslant$ 7pF. Never use a resonator with a load capacitance of 12.5pF.

Example: if a resonator with a load capacitance of C_L = 6pF, and C_{stray} = 2pF is chosen, then $C_{L1} = C_{L2}$= 8pF.

Table 4-17 LSE oscillator characteristics (f_{LSE}=32.768KHz)(1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	IBSEL=01 DR=00(recommend)	-	290	-	nA
		IBSEL=10 DR=01(Default)	-	425	-	nA
g_m	Oscillator transconductance	IBSEL=01 DR=00	-	3	-	uA/V
		IBSEL=10 DR=01	-	5	-	uA/V
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stabilized	-	1	3	S

1. Drawn from comprehensive evaluation.
2. Refer to the note and caution above this table.
3. A high-quality oscillator (such as MSIV-TIN 32.768Khz) with a smaller RS value can be selected to optimize the current consumption. For details, please consult the crystal manufacturer.
4. $t_{SU(LSE)}$ is the startup time, measured from the moment the software enables LSE to a stable 32.768KHz oscillation is obtained. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

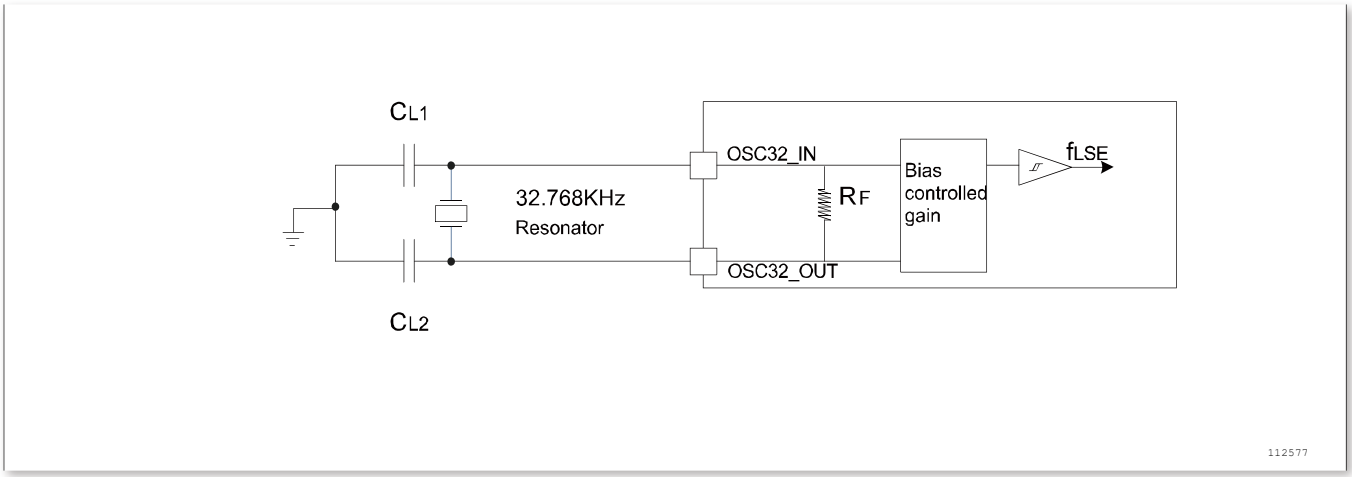

Figure 4-10 Typical application for 32.768KHz crystal

4.3.7 Internal clock source characteristics

The characteristic parameters given in the following table are measured when ambient temperature and power supply voltage conform to the general operating conditions.

High-speed internal (HSI) oscillator

Table 4-18 HSI oscillator characteristics (1)(2)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{HSI}	frequency	-	-	8	-	MHz
ACC_{HSI}	HSI oscillator accuracy	T_A = -40°C ~ 105°C	-2.5	-	+2.5	%
		T_A = 25°C	-1	-	+1	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	-	5	us
$T_{stab(HSI)}$	HSI oscillator stabilization time	-	-	-	10	us
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	-	μA

1. V_{DD} = 3.3V, T_A = -40◦C~85◦C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 4-19 LSI oscillator characteristics (1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{LSI}(2)	frequency	-	-	40	-	KHz
$t_{SU(LSI)}$(3)	LSI oscillator startup time	-	-	-	50	us
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time	-	-	-	100	us
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	0.26	-	μA

1. V_{DD} = 3.3V, T_A = -40◦C~85◦C, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

4.3.8 PLL characteristics

Input clocks f_{PLL_IN} and f_{PLL_OUT} of PLL have the following relationship:

Equation 1:

$$\frac{f_{PLL\_IN}}{\mathrm{PLLDIV}[2:0]+1} = \frac{f_{PLL\_OUT}}{\mathrm{PLLMUL}[6:0]+1}$$

PLLMUL[6:0] and PLLDIV[2:0] are frequency dividing ratios of PLL multiplier divider and output divider.

The characteristic parameter listed in the following table is measured when ambient temperature and power supply voltage meet with the general operating condition.

Table 4-20 PLL characteristics(1)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	4	8	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	20	-	80	%
f_{vco}	PLL output clock frequency range	-	200	-	400	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	12.5	-	200	MHz
t_{LOCK}	PLL lock time	Input clock=8MHz Output clock=100MHz Tolerance=0.1%	-	21.5	60	us
Jitter	RMS cycle-to-cycle jitter	Input clock=8MHz Output clock=100MHz	-	40	-	ps
	RMS period jitter	Input clock=8MHz Output clock=100MHz	-	30	-	
$I_{DD(PLL)}$	PLL current consumption	Input clock=8MHz Output clock=100MHz	-	1.2	-	uA

1. Guaranteed by design, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock frequency compatible with the range defined by f_{PLL_OUT}

4.3.9 Memory characteristics

Table 4-21 Flash memory characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
t_{prog}	16-bit programming time	-	-	30	-	us
t_{ERASE}	Page (1024 bytes) erasing time	-	-	4.5	-	ms
t_{ME}	Mass erasing time	-	-	30	-	ms
I_{DD}	Average current consumption	Read mode 40MHz	-	-	6	mA
	-	Write mode	-	-	7	mA
	-	Erase mode	-	-	2	mA

Table 4-22 Flash memory endurance and data retention period (1)(2)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
N_{END}	Erase/program cycles	-	20000	-	-	Cycles
T_{DR}	Data retention	T_A = 105°C	20	-	-	Years
		T_A = 25°C	100	-	-	

4.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during product comprehensive evaluation.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the

test sample is stressed by one electromagnetic interference until a failure occurs. The failure is indicated by the LEDs.

- EFT: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional failure occurs. This test is compliant with the IEC61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 4-23 EMS characteristics

Symbol	Parameter	Condition	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional failure	V_{DD} = 3.3V, T_A = +25°C, f_{HCLK} = 96MHz, conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF capacitor on V_{DD} and V_{SS} to induce a functional failure	V_{DD} = 3.3V, T_A = +25°C, f_{HCLK} = 96MHz, conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC evaluation and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software. Therefore, it is recommended that the user applies EMC software optimization and qualification tests in relation with the EMC.

Software recommendations

The software flowchart must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or the crystal oscillator pins for 1 second.

To complete these trials, a voltage can be applied directly on the chip, over the range of application requirements. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.3.11 Functional EMS (electrical sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive then a negative pulse separated by 1 second) are applied to all pins of each sample. The sample size depends on the number of supply pins on the chip (3 parts X (n + 1) supply pins). This test conforms to the JEDEC JS-001-2017/002-2018 standard.

Static latchup

Two complementary static latchup tests are required on six samples to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin. These tests are compliant with the EIA/JESD78E IC latchup standard.

Table 4-24 ESD and latch-up characteristics

Symbol	Parameter	Conditions	Class	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (mannequin)	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	C3	±1500	V
I_{LU}	Electrostatic latchup (Latchup current)	T_A = 25°C, conforming to JESD78E	I, A	±100	mA

4.3.12 GPIO port general input/output characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests performed under the conditions summarized in Table 4-3. All I/O ports are CMOS-compliant.

Table 4-25 I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	3.3V CMOS port	-	-	1.47	V
V_{IL}	Input low level voltage	5V CMOS port	-	-	2.26	V
V_{IH}	Input high level voltage	3.3V CMOS port	1.74	-	-	V
V_{IH}	Input high level voltage	5V CMOS port	2.61	-	-	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	3.3V	0.52	0.59	0.66	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	5V	0.72	0.78	0.83	V
I_{lkg}	Input leakage current (2)	3.3V	-	0.0001	-	μA
I_{lkg}	Input leakage current (2)	5V	-	0.0001	-	μA
R_{PU}	Weak pull-up equivalent resistance (3)	3.3V $V_{IN} = V_{SS}$	-	50	-	kΩ
R_{PU}	Weak pull-up equivalent resistance (3)	5V $V_{IN} = V_{SS}$	-	50	-	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V $V_{IN} = V_{DD}$	-	50	-	kΩ

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PD}	Weak pull-down equivalent resistance (3)	5V V_{IN} = V_{SS}	-	50	-	kΩ
C_{IO}	I/O pin capacitor	-	-	-	1	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. In case of a negative current back flow in the adjacent pin, the leakage current may be higher than the maximum value.
3. Pull-up and pull-down resistance is poly resistance.
4. The above input level value corresponds to CS =0 condition.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA current.

In user application, the number of I/O pin must ensure that the drive current must be limited to respect the absolute maximum rating specified in Section 4.2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum running current of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents absorbed and sunk by all the I/O pins on V_{SS}, plus the maximum running current of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 4-3. All I/O ports are CMOS-compliant.

Table 4-26 Output voltage characteristics

SPEED	Symbol	Parameter	Conditions	Typ.	Unit
11 (50MHz)	V_{OL} (1)	Output low level	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.17	V
	V_{OH} (2)	Output high level		3.12	
	V_{OL} (1)(3)	Output low level	$\|I_{IO}\|$=20mA, VDD=3.3V	0.51	
	V_{OH} (2)(3)	Output high level		2.83	
	V_{OL} (2)(3)	Output low level	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.13	
	V_{OH} (2)(3)	Output high level		3.17	
10 (2MHz)	V_{OL} (1)	Output low level	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.18	
	V_{OH} (2)	Output high level		3.12	
	V_{OL} (1)(3)	Output low level	$\|I_{IO}\|$=20mA, VDD=3.3V	0.52	
	V_{OH} (2)(3)	Output high level		2.83	
	V_{OL} (2)(3)	Output low level	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.13	
	V_{OH} (2)(3)	Output high level		3.17	
01 (10MHz)	V_{OL} (1)	Output low level	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.18	
	V_{OH} (2)	Output high level		3.12	

SPEED	Symbol	Parameter	Conditions	Typ.	Unit
	V_{OL} (1)(3)	Output low level	$\|I_{IO}\|$= 20mA, VDD=3.3V	0.52	
	V_{OH} (2)(3)	Output high level		2.83	
	V_{OL} (2)(3)	Output low level	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.13	
	V_{OH} (2)(3)	Output high level		3.17	

1. The I_{IO} current sourced by the chip must always respect the absolute maximum rating specified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} sunk by the chip must always respect the absolute maximum rating speified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VDD}.
3. Drawn from comprehensive evaluation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 4-11 and Table 4-27, respectively.

Unless otherwise specified, the parameter listed in Table 4-27 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 4-3.

Table 4-27 Input/output AC characteristics (1)(3)

SPEED[1:0] configuration	Symbol	Parameter	Conditions	Typ.	Unit
11	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF VDD=3.3V	3.49	ns
	$t_{r(IO)out}$	Output low to high level rise time		3.59	ns
10	$t_{f(IO)out}$	Output high to low level fall time		6.35	ns
	$t_{r(IO)out}$	Output low to high level rise time		6.95	ns
01	$t_{f(IO)out}$	Output high to low level fall time		4.25	ns
	$t_{r(IO)out}$	Output low to high level rise time		3.87	ns

1. The I/O port speed is configured through MODEx[1:0]. Refer to the Reference manual for a description of the GPIO port configuration register.
2. The maximum frequency is defined in Figure 4-11
3. Guaranteed by design, not tested in production.

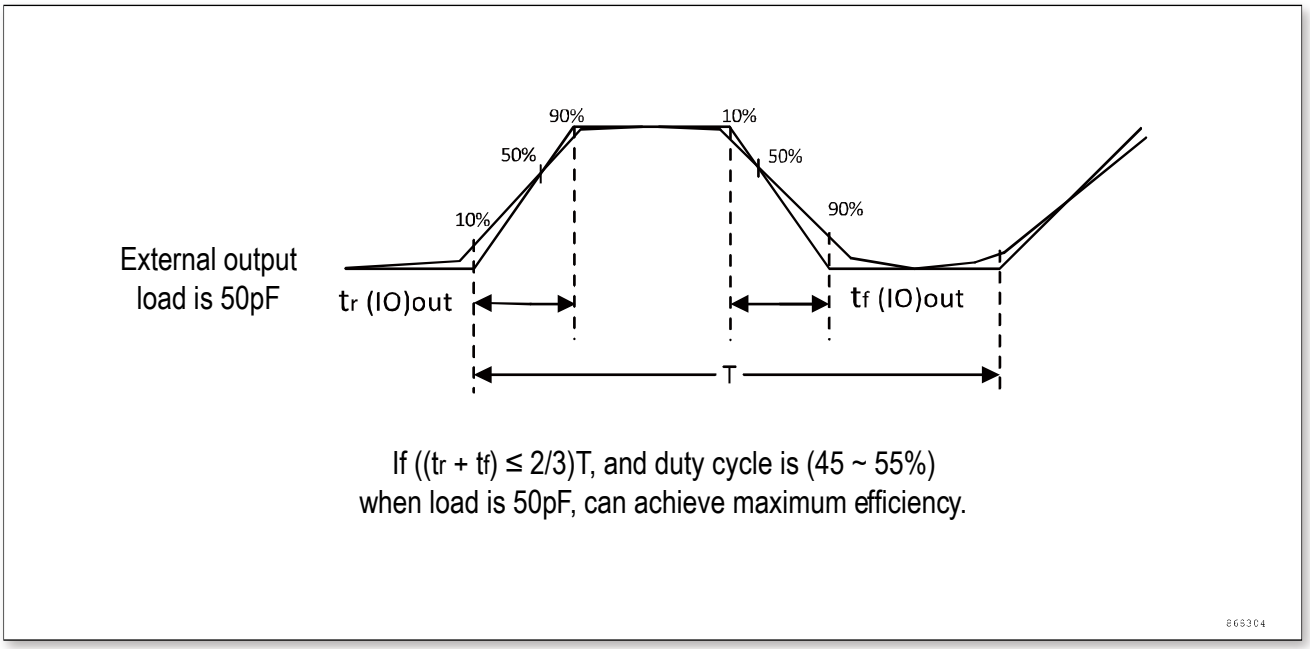

Figure 4-11 Input/output AC characteristics definition

4.3.13 NRST pin characteristics

The NRST pin input driver uses the CMOS technology, and it is connected to a permanent pull-up resistor, RPU. Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-28 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage	VDD=3.3V	-	-	1.47	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage	VDD=3.3V	1.74	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	VDD=3.3V	0.52	0.59	0.66	V
R_{PU}	Weak pull-up equivalent resistor (1)	$V_{IN} = V_{SS}$	25	50	85	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	-	-	-	1.0	us
$V_{NF(NRST)}$ (1)	NRST input unfiltered pulse	-	4.0	-	-	us

1. Guaranteed by design, not tested in production.

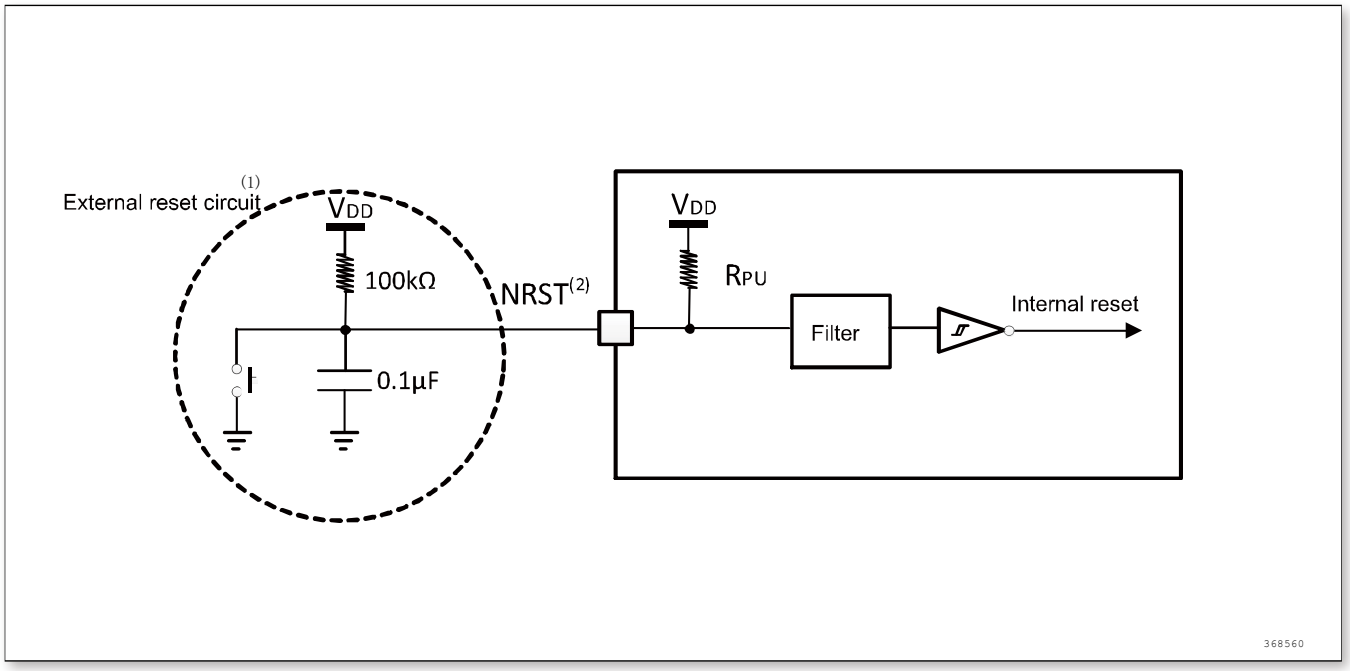

Figure 4-12 Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 4-28, otherwise the MCU cannot be reset.

4.3.14 Timers characteristics

The parameters given in the table below are guaranteed by design.

Refer to Section 0 for details on the input/output alternate function pin (output compare, input capture, external clock, PWM input).

Table 4-29 TIMx(1) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	10.4	-	ns
f_{EXT}	CH1 to CH4 timer external clock frequency	-	0	-	MHz
		$f_{TIMxCLK}$ = 96MHz	0	48	
Res_{TIM}	Timer resolution	-	-	16	Bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	0.0104	682.6	us
t_{MAX_COUNT}	Maximum possible count (TIM_PSC adjustable)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96MHz	-	44.7	s
t_{MAX_IN}	TIM maximum input frequency	-	-	96MHz	MHz

4.3.15 Communication interface

I2C interface characteristics

Unless otherwise specified, the parameters given in the table below are derived from the tests performed under the ambient temperature, f_{PCLK1} frequency and VDD supply voltage conditions summarized in Table 4-3.

The I2C interface complies with the standard I2C communication protocol but has the following limitations: the SDA and SCL are not "true" open-drain pins. When configured as open-drain, the PMOS tube connected between the pin and VDD is disabled, but is still present.

I2C interface characteristics are listed in the table below. Refer to section 0 for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 4-30 I2C interface characteristics

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	us
$t_{w(SCLH)}$	SCL clock high time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	us
$t_{su(SDA)}$	SDA establishment time	$2*t_{PCLK}$	-	$2*t_{PCLK}$	-	ns
$t_{h(SDA)}$	SDA data retention time	0(3)	-(4)	0(3)	-(4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	$6*t_{PCLK}$ - 1(4)	-	$6*t_{PCLK}$ - 0.3(4)	μs
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	$6*t_{PCLK}$ - 1(4)	-	$6*t_{PCLK}$ - 0.3(4)	μs
$t_{h(STA)}$	Start condition hold time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	us
$t_{su(STA)}$	Repeated start condition establishment time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	us
$t_{su(STO)}$	Stop condition establishment time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	us
$t_{w(STO:STA)}$	Time from stop condition to start condition (Bus Free)	$5*t_{PCLK}$	-	$5*t_{PCLK}$	-	us
C_b	Capacitive load of each bus	4.7	-	1.2	-	pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of I2C standard mode, f_{PCLK1} must be greater than 3MHz. To reach the maximum frequency of I2C fast mode, f_{PCLK1} must be greater than 12MHz.
3. Ensure SCL drops below $0.3V_{DD}$ on falling edge before SDA crosses into the indeterminate range of $0.3V_{DD}$ to $0.7V_{DD}$.

   NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to $0.3V_{DD}$ should be used to insert a delay of the SDA transition with respect to SCL.
4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.

5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
6. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

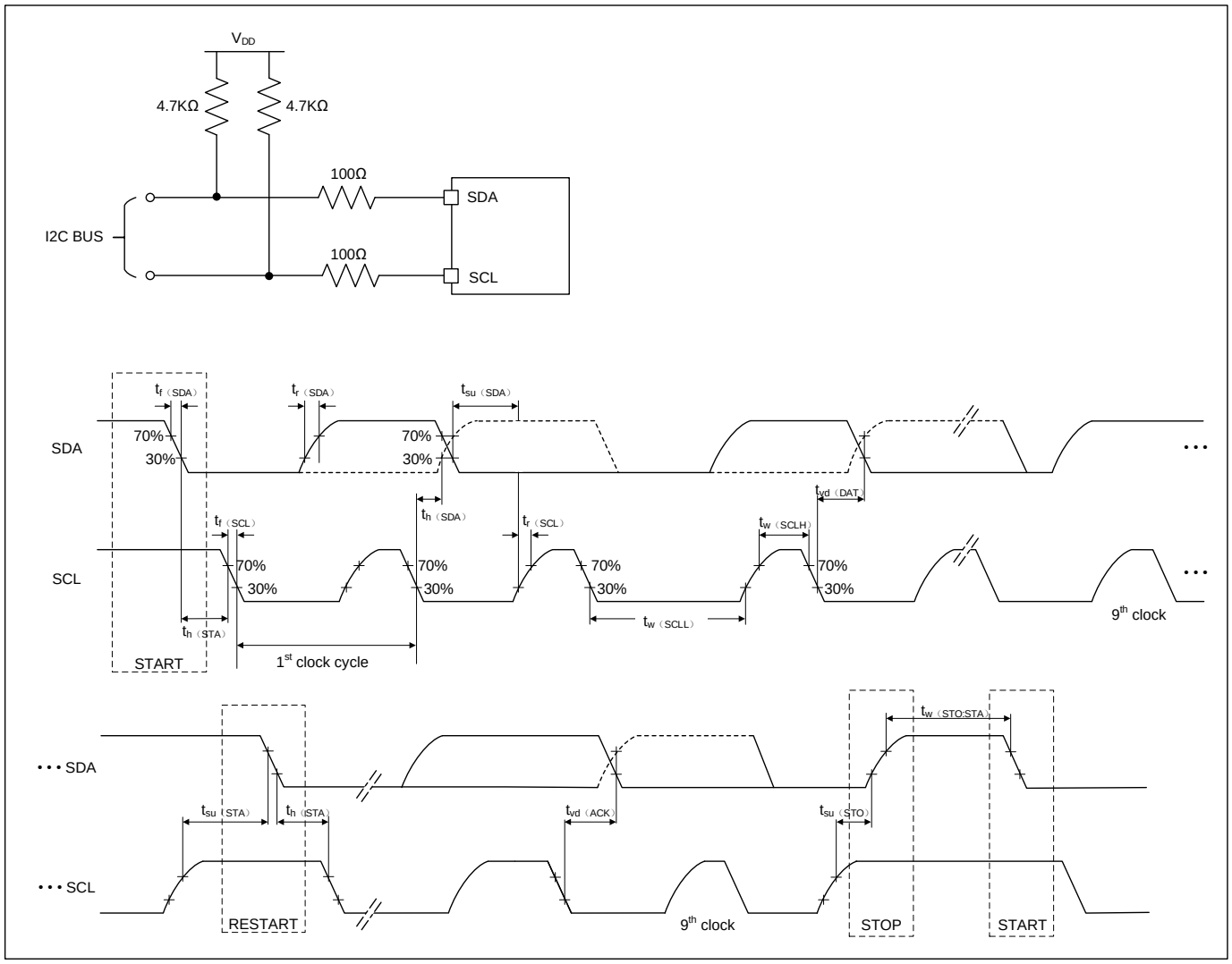

Figure 4-13 I2C bus AC waveform and measurement circuit (1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$

SPI interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 0 for more details on the input/output alternate function pins (NSS, SCK, MOSI, MISO)

Table 4-31 SPI characteristics (1)

Symbol	Parameter	Conditions	Min.	Max.	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	24	MHz

Symbol	Parameter	Conditions	Min.	Max.	Unit
		Auxiliary mode	-	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance:C = 15pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS establishment time	Auxiliary mode	$1t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Auxiliary mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ (1)	SCK high level time	-	$t_{c(SCK)/2}$- 6	-	ns
$t_{w(SCKL)}$ (1)	SCK low level time	-	$t_{c(SCK)/2}$- 6	-	ns
$t_{su(MI)}$ (1)	Data input establishment time	Master mode, f_{PCLK} = 48MHz, prescaler coefficient= 2, high-speed mode	12	-	ns
$t_{su(SI)}$ (1)		Auxiliary mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler coefficient= 2, high-speed mode	0	-	ns
$t_{h(SI)}$ (1)		Auxiliary mode	6	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enabling edge)	-	34	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enabling edge)	-	13	ns
$t_{h(MO)}$ (1)	SPI clock frequency	Master mode (after enabling edge)	-0.6	2	ns

1. Drawn from comprehensive evaluation.
2. The minimum value indicates the minimum time for driving output, and the maximum value indicates the maximum time to obtain data correctly.
3. The minimum value represents the minimum time for closing output, and the maximum value represents the maximum time to put the data line in the high impedance state.

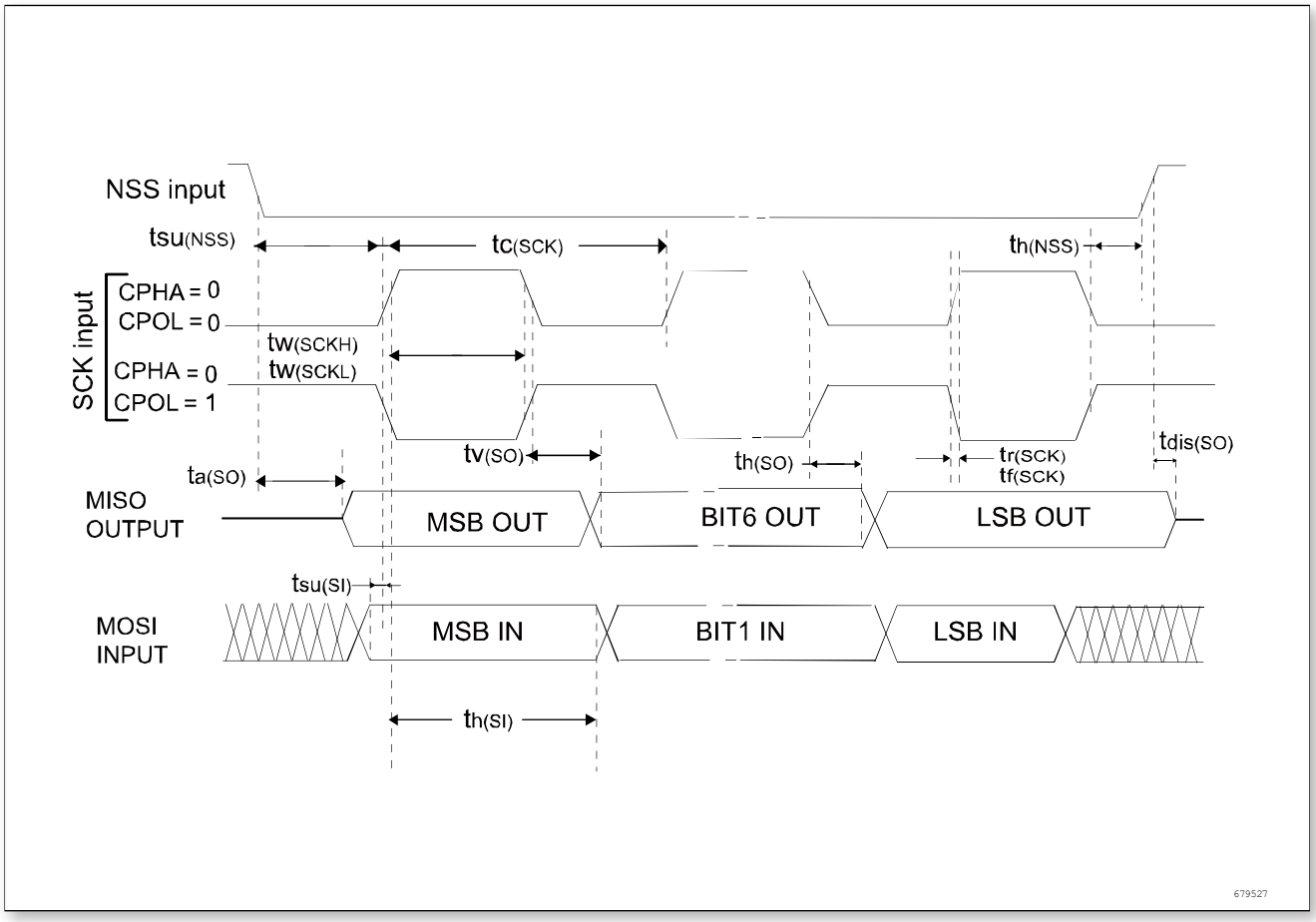

Figure 4-14 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

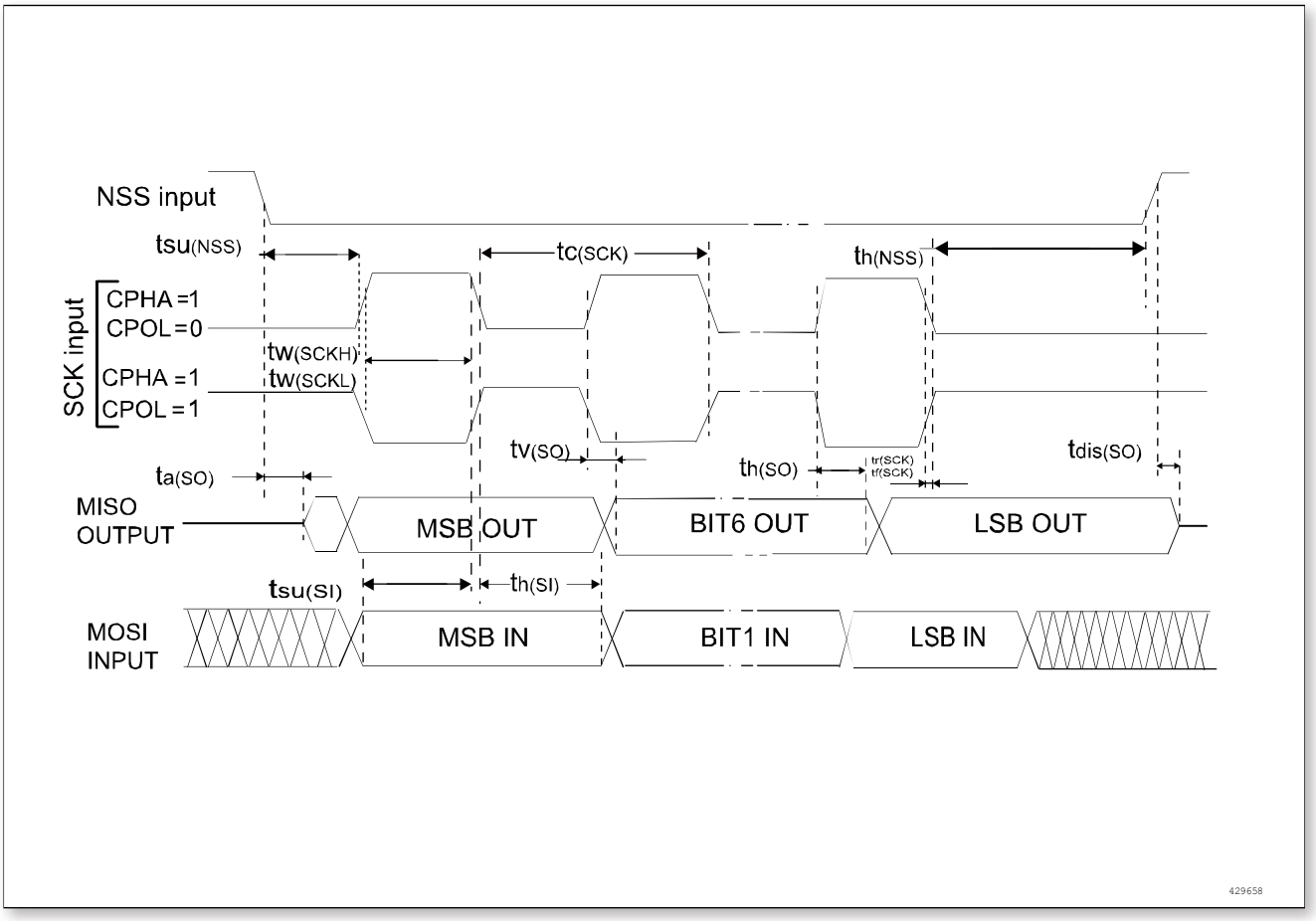

Figure 4-15 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

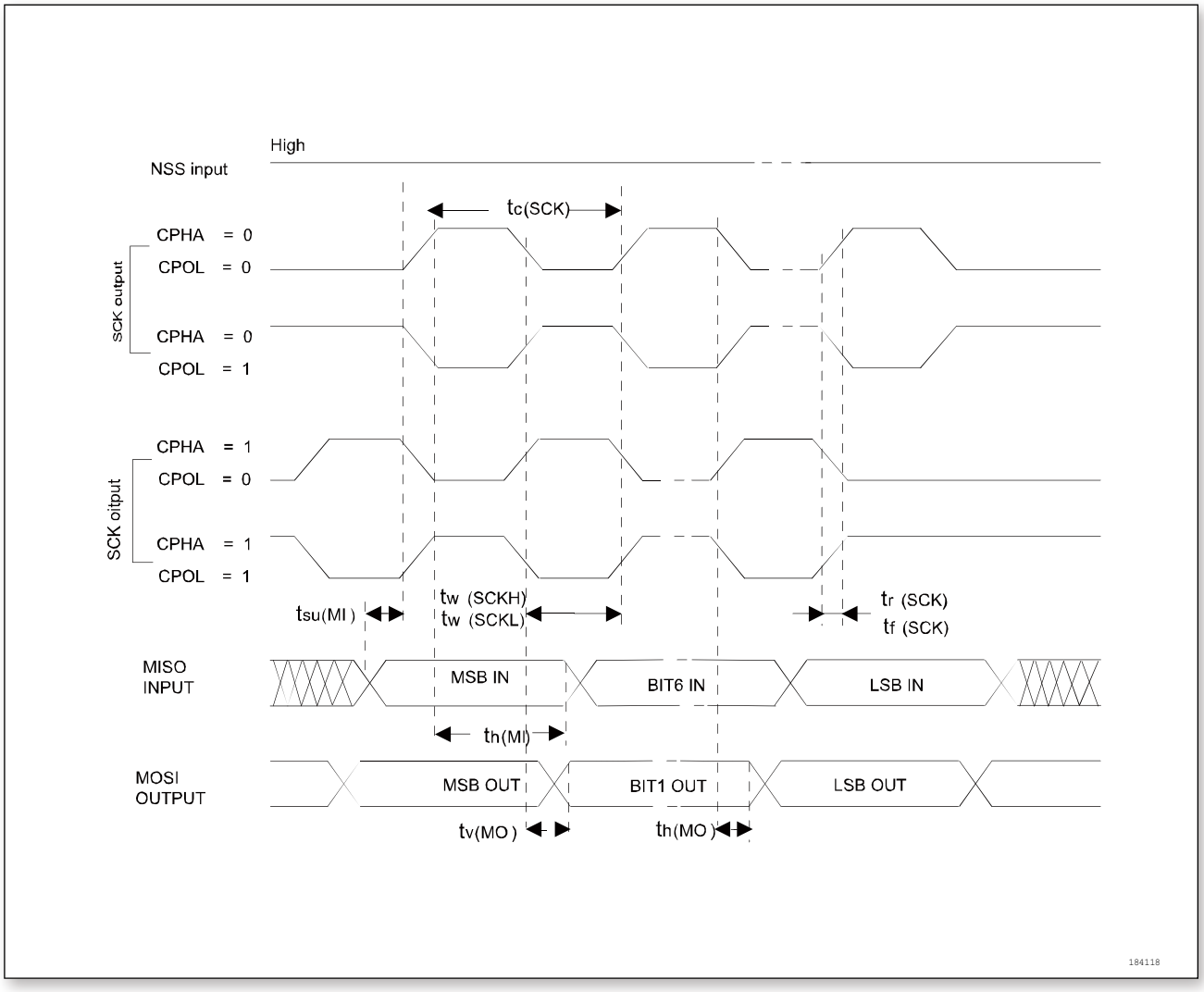

Figure 4-16 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.16 CAN Characteristics

Refer to Section 0 for the details on characteristics of input/output alternate function pin (CAN_TX and CAN_RX).

4.3.17 USB Characteristics

Table 4-32 USB electrical parameter

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DD}	USB operating voltage	-	2.8	3.6	V
V_{DI}	Differential input range	-	0.2	-	V
V_{CM}	Differential common mode range	-	0.8	2.5	V

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{SE}	Single-end reception threshold	-	1.3	2	V
V_{OL}	Electrostatic output low voltage	Load resistance 1.5kΩ connected to 3.6V	-	0.3	V
V_{OH}	Electrostatic output high voltage	Load resistance 15kΩ connected to V_{SS}	2.8	3.6	V
R_{PD}	PA11/PA12 pull-down resistance	-	13.5	16.5	kΩ
R_{PU}	PA11/PA12 pull-up resistance	-	1.25	1.75	kΩ

1. Guaranteed by design, not tested in production.

Table 4-33 USB dynamic characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_r	Rising edge	C_L = 50pF	7.688	20.75	ns
t_f	Falling edge	C_L = 50pF	7.42	20.59	ns
V_{CRS}	Output signal crossover voltage	-	1.36	2.0	V

1. Guaranteed by design, not tested in production.

4.3.18 ADC characteristics

Unless otherwise specified, the parameters in the following table are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage specified in Table 4-3.

Table 4-34 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S(1)	Sampling rate	-	-	-	1	MHz
f_{TRIG}(1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	See equation 2			kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	-	10	pF
t_{STAB}(1)	Power-on time	-	-	-	10	us
t_{lat}(1)	Injection trigger conversion time delay	-	-	-	-	$1/f_{ADC}$
t_{latr}(1)	Conventional trigger conversion time delay	-	-	-	-	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	us

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
			2.5	-	240.5	$1/f_{ADC}$
t_{CONV}(1)	Total conversion time (Including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	us
		-	15 ~ 253 (Sampling t_S + SAR conversion 12.5)			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product series, V_{REF+} is connected to V_{DDA}, V_{REF-} connected to V_{SSA} internally.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of 1/ f_{ADC} must be added to the delay.

Input impedance list

Equation 2

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula (equation 2) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB, where N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 4-35 Maximum R_{AIN} under f_{ADC}=15MHz

T_S(cycle)	t_S(us)	Maximum R_{AIN}(kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

Table 4-36 ADC static parameter (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Composite error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	8	LSB
EO	Offset error		-5/+3	
EG	Gain error		+4	
ED	Differential linearity error		-1/+4	
EL	Integral linearity error		-4/ +2	

1. Correlation between ADC accuracy and negative injection current: Injecting negative current on

any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input pin. It is recommended to add a Schottky diode (pin to ground) to standard analog pins that may potentially inject negative current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Section 4.2, the ADC accuracy will not be affected.

2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: the maximum deviation between the actual and ideal transfer curves.

EO = Offset error: the deviation between the first actual transition and the first ideal one.

EG = Gain error: the deviation between the last ideal transition and the last actual one.

ED = Differential linearity error: the maximum deviation between the actual steps and the ideal ones.

EL = Integral linearity error: the maximum deviation between any actual transition and the endpoint correlation line.

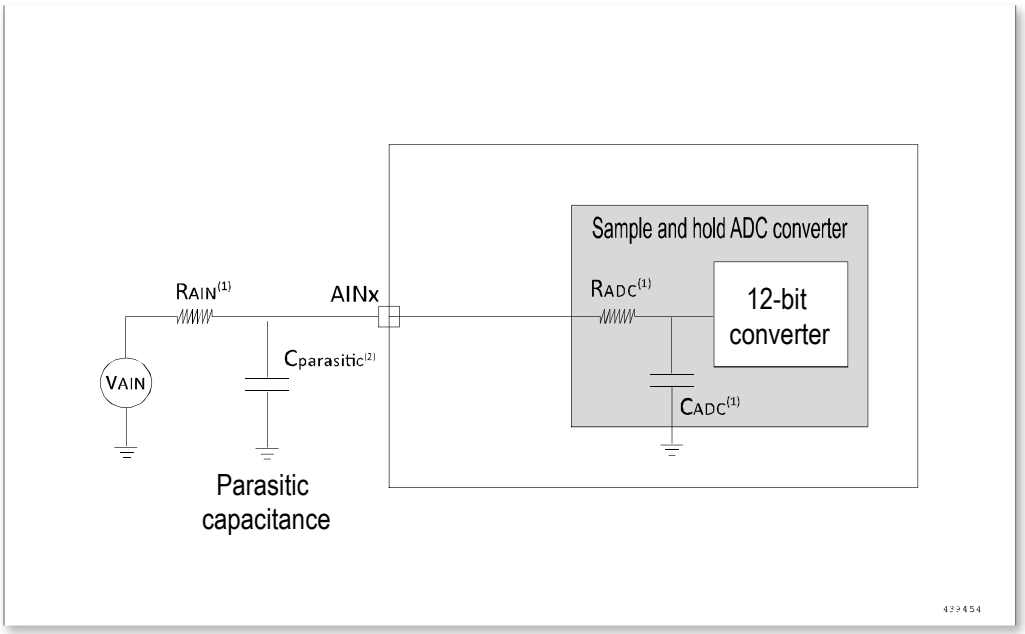

Figure 4-17 Typical connection diagram using ADC

1. Refer to Table 4-34 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the parasitic capacitance (about 7pF) on the PCB (dependent on soldering and PCB layout quality) and the pad. A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design guidelines

Power supply decoupling should be performed as shown in the diagram below. The 10 nF capacitor should be ceramic and it should be placed as close as possible to the MCU chip.

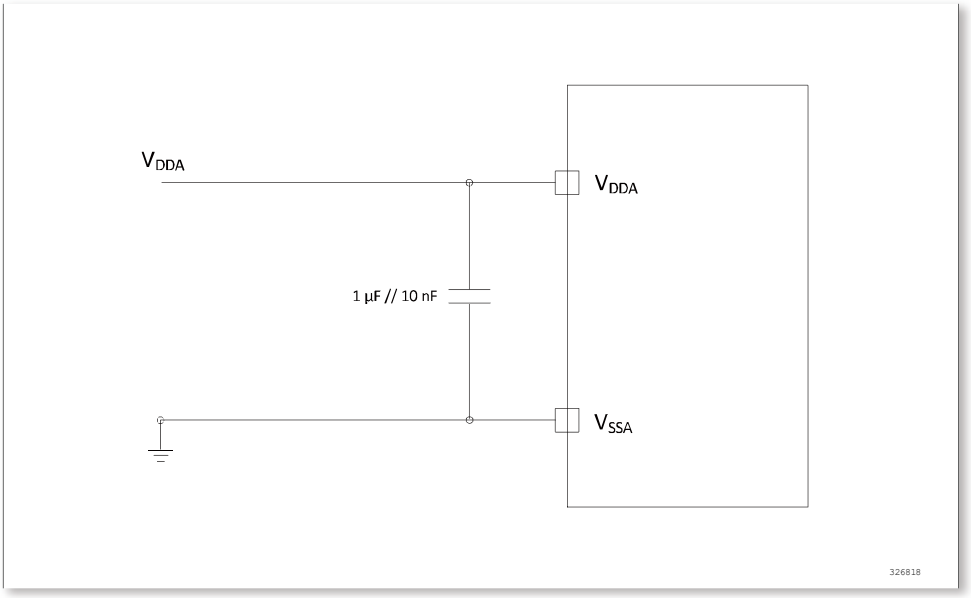

Figure 4-18 Decoupling circuit of power supply and reference power supply

4.3.19 Temperature sensor characteristics

Table 4-37 Temperature sensor characteristics (3)(4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L (1)	V_{SENSE} linearity with temperature	-10	-	+10	°C
Avg_Slope (1)	Average slope	-	4.955	-	mV/°C
V_{25} (1)	Voltage at 25°C	-	1.465	-	V
t_{START} (2)	Establishment time	-	-	10	µS
t_{S_temp} (2)	ADC sampling time when reading the temperature	-	-	-	µS

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by application through multiple circulations.
4. V_{DD} = 3.3V.
5. Temperature formula: TS_adc = 25 + (value * vdda – offset * 3300) / (4096 * Avg_slope), offset recorded in 0x1FFFF7F6 low 12-bit.

4.3.20 Built-in reference voltage characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conforming to the general operating conditions.

Table 4-38 Built-in reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in reference voltage	-40◦C < T_A < 105◦C	-	1.2	-	V
$T_{s\_vrefint}$(1)	ADC sampling time when reading internal reference voltage	-	-	11.8	-	us

1. The shortest sampling time may be determined by application through multiple circulations.

4.3.21 DAC characteristics

Table 4-39 DAC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
V_{REF+}	Reference voltage	-	2.5	3.3	5.5	V
R_O	Output impedance	buff on, output connected to V_{SSA}	-	97	-	Ω
		buff on, output connected to V_{DDA}	-	85	-	
DAC_OUT_{min}	Lowest output voltage	-	V_{SSA}+0.1	-	-	V
DAC_OUT_{max}	Highest output voltage	-	-	-	V_{DDA}-0.1	V
I_{DDA}	DAC static current	-	-	430	-	uA
DNL	Differential nonlinear error	-	-	-4/+1	-	LSB
INL	Integer nonlinear error	-	-	-2.5/+3	-	LSB
Offset	Offset error	-	-	-1/+1	-	LSB
Gain error	Gain error	-	-	-2/+2	-	LSB
Update rate	Maximum update rate	-	-	1	-	MS/s

1. Guaranteed by comprehensive evaluation, not tested during production

4.3.22 Comparator characteristics

Table 4-40 Comparator characteristics

Symbol	Parameter	Register configuration	Min.	Typ.	Max.	Unit
t_{HYST}	Hysteresis	00	-	0	-	mV
		01	-	15	-	mV
		10	-	30	-	mV
		11	-	90	-	mV
V_{OFFSET}	Offset voltage	00	0.091	0.213	0.358	mV
t_{DELAY}		00	-	80	-	ns

Symbol	Parameter	Register configuration	Min.	Typ.	Max.	Unit
	Propagation delay (1)	01	-	51	-	ns
		10	-	26	-	ns
		11	-	9	-	ns
I_q	Average operating current (2)	00	-	4.5	-	uA
		01	-	4.4	-	uA
		10	-	4.4	-	uA
		11	-	4.4	-	uA

1. Time difference between output flip 50% and input flip.
2. Mean value of the total consumption current, running current.

5 Package dimensions

5.1 Package LQFP144

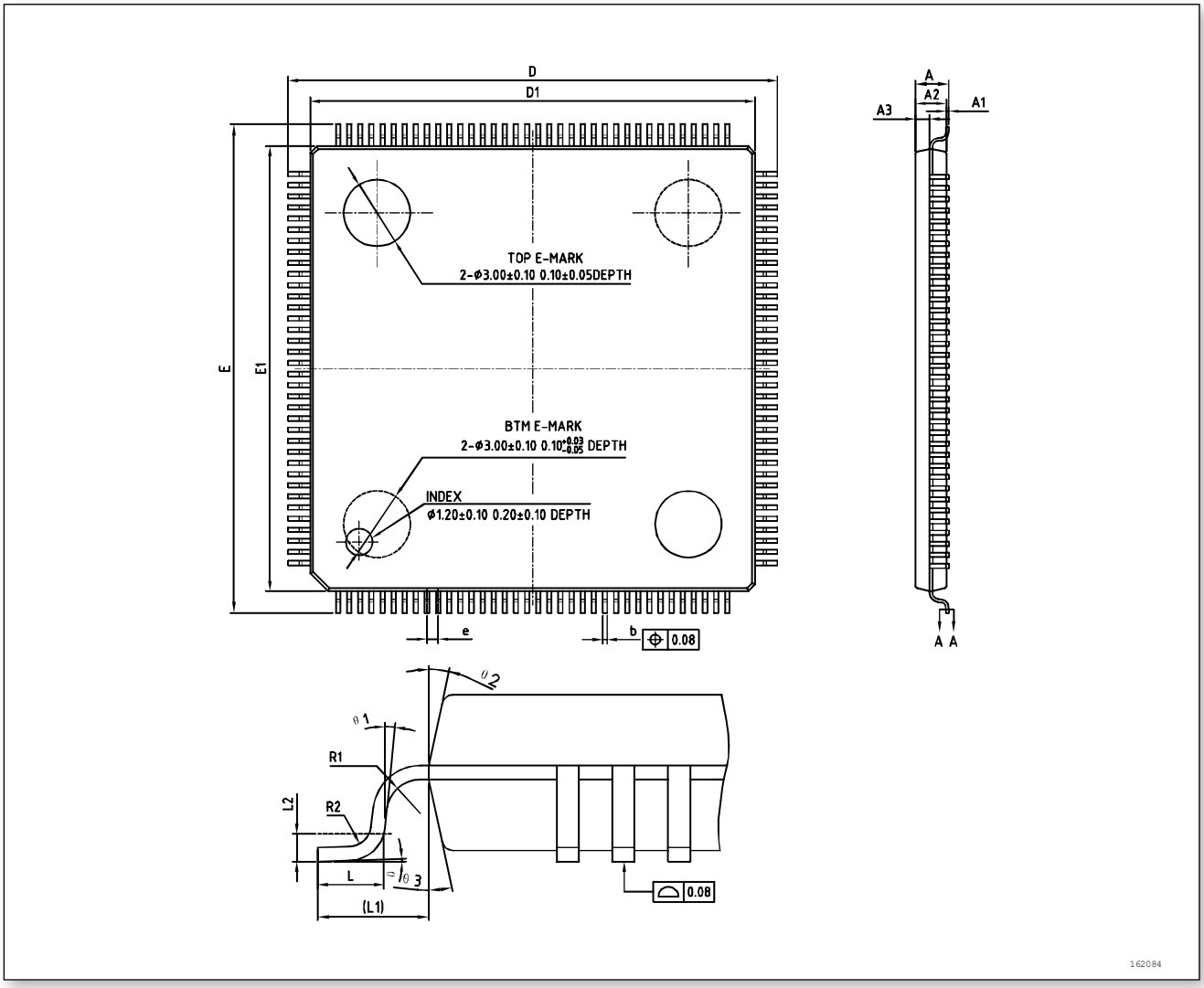

Figure 5-1 LQFP144, 144-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-1 LQFP144 dimensions

Symbol	Millimeter		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.127	-	0.18
c1	0.119	0.127	0.135
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	-
θ	0°	-	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ2	11°	12°	13°

5.2 Package LQFP100

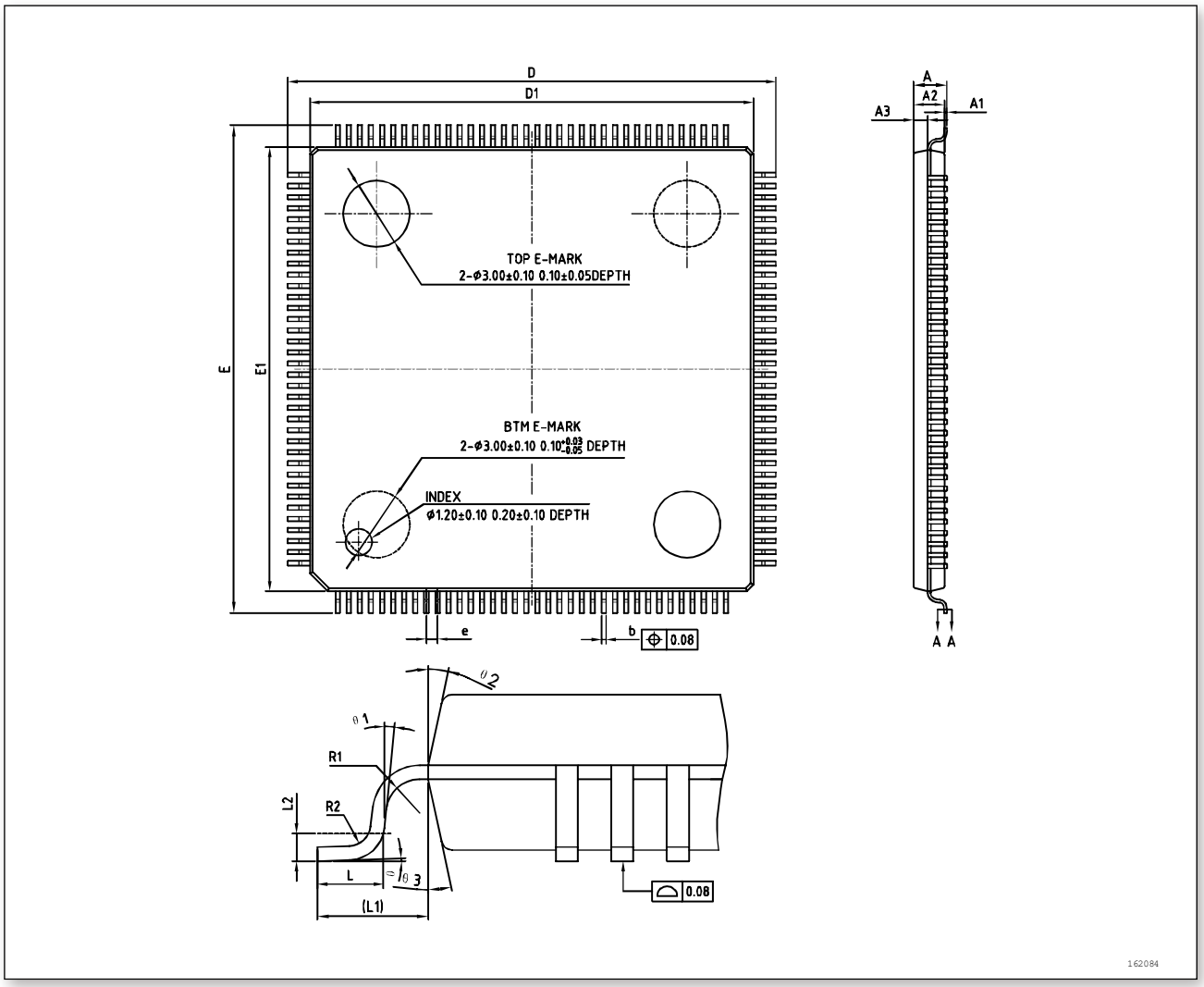

Figure 5-2 LQFP100, 100-pin low-profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-2 LQFP100 dimensions

Symbol	Millimeter		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°

5.3 Package LQFP64

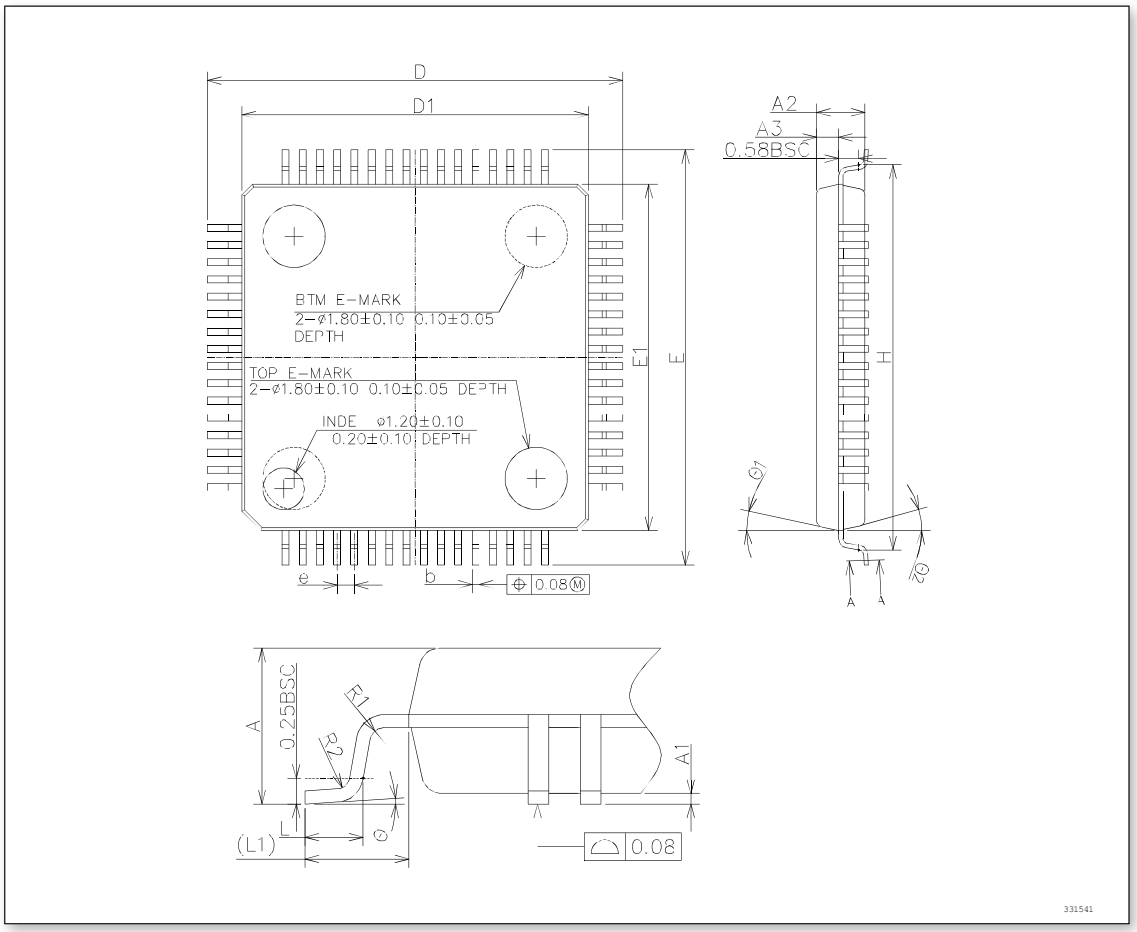

Figure 5-3 LQFP64, 64-pin low-profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-3 LQFP64 dimensions

Symbol	Millimeter		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	-	0.50	-
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

5.4 Package LQFP48

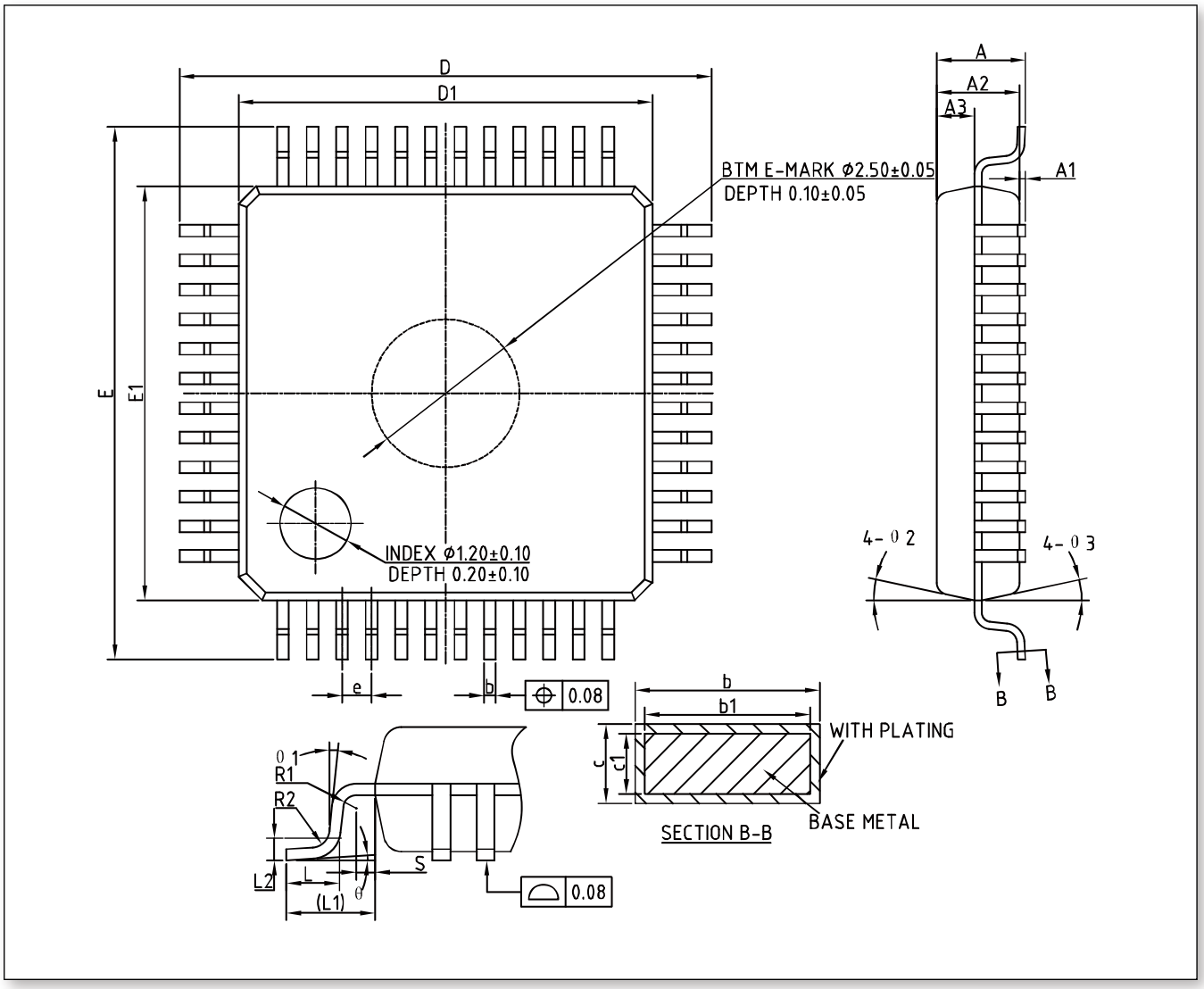

Figure 5-4 LQFP48, 48-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-4 LQFP48 dimensions

Symbol	Millimeters		
	Minimum	Typical	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

5.5 Package QFN40

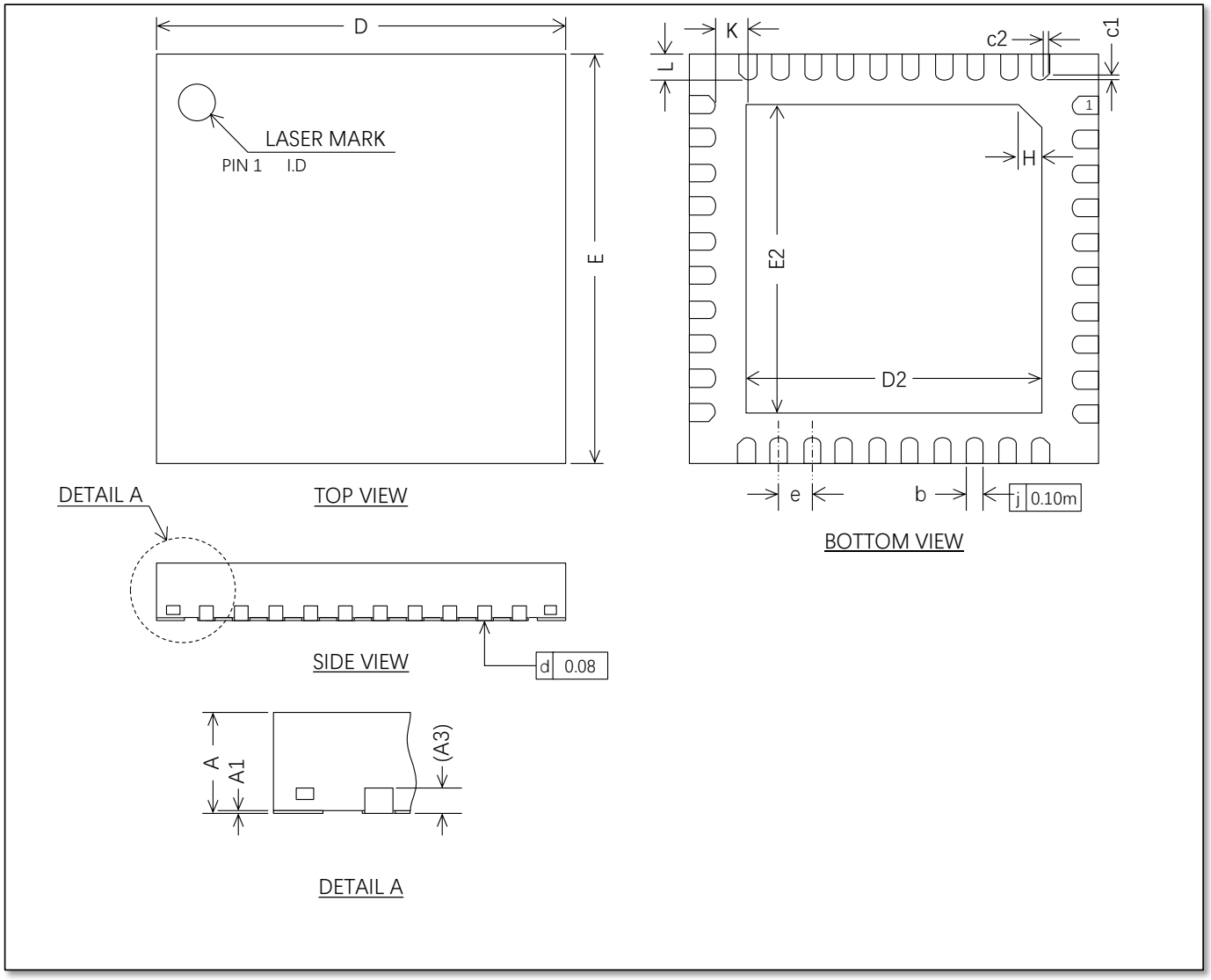

Figure 5-5 QFN40, 40-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 5-5 QFN40 dimensions

Symbol	Millimeter		
	Minimum	Typical	Maximum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.20	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
e	-	0.50	-
H	0.35REF		
K	0.25	0.35	0.45
L	0.30	0.40	0.50
c1	-	0.08	-
c2	-	0.08	-

6 Part identification

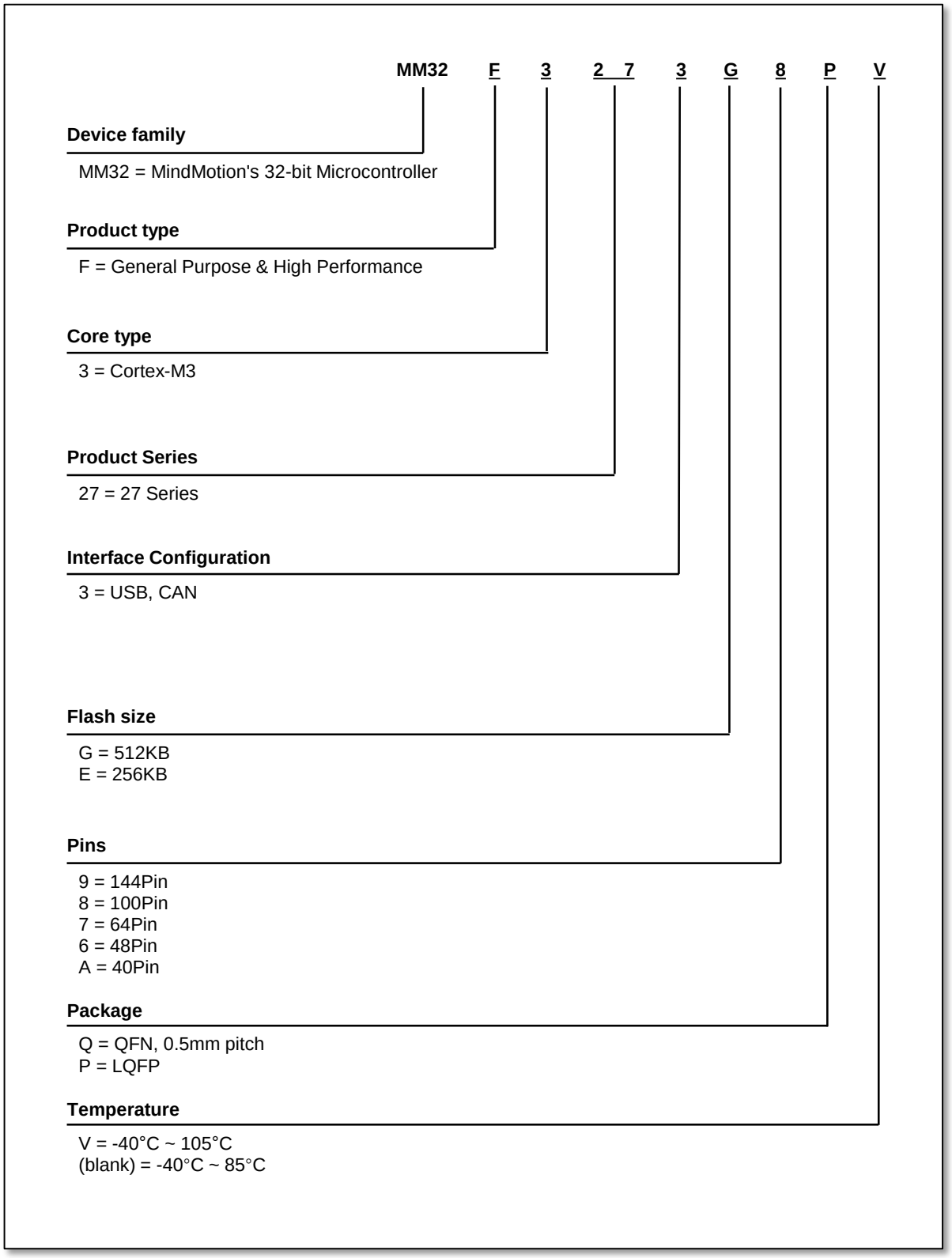

Figure 6-1 MM32 model naming

7 Abbreviation

ADC	Analog Digital Converter
BKP	Backup Register
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access Controller
EXTI	External Interrupt Event Controller
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
Flash	Flash Memory
GPIO	General-Purpose Input/Output
HSE	External High Speed Clock
HSI	Internal High Speed Clock
I2C	Inter-Integrated Circuit
IWDG	Independent Watchdog
LP	Low Power
LSI	Internal Low Speed Clock
NVIC	Nested Vectored Interrupt Controller
PWR	Power Control
POR	Power On Reset
PDR	Power Down Reset
PVD	Voltage Detector
RCC	Reset Clock Controller
RTC	Real-time Clock
SRAM	Static Random Access Memory
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug Interface
SysTick	System Tick Timer
Sleep	Sleep
Stop	Stop
Standby	Standby
TIM	Timer
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

8 Revision history

Table 8-1 Revision history

Date	Revision	Description
2023/01/03	Rev1.45	1. Deleted Cache related information 2. Updated the format of Ordering information
2022/12/07	Rev1.44	1. Added the maximum current at room temperature to Typical and maximum current consumption in Stop and Standby mode (1) 2. Added more data to Flash memory endurance and data retention period (1)(2) 3. Deleted blank rows in Comparator characteristics 4. Added class to ESD and latch-up characteristics
2022/10/19	Rev1.43	1. Added the power consumption at 120MHz to Typical current consumption in Run mode and Typical current consumption in Sleep mode 2. Updated LQFP and QFN package marketing and the related descriptions, added identification and description to temperature range 3. Added notes about I/O stat after power-on reset for general I/O ports and JTAG and BOOT0 related pins to Pin assignment table
2022/04/20	Rev1.42	1. Fixed the NRST related figures and values 2. Fixed the HSE and LSE related figures
2022/01/24	Rev1.41	Fixed the maximum value of voltage characteristics
2022/01/04	Rev1.4	1. Updated VBAT operating conditions 2. Removed external interrupt support on GPIO group H 3. Fixed I2C communication diagram wrong description 4. Fixed the BOOT pin name in LQFP144 and LQFP48 PB2 pin 5. Fixed some wrong abbreviation
2021/12/15	Rev1.3	1. Updated USB interface description 2. Deleted Ethernet related part numbers and descriptions 3. Updated ESD and LU data
2021/07/06	Rev1.02	2 Specification Updated part number list 4 Electrical characteristics Updated ESD data Updated power-on and power-down conditions
2021/05/12	Rev1.01	1 Overview Updated QFN40 package description 2 Specification Added LQFP48 and QFN40 part numbers 3 Pinout and assignment Added QFN40 pin assignment 5 Package dimensions Added QFN40 package dimensions
2021/04/08	Rev1.00	1. Formal release