Data Sheet

MM32L0130

Arm® Cortex®-M0+ based 32-bit Microcontrollers

Revision：1.0

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1 Introduction

1.1 Overview

The MM32L0130 microcontrollers are based on Arm® Cortex®-M0+ core. These devices have a maximum clocked frequency of 48MHz, built-in 64KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one comparator, two 16-bit general-purpose timers, two 16-bit basic timers, one low-power timer and one RTC counter as well as standard communication interfaces including two UART, one low-power UART, two SPI, two I2S and one I2C. Besides, this device is also embedded with SLCD and IRM.

The operating voltage of this product series is 1.8V to 5.5V, and the operating temperature range (ambient temperature) is -40°C to 85°C. Multiple sets of power-saving modes make the design of low-power applications possible.

These rich peripheral configurations make this device suitable for multiple applications.

- Air conditioner remote
- Thermostat
- Ear and forehead thermometer
- Portable medical device
- Gas, water, and heat meter
- Small appliance

This product series is available in LQFP64 and LQFP48.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M0+
  - Operating frequency up to 48MHz
- Memory
  - Up to 64KB embedded Flash storage
  - Up to 8KB SRAM
  - Embedded Bootloader to support In-System-Programming (ISP)
- Clock, reset and power management
  - Power supply ranges from 1.8 to 5.5V
  - Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - 4 to 24MHz high speed crystal oscillator
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
  - 8MHz factory-trimmed high speed RC oscillator, with the full temperature range

deviation of no more than ±2.5%

  - PLL supports CPU operating at a frequency of up to 48MHz and multiple frequency division mode
  - 16.384KHz low speed oscillator, with the full temperature range deviation of no more than ±3.5%
- Low power
  - Multiple low-power modes, including Lower Power Run, Sleep, Low Power Sleep, Stop, Deep Stop, Standby and Shutdown modes
- One 5-channel DMA controller to support peripherals including timer, ADC, UART, LPUART, I2C, SPI and SLCD
- 9 timers
  - Two 16-bit general-purpose timers (TIM3/TIM4) providing up to 4 input capture/output compare for IR control decoding
  - Two 16-bit basic timers (TIM16/TIM17) providing one input capture/output compare and one set of complementary output, with functions of dead time generation, emergency stop and modulator gate circuit for IR control
  - One LPTIM to wake up CPU in all modes except for Standby and Shutdown mode
  - Two watchdog timers (independent type and window type)
  - One RTC counter to support calendar function
  - One SysTick timer: 24-bit down counter
- Up to 57 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports can input and output signals whose voltage lower than V_{DD}
- Up to six communication interfaces
  - Two UART interfaces
  - One LPUART interface
  - One I2C interface
  - Two SPI interfaces (Two I2S interfaces)
- One IRM to support ASK/PSK/FSK modulation
- One SLCD able to drive 40x4 or 36x8 segments
- One 12-bit analog-to-digital converter with 1μS of conversion time, up to 15 external input channels and 1 internal input channel
  - Conversion range: 0 ~ V_{DDA}
  - Support the configuration of sampling time and resolution
  - On-chip temperature sensor
  - On-chip voltage sensor
- One comparator
- CRC calculation unit, with 8/16/32 polinomial configurable

- 96-bit unique ID (UID) of the chip
- Debug mode
  - Serial wire debug (SWD) interface
- Adopts LQFP64 and LQFP48 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers		MM32 L0131 B6P	MM32 L0136 B6P	MM32 L0131 C6P	MM32 L0136 C6P	MM32 L0131 B7P	MM32 L0136 B7P	MM32 L0131 C7P	MM32 L0136 C7P
CPU frequency		48 MHz Arm® Cortex®-M0+							
DMA		5ch							
Flash - KB		32		64		32		64	
SRAM - KB		4		8		4		8	
Timer	General-purpose (16-bit)	2	2	2	2	2	2	2	2
	Basic	2	2	2	2	2	2	2	2
	Low power	1	1	1	1	1	1	1	1
Communication interface	UART	2	2	2	2	2	2	2	2
	LPUART	1	1	1	1	1	1	1	1
	I2C	1	1	1	1	1	1	1	1
	SPI/I2S	2	2	2	2	2	2	2	2
GPIO number		41	41	41	41	57	57	57	57
SLCD		-	4x24 or 8x20	-	4x24 or 8x20	-	4x40 or 8x36	-	4x40 or 8x36
IRM		√	√	√	√	√	√	√	√
12-bit ADC	Number	1	1	1	1	1	1	1	1
	Channel	11	11	11	11	15	15	15	15
Comparator		1	1	1	1	1	1	1	1
RTC		√	√	√	√	√	√	√	√
Operating voltage		1.8V ~ 5.5V							
Operating temperature		-40°C ~ +85°C							
Package		LQFP48				LQFP64			

2.2 Marking information

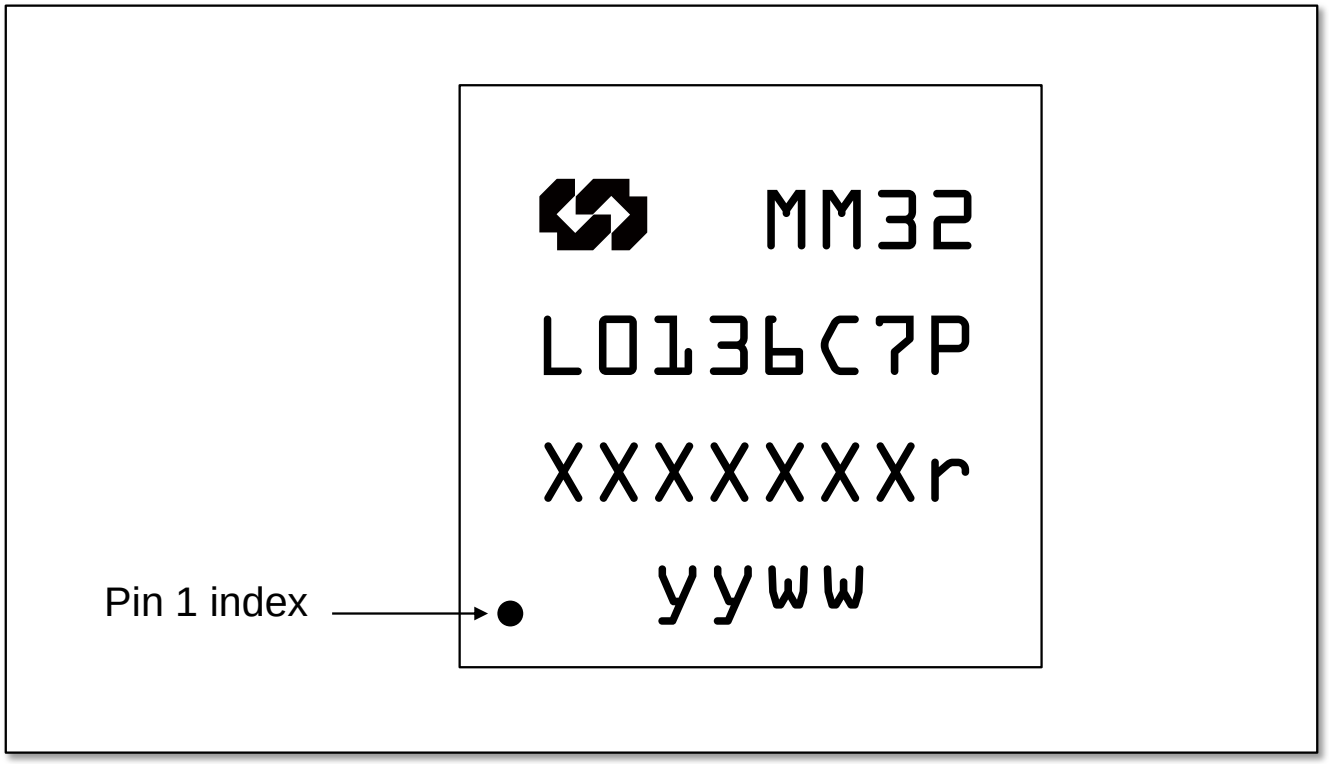

Figure 2-1 LQFP package marking

LQFP package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: L013xxxx
  - Second part of product name.
- 3rd line: XXXXXXXr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww

Date code, “yy” means year and “ww” means week in date code.

2.3 Part identification

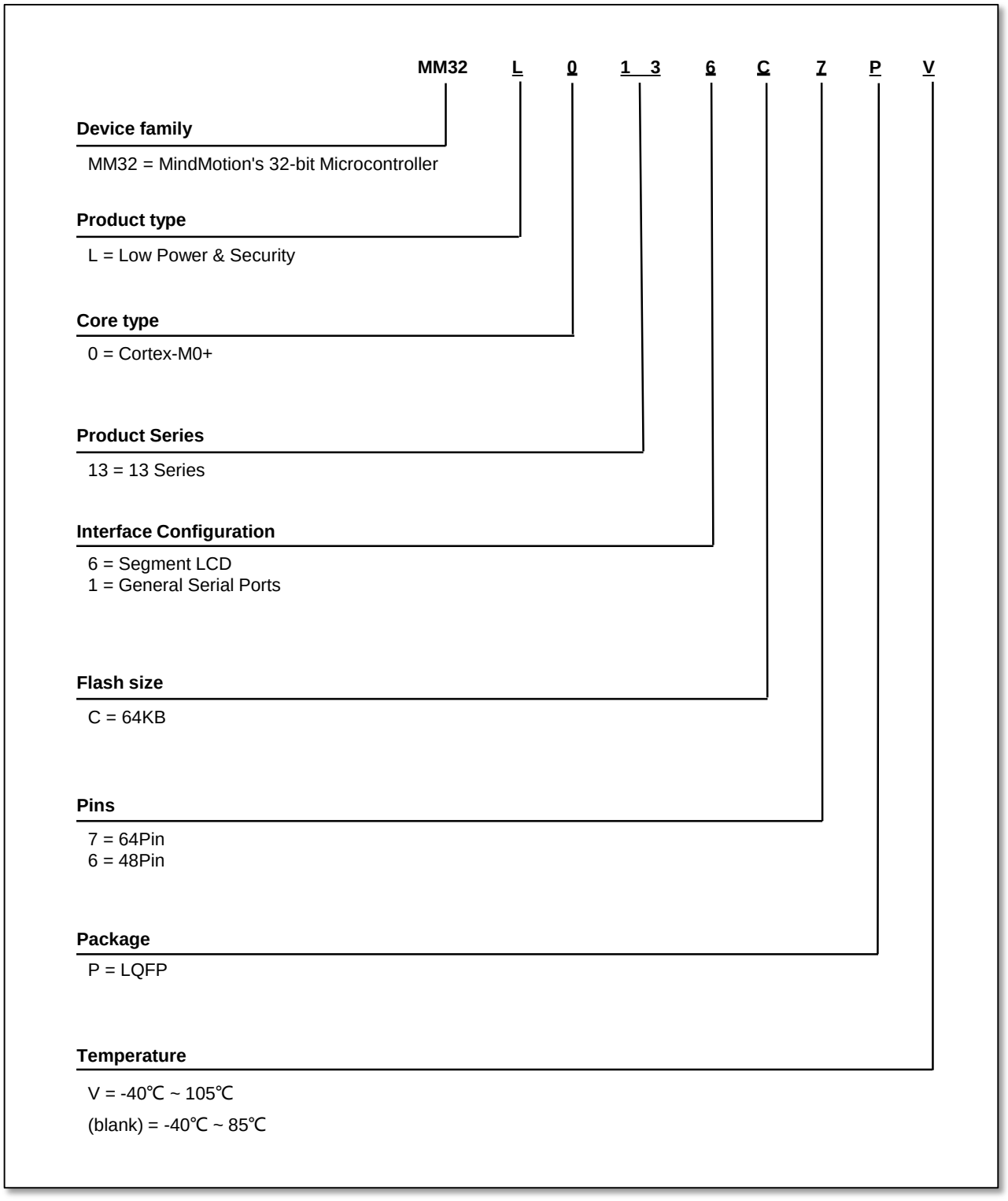

Figure 2-2 MM32 part number naming rule

3 Functional description

3.1 Block diagram

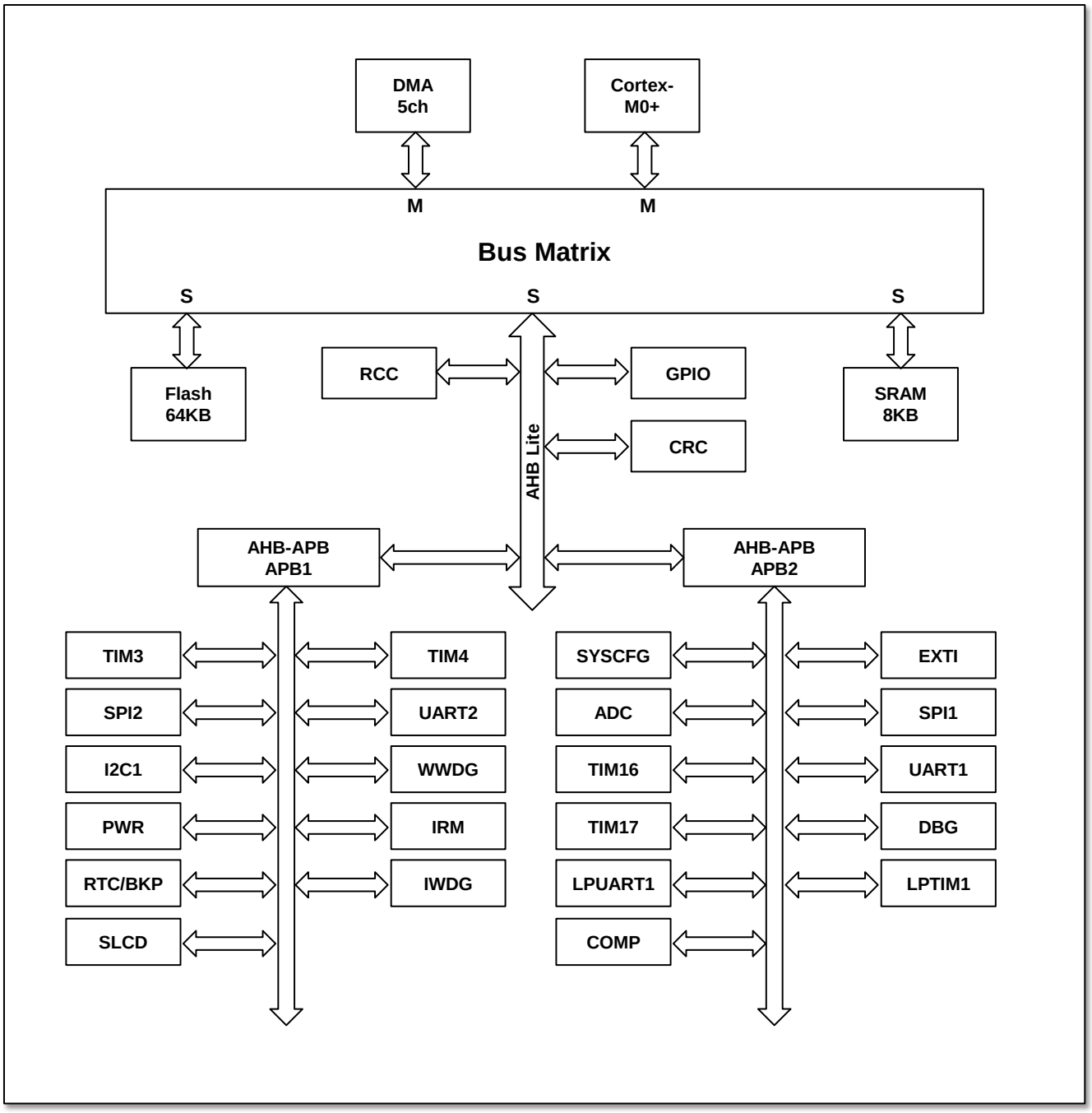

Figure 3-1 System block diagram

3.2 Core introduction

The Arm® Cortex®-M0+ is the latest generation of Arm processor for embedded system. It has been developed to provide a low-cost platform that meets the needs of MCU, with reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex®-M0+ is a 32-bit RISC processor, providing exceptional code-efficiency, and delivering the high performance expected from an Arm core, with memory sizes usually associated with 8- and 16-bit devices.

The device has embedded Arm core and is compatible with all Arm-based tools and software

3.3 Bus introduction

The bus matrix consists of an AHB interconnected matrix, an AHB bus and two bridged APB buses. When CPU and DMA are requesting simultaneously, it owns arbitration function. Peripherals (RCC, GPIO and CRC) of the AHB bus are connected to the system bus via the AHB interconnected matrix. The connections between the APB and AHB buses exchange data via the AHB2APB bridge. When the APB registers are accessed by 8-bit or 16-bit, the APB is automatically widened to 32-bit, and similarly, the AHB2APB bridge has an automatic widening function.

3.4 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x0000 0000 - 0x0000 FFFF	64 KB	Map to main Flash, system memory or SRAM according to boot configuration
	0x0000 0000 - 0x07FF FFFF	~128 MB	Reserved
	0x0800 0000 - 0x0800 FFFF	64 KB	Main Flash
	0x0801 0000 - 0x1FFD FFFF	~383 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000 - 0x1FFE 15FF	1.5 KB	Encrypted area
	0x1FFE 1600 - 0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5KB	Option bytes
	0x1FFF FA00 - 0x1FFF FFFF	1.5KB	Reserved
SRAM	0x2000 0000 - 0x2000 1FFF	8 KB	SRAM
	0x2000 2000 - 0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000 – 0x4000 03FF	1 KB	Reserved
	0x4000 0400 – 0x4000 07FF	1 KB	TIM3

Bus	Address range	Size	Peripheral
	0x4000 0800 – 0x4000 0BFF	1 KB	TIM4
	0x4000 0C00 – 0x4000 27FF	7 KB	Reserved
	0x4000 2800 – 0x4000 2BFF	1 KB	RTC/BKP
	0x4000 2C00 – 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 – 0x4000 33FF	1 KB	IWDG
	0x4000 3400 – 0x4000 37FF	1 KB	Reserved
	0x4000 3800 – 0x4000 3BFF	1 KB	SPI2
	0x4000 3C00 – 0x4000 43FF	2 KB	Reserved
	0x4000 4400 – 0x4000 47FF	1 KB	UART2
	0x4000 4800 – 0x4000 53FF	3 KB	Reserved
	0x4000 5400 – 0x4000 57FF	1 KB	I2C1
	0x4000 5800 – 0x4000 6FFF	1 KB	Reserved
	0x4000 7000 – 0x4000 73FF	1 KB	PWR
	0x4000 7400 – 0x4000 8FFF	1 KB	Reserved
	0x4000 9000 – 0x4000 93FF	1 KB	IRM
	0x4000 9400 – 0x4000 97FF	1 KB	LCD
	0x4000 9800 – 0x4000 FFFF	26 KB	Reserved
APB2	0x4001 0000 – 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 – 0x4001 07FF	1 KB	EXTI
	0x4001 0800 – 0x4001 0BFF	1 KB	LPUART1
	0x4001 0C00 – 0x4001 23FF	6 KB	Reserved
	0x4001 2400 – 0x4001 27FF	1 KB	ADC
	0x4001 2800 – 0x4001 2BFF	1 KB	LPTIM1
	0x4001 2C00 – 0x4001 2FFF	1 KB	Reserved
	0x4001 3000 – 0x4001 33FF	1 KB	SPI1
	0x4001 3400 – 0x4001 37FF	1 KB	DBG
	0x4001 3800 – 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 – 0x4001 3FFF	1 KB	COMP
	0x4001 4000 – 0x4001 43FF	1 KB	Reserved
	0x4001 4400 – 0x4001 47FF	1 KB	TIM16
	0x4001 4800 – 0x4001 4BFF	1 KB	TIM17
	0x4001 4C00 – 0x4001 FFFF	45 KB	Reserved
AHB	0x4002 0000 – 0x4002 03FF	1KB	DMA
	0x4002 0400 – 0x4002 0FFF	3KB	Reserved
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 1400 – 0x4002 1FFF	3KB	Reserved
	0x4002 2000 – 0x4002 23FF	1KB	Flash Interface
	0x4002 2400 – 0x4002 2FFF	3KB	Reserved

Bus	Address range	Size	Peripheral
	0x4002 3000 – 0x4002 33FF	1KB	CRC
	0x4002 3400 – 0x47FF FFFF	~128MB	Reserved

3.5 Flash

This product provides up to 64KB embedded Flash memory available for storing program and data.

3.6 SRAM

This product provides up to 8KB embedded SRAM.

3.7 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0+) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Support high priority interrupt preemption
- Support interrupt tail-chaining
- Automatically save processor status
- Automatic restoration when the interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

3.8 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event request. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 bus clock period.

3.9 Clock and boot

The system clock is selected after the chip is booted. After reset, the internal 8 MHz

oscillator is used as the default system clock, and then an external 4 ~ 24 MHz clock source can be used. When an invalid external clock is monitored, the system will automatically mask the external clock source, turn off the PLL, and use the internal oscillator. At that time, if the associated interrupt monitoring switch is enabled, a corresponding interrupt request will also be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and high-speed APB (APB1 and APB2) bus. The maximum frequency of the AHB and high-speed APB bus clock can reach up to 48MHz. The clock tree of the clock system is shown in Figure 3-2.

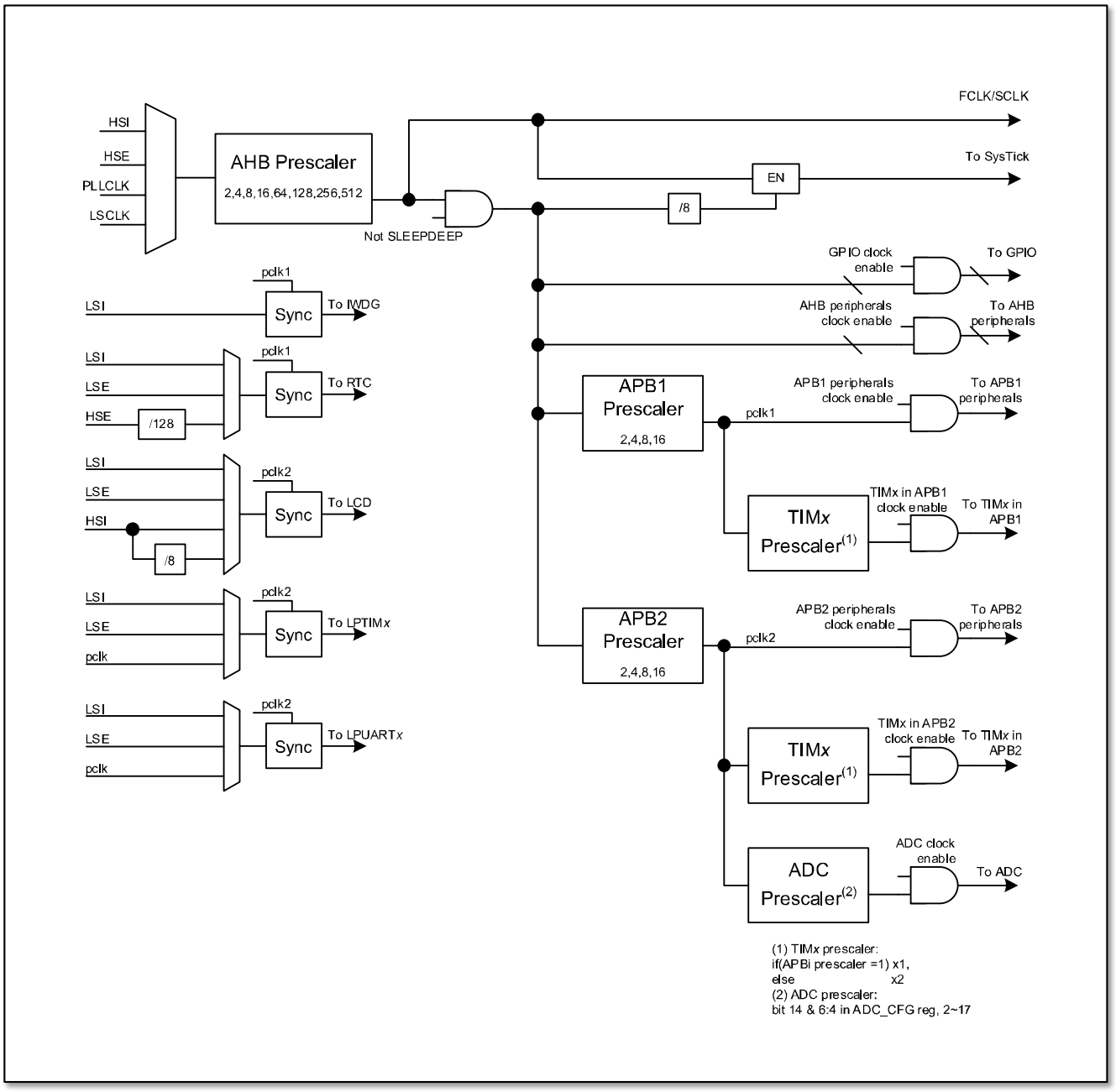

Figure 3-2 Clock tree

3.10 Boot mode

During boot, BOOT0 pin and nBoot1 bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader proram locates in the system memory. Once the Bootloader boots from the system memory, it will program the embedded Flash through UART1.

3.11 Power supply scheme

- V_{DD} = 1.8V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- VDDA = 1.8V ~ 5.5V: ADC, reset module, oscillator and PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually (when powered individually, the voltage should be the same as the V_{DD} and V_{SS}).

Note: The performance of the analog module conforms to this manual's specification only when V_{DDA} = 2.5V ~ 5.5V

3.12 Power supply supervisor

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is always in operation to ensure that the chip can work when the system power supply exceeds 1.8V. When the V_{DD} is lower than the preset threshold ($V_{POR/PDR}$), this circuit will put system to reset status, without the need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), which can monitor the V_{DD} and V_{DDA} power supply, and make comparison with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through program.

3.13 Voltage regulator

The on-chip voltage regulator can convert the external voltage to the one at which the internal logic circuit operates. The voltage regulator is workable after chip reset.

3.14 Low power mode

This product supports low power mode that allows for an optimal balance among low

power consumption, short boot time and multiple wake-up events.

Low Power Run

Low Power Run mode can function with VCORE provided by a low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or Flash, and the CPU frequency is limited to 2MHz.

Sleep

In Sleep mode, only the CPU clock is gated off. All peripherals are in operation and can wake up the CPU when an interrupt/event occurs.

Low Power Sleep

Enter this mode from Low Power Run mode. Only the CPU clock is stopped. When an event or interrupt triggers a wakeup, the system will restore to Low Power Run mode.

Stop

The Stop mode can achieve lower power consumption with SRAM and register contents being intact. In Stop mode, HSI oscillator and HSE crystal oscillator are turned off. The microcontroller can be woken up from the Stop mode by signals configured as EXTI. The EXTI signals can be the wake-up source signal from one of the 16 externa I/O ports or PVD output.

Deep Stop

It is the same with the Stop mode, but can achieve lower power consumption.

Standby

In Standby mode, the voltage regulator is powered off when CPU is in Deep Sleep mode, and all the 1.5V domain are shut down. PLL, HSI and HSE are also powered off, and can be woken up by the rising edge on WKUP pin, the external reset on NRST pin as well as IWDG reset or woken up and reset by watchdog timer. SRAM and registers content are lost. Only backup register and Standby circuit are powered.

Shutdown

The lowest system power consumption can be achieved in Shutdown mode, in which all internal regulators and BOR are turned off, and only POR and other VDD domain circuits work normally (Part logic of PMU/POR/IO Wakeup logic).

3.15 DMA

The flexible 5-channel general-purpose DMA can be used to manage data transfer from memory to memory, device to memory or memory to device. The DMA controller support ring buffer managment, avoiding interrupts generated when the controller transfer reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic. All channels can be triggered by software simultaneously. The length, source and destination address of the transfer can be set independently by software.

DMA can be used for peripherals including UART, I2C, SPI, ADC, and timer.

3.16 TIM & WDG

This product has two general-purpose timers, two basic timers, one LPTIM, two watchdog timers and one Systick timer. The table below compares the features of general-purpose, basic and low power timers:

Table 3-2 Comparison of timer functions

Timer type	Name	Counter resolution	Counter direction	Pre-divider	DMA request generation	Capture/compare channel	Complementary output
General-purpose	TIM3/TIM4	16-bit	up, down, up/down	Any integer between 1 ~ 65536	Yes	4	No
Basic	TIM16/TIM17	16-bit	up, down, up/down	Any integer between 1 ~ 65536	Yes	1	Yes
Low power	LPTIM1	16-bit	Up	Any integer between 1 ~ 128	Yes	No	No

General-purpose timer (TIM3 / TIM4)

This product has two 16-bit general-purpose timers (TIM3, TIM4). Each timer has one 16-bit counter, supporting both up and down counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or one pulse mode output.

These timers can also work together through the timer linking function to offer synchronization or event linking. Counters can be frozen in the debug mode. Any general-purpose timer can be used to produce PWM output. Each timer has a separate DMA request mechanism.

These timers can also handle signals from incremental encoders and digital output from 1~4 Hall sensors. Each timer can produce PWM output or be taken as a simple time reference.

Basic timer (TIM16 / TIM17)

This product has two 16-bit basic timers (TIM16, TIM17). Each timer has one 16-bit counter, supporting both up and down counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and one independent channel. Each channel can be used as input capture, output compare, PWM or one pulse mode

output. When working in PWM mode, this timer supports complementary ports to generate complementary PWM pairs and support hardware dead time insertion function.

LPTIM1

This product has one 16-bit LPTIM1. This timer consists of one 16-bit counter, which can provide users with convenient counting and timing functions. The LPTIM can operate in various low-power modes and features low power consumption. The clock of LPTIM can also be provided by an external clock. If LPTIM works without an internal clock, the external pulse counting function can be achieved in Sleep mode. Low-power timeout wake-up can be achieved via an external input trigger signal. LPTIM can be used for a variety of purposes, such as external clock counting, timeout wake-up function, and PWM output.

IWDG

The independent watchdog is based on one 12-bit down counter and one 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in Stop and Standby mode. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

WWDG

The window watchdog has one 7-bit down counter and can be set as free running. It can be taken as watchdog to reset the entire system when an error occurs. It is driven by the main clock and has early warning interrupt function. In debug mode, the counter can be frozen.

Systick

This timer is dedicated to the real-time operating system and can also be used as a standard down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.17 RTC

RTC is an independent timer and supports hardware calendar

3.18 Backup register

The backup register is composed of ten 16-bit registers that can be used to store user application data. These registers will not reset when the system is woken up in Standby mode, or when the system or power is reset.

3.19 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals.

If necessary, the peripheral functions of the I/O pins can be locked by a specific operation to avoid accidental writing to the I/O register.

3.20 UART

This product has two UART interfaces. The UART interface supports LIN master and slave function and is compatible with ISO7816 smart card. It also supports configurable output data length of 5-, 6-, 7-, 8-, and 9-bits.

All UART interfaces support DMA operation

3.21 LPUART

This product has one built-in low power UART interface (LPUART). Compared with UART, it has lower power consumption and supports running and waking up the chip in Sleep and Deep Sleep mode.

3.22 I2C

This product has one built-in I2C bus. The I2C bus interface can work in multi-master mode or slave mode and supports standard and fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

3.23 SPI

This product has two built-in SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in slave or master mode, allowing up to 12 Mbps in master mode and 6 Mbps in slave mode.

All SPI interfaces support DMA operation.

3.24 I2S

This product has two built-in I2S interfaces. The I2S interface shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave) and frame error flag in receive and transmit mode (only slave).

8-bit programmable linear prescaler is used to achieve precise audio sampling frequency (8KHz to 192KHz).

The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.25 IRM

This product has one built-in IRM. The IRM module uses the on-chip timer and serial port to achieve the ASK/PSK/FSK modulation of data for IR code sending.

3.26 SLCD

This product embeds with SLCD. Its features are seen below:

- Able to drive 40x4 or 36x8 segments
- Any LCD pin can be configured as COM or SEG function
- Built-in charge pump to keep the LCD screen clear when the power supply voltage drops
- Support static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycles
- Configurable 1/2, 1/3 and 1/4 bias voltage
- Adjustable contrast
- Flexible control of display frame rate
- Built-in 16*32bit display data register for storing display data
- Support flashing function with which 1~8 segments or all segments can be chosen to flash and frequency 0.5Hz/1Hz/2Hz/4Hz is configurable
- Available in all low power modes except Shutdown mode

3.27 ADC

This product has one 12-bit analog/digital converter (ADC), with up to 15 ADC external channels available, supports single-shot, single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The analog watchdog function allows precise monitoring of one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated.

The events generated by the general-purpose timers (TIMx) and the advanced timers can be internally cascaded to the ADC trigger, in this way the ADC can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.28 COMP

This product has one built-in analog comparator, which can be used independently (applicable to I/O ports on all terminals) or combined with timers. The COMP module can be used for a variety of functions including:

- low-power mode wake-up event triggered by analog input
- Adjust analog signal
- Rail-to-rail comparator
- Each comparator has selectable thresholds
  - Multiplexed I/O pin
  - The internal comparison voltage CRV can select the divided voltage value of V_{DDA} or internal reference voltage
- Programmable hysteresis voltage
- Programmable rate and power consumption
- Output end can be redirected to one I/O port or multiple timer input ends, which can trigger the following events:
  - Capture event
- Break event for fast PWM interrupt

3.29 CRC

This product has one built-in CRC computation unit to support 8/16/32-bit configurable polynomial.

3.30 Debug

This product embeds with Arm standard two-wire serial debug interface (SW-DP).

4 Pinout and multiplexing function

4.1 Pinout diagram

4.1.1 LQFP64 pinout

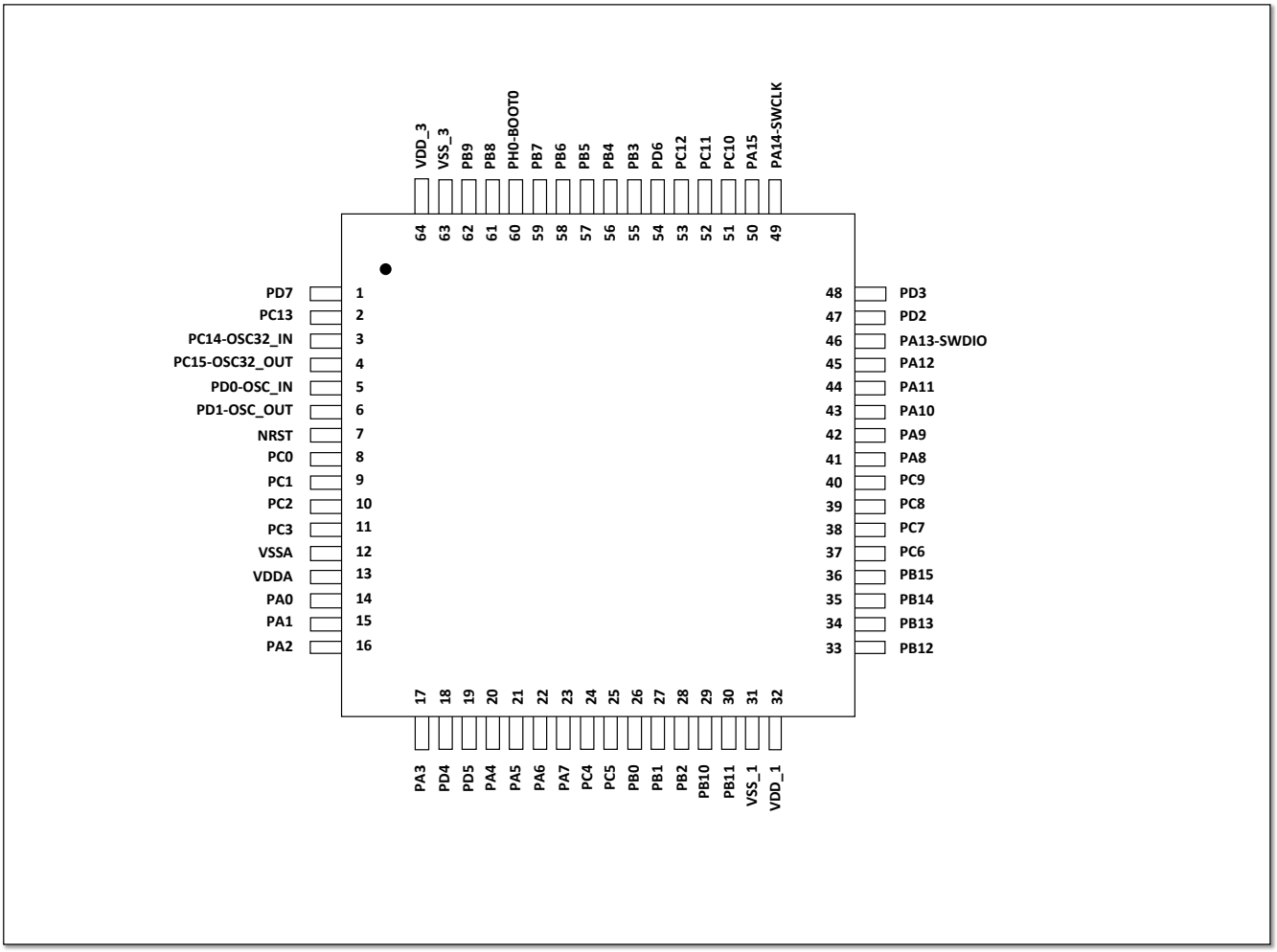

Figure 4-1 LQFP64 pinout diagram

4.1.2 LQFP48 pinout

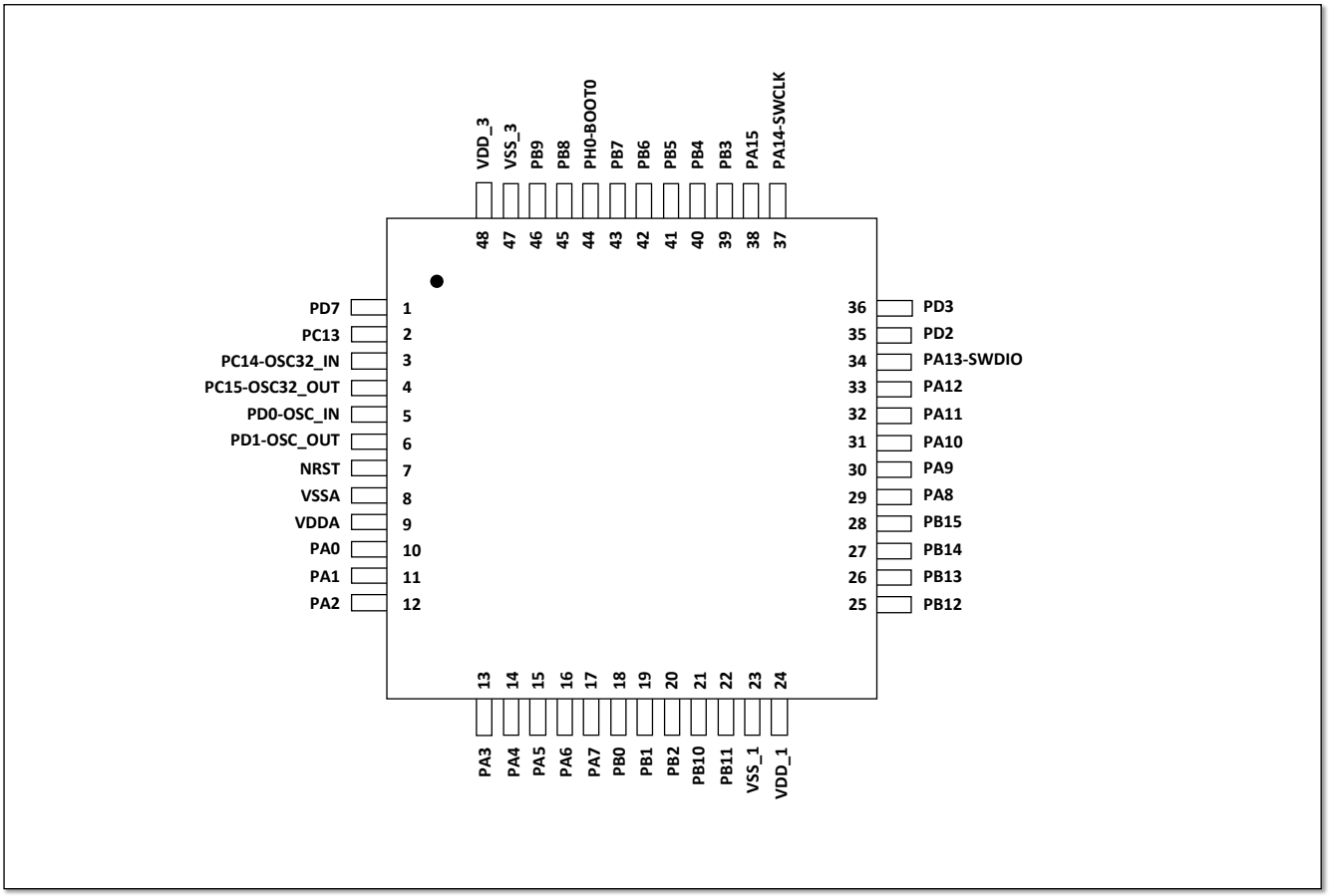

Figure 4-2 LQFP48 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment

LQFP 64	LQFP 48	Name	Type (1)	I/O level (2)	Main function	Multiplex function	LCD function	Additional function
1	1	PD7	I/O	TC	PD7	TIM3_CH1 TIM4_CH4 TIM17_CH1	L1	WKP3
2	2	PC13	I/O	TC	PC13	TIM4_CH1/TIM4_ETR	L0	WKP2 RTC_TAMP1 RTC_TS RTC_OUT (3)
3	3	PC14 OSC32_IN	I/O	TC	PC14	TIM4_CH2	-	OSC32_IN
4	4	PC15 OSC32_OUT	I/O	TC	PC15	TIM4_CH3	-	OSC32_OUT
5	5	PD0 OSC_IN	I/O	TC	PD0	I2C1_SDA UART1_TX SPI1_MOSI/I2S1_SD	-	OSC_IN
6	6	PD1 OSC_OUT	I/O	TC	PD1	I2C1_SCL UART1_RX SPI1_MISO/I2S1_MCK	-	OSC_OUT
7	7	NRST	NRST	-	NRST	-	-	-
8	-	PC0	I/O	TC	PC0	EVENTOUT LPUART1_TX	L43	ADC_IN11
9	-	PC1	I/O	TC	PC1	EVENTOUT LPUART1_RX	L42	ADC_IN12
10	-	PC2	I/O	TC	PC2	EVENTOUT SPI2_MISO/I2S2_MCK LPTIM1_TRIGGER	L41	ADC_IN13
11	-	PC3	I/O	TC	PC3	EVENTOUT SPI2_MOSI/I2S2_SD LPTIM1_OUT	L40	ADC_IN14
12	8	VSSA	S	-	VSSA	-	-	-
13	9	VDDA	S	-	VDDA	-	-	-
14	10	PA0	I/O	TC	PA0	UART2_CTS TIM4_CH1/TIM4_ETR UART1_RX COMP1_OUT	L39	ADC_IN0 COMP1_INP0 COMP1_INM2 WKP1 TAMP2
15	11	PA1	I/O	TC	PA1	UART2_RTS TIM4_CH2 UART1_TX	L38	ADC_IN1 COMP1_INP1
16	12	PA2	I/O	TC	PA2	UART2_TX TIM4_CH3	L37	ADC_IN2 COMP1_INP2 WKP4
17	13	PA3	I/O	TC	PA3	UART2_RX TIM4_CH4	L36	ADC_IN3 COMP1_INP3
18	-	PD4	I/O	TC	PD4	SPI1_MISO/I2S1_MCK	L35	-
19	-	PD5	I/O	TC	PD5	SPI1_MOSI/I2S1_SD	L34	-
20	14	PA4	I/O	TC	PA4	SPI1_NSS/I2S1_WS LPUART1_TX TIM16_CH1N	L33	ADC_IN4 COMP1_INM0
21	15	PA5	I/O	TC	PA5	SPI1_SCK/I2S1_CK TIM4_CH1/TIM4_ETR LPUART1_RX TIM17_CH1N	L32	ADC_IN5 COMP1_INM1

LQFP 64	LQFP 48	Name	Type (1)	I/O level (2)	Main function	Multiplex function	LCD function	Additional function
22	16	PA6	I/O	TC	PA6	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM16_CH1 EVENTOUT COMP1_OUT	L31	ADC_IN6
23	17	PA7	I/O	TC	PA7	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM17_CH1 EVENTOUT	L30	ADC_IN7
24	-	PC4	I/O	TC	PC4	EVENTOUT UART2_TX TIM3_CH1 SPI1_MOSI/I2S1_SD	L29	-
25	-	PC5	I/O	TC	PC5	UART2_RX TIM3_CH2 SPI1_MISO/I2S1_MCK	L28	WKP5
26	18	PB0	I/O	TC	PB0	TIM3_CH3	L27	ADC_IN8
27	19	PB1	I/O	TC	PB1	TIM3_CH4	L26	ADC_IN9
28	20	PB2	I/O	TC	PB2	EVENTOUT	L25	ADC_IN10
29	21	PB10	I/O	TC	PB10	TIM4_CH3 I2C1_SCL SPI2_SCK/I2S2_CK	L24	-
30	22	PB11	I/O	TC	PB11	EVENTOUT TIM4_CH4 I2C1_SDA	L23	-
31	23	VSS_1	S	-	VSS_1	-	-	-
32	24	VDD_1	S	-	VDD_1	-	-	-
33	25	PB12	I/O	TC	PB12	SPI2_NSS/I2S2_WS EVENTOUT	L22	-
34	26	PB13	I/O	TC	PB13	SPI2_SCK/I2S2_CK LPTIM1_TRIGGER I2C1_SCL TIM17_CH1	L21	-
35	27	PB14	I/O	TC	PB14	SPI2_MISO/I2S2_MCK RTC_OUT (4) LPTIM1_OUT I2C1_SDA	L20	-
36	28	PB15	I/O	TC	PB15	SPI2_MOSI/I2S2_SD	L19	-
37	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM3_CH3 SPI1_NSS/I2S1_WS	L18	-
38	-	PC7	I/O	TC	PC7	TIM3_CH2 SPI1_SCK/I2S1_CK	L17	-
39	-	PC8	I/O	TC	PC8	TIM3_CH3	L16	-
40	-	PC9	I/O	TC	PC9	TIM3_CH4	L15	-
41	29	PA8	I/O	TC	PA8	MCO RTC_OUT (4)	L14	-
42	30	PA9	I/O	TC	PA9	UART1_TX I2C1_SCL MCO IROUT	L13	-
43	31	PA10	I/O	TC	PA10	TIM17_BKIN1 UART1_RX I2C1_SDA TIM16_CH1 IROUT	L12	-

LQFP 64	LQFP 48	Name	Type (1)	I/O level (2)	Main function	Multiplex function	LCD function	Additional function
44	32	PA11	I/O	TC	PA11	UART1_CTS I2C1_SCL COMP1_OUT	L11	-
45	33	PA12	I/O	TC	PA12	UART1_RTS I2C1_SDA	L10	-
46	34	PA13 SWDIO	I/O	TC	PA13	SWDIO UART1_TX	-	-
47	35	PD2	I/O	TC	PD2	I2C1_SCL SPI1_NSS/I2S1_WS	L9	-
48	36	PD3	I/O	TC	PD3	I2C1_SDA SPI1_MISO/I2S1_MCK	L8	-
49	37	PA14 SWCLK	I/O	TC	PA14	SWCLK UART2_TX UART1_RX	-	-
50	38	PA15	I/O	TC	PA15	SPI1_NSS/I2S1_WS UART2_RX TIM4_CH1/TIM4_ETR SPI2_SCK/I2S2_CK	L7	-
51	-	PC10	I/O	TC	PC10	UART1_TX SPI2_MISO/I2S2_MCK	L6	-
52	-	PC11	I/O	TC	PC11	UART1_RX SPI2_MOSI/I2S2_SD	L5	-
53	-	PC12	I/O	TC	PC12	UART1_TX SPI2_NSS/I2S2_WS	L4	-
54	-	PD6	I/O	TC	PD6	TIM3_ETR	V4/L58	-
55	39	PB3	I/O	TC	PB3	SPI1_SCK/I2S1_CK TIM4_CH2	V3/L59	-
56	40	PB4	I/O	TC	PB4	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM17_BKIN2	V2/L60	-
57	41	PB5	I/O	TC	PB5	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM16_BKIN1	V1/L61	WKP6
58	42	PB6	I/O	TC	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM4_CH1	LCDCAP 2/L62	-
59	43	PB7	I/O	TC	PB7	UART1_RX I2C1_SDA TIM17_CH1N TIM4_CH2	LCDCAP 1/L63	-
60	44	PH0 BOOT0	I/O	TC	PH0	-	-	BOOT0
61	45	PB8	I/O	TC	PB8	LPUART1_RX I2C1_SCL TIM16_CH1 TIM4_CH3 IROUT	L3	-
62	46	PB9	I/O	TC	PB9	LPUART1_TX I2C1_SDA TIM17_CH1 EVENTOUT SPI2_NSS/I2S2_WS TIM4_CH4	L2	-
63	47	VSS_3	S	-	VSS_3	-	-	-
64	48	VDD_3	S	-	VDD_3	-	-	-

1. I = input, O = output, S = power supply, HiZ = high resistance state
2. TC: standard IO. Input signal level should not exceed V_{DD} voltage
3. RTC domain RTC_OUT

4. Core domain RTC_OUT

4.3 GPIO multiplexing table

Table 4-2 PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM4_CH1/TIM4_ETR	-	-	-	UART1_RX	COMP1_OUT
PA1	-	UART2_RTS	TIM4_CH2	-	-	-	UART1_TX	-
PA2	-	UART2_TX	TIM4_CH3	-	-	-	-	-
PA3	-	UART2_RX	TIM4_CH4	-	-	-	-	-
PA4	SPI1_NSS/I2S1_WS	-	-	LPUART1_TX	-	TIM16_CH1N	-	-
PA5	SPI1_SCK/I2S1_CK	-	TIM4_CH1/TIM4_ETR	LPUART1_RX	-	TIM17_CH1N	-	-
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	-	TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	-	-	-	TIM17_CH1	EVENTOUT	-
PA8	MCO	-	RTC_OUT	-	-	-	-	-
PA9	-	UART1_TX	-	-	I2C1_SCL	MCO	-	IROUT
PA10	TIM17_BKIN1	UART1_RX	-	-	I2C1_SDA	-	TIM16_CH1	IROUT
PA11	-	UART1_CTS	-	-	-	I2C1_SCL	-	COMP1_OUT
PA12	-	UART1_RTS	-	-	-	I2C1_SDA	-	-
PA13	SWDIO	-	-	UART1_TX	-	-	-	-
PA14	SWCLK	UART2_TX	-	UART1_RX	-	-	-	-
PA15	SPI1_NSS/I2S1_WS	UART2_RX	TIM4_CH1/TIM4_ETR	SPI2_SCK/I2S2_CK	-	-	-	-

Table 4-3 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	-	-	-	-	-	-
PB1	-	TIM3_CH4	-	-	-	-	-	-
PB2	-	-	EVENTOUT	-	-	-	-	-
PB3	SPI1_SCK/I2S1_CK	-	TIM4_CH2	-	-	-	-	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	-	TIM17_BKIN2	-	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN1	-	-	-	-	-
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	TIM4_CH1	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM4_CH2	-
PB8	LPUART1_RX	I2C1_SCL	TIM16_CH1	-	-	-	TIM4_CH3	IROUT
PB9	LPUART1_TX	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS/I2S2_WS	TIM4_CH4	-
PB10	-	-	TIM4_CH3	I2C1_SCL	-	SPI2_SCK/I2S2_CK	-	-
PB11	EVENTOUT	-	TIM4_CH4	I2C1_SDA	-	-	-	-
PB12	SPI2_NSS/I2S2_WS	-	-	EVENTOUT	-	-	-	-
PB13	SPI2_SCK/I2S2_CK	-	-	LPTIM1_TRIGGER	-	I2C1_SCL	TIM17_CH1	-
PB14	SPI2_MISO/I2S2_MCK	-	RTC_OUT	LPTIM1_OUT	-	I2C1_SDA	-	-
PB15	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-

Table 4-4 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	LPUART1_TX	-	-	-	-	-
PC1	EVENTOUT	-	LPUART1_RX	-	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I2S2_MCK	-	LPTIM1_TRIGGER	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I2S2_SD	-	LPTIM1_OUT	-	-	-	-
PC4	EVENTOUT	-	-	UART2_TX	-	TIM3_CH1	SPI1_MOSI/I2S1_SD	-
PC5	-	-	-	UART2_RX	-	TIM3_CH2	SPI1_MISO/I2S1_MCK	-
PC6	TIM3_CH1	-	-	-	-	TIM3_CH3	SPI1_NSS/I2S1_WS	-
PC7	TIM3_CH2	-	-	-	-	-	SPI1_SCK/I2S1_CK	-
PC8	TIM3_CH3	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-
PC10	-	-	UART1_TX	SPI2_MISO/I2S2_MCK	-	-	-	-
PC11	-	-	UART1_RX	SPI2_MOSI/I2S2_SD	-	-	-	-
PC12	-	-	UART1_TX	SPI2_NSS/I2S2_WS	-	-	-	-
PC13	-	-	-	-	-	-	TIM4_CH1/TIM4_ETR	-
PC14	-	-	-	-	-	-	TIM4_CH2	-
PC15	-	-	-	-	-	-	TIM4_CH3	-

Table 4-5 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	-	UART1_TX	-	SPI1_MOSI/I2S1_SD	-	-
PD1	-	I2C1_SCL	-	UART1_RX	-	SPI1_MISO/I2S1_MCK	-	-
PD2	-	I2C1_SCL	-	-	-	-	SPI1_NSS/I2S1_WS	-
PD3	-	I2C1_SDA	-	-	-	-	SPI1_MISO/I2S1_MCK	-
PD4	SPI1_MISO/I2S1_MCK	-	-	-	-	-	-	-
PD5	SPI1_MOSI/I2S1_SD	-	-	-	-	-	-	-
PD6	TIM3_ETR	-	-	-	-	-	-	-
PD7	-	-	-	-	-	TIM3_CH1	TIM4_CH4	TIM17_CH1

Table 4-6 PH port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PH0	-	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

5.1.1 Load capacitor

The load conditions for measuring pin parameters are shown in the Figure 5-1.

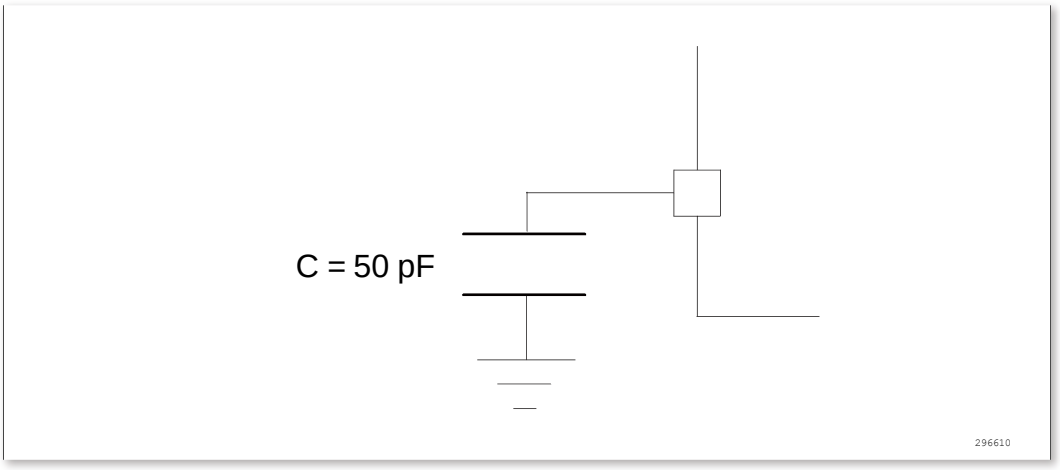

Figure 5-1 Load condition of the pin

5.1.2 Pin input voltage

The measurement of the input voltage on the pin is shown in Figure 5-2.

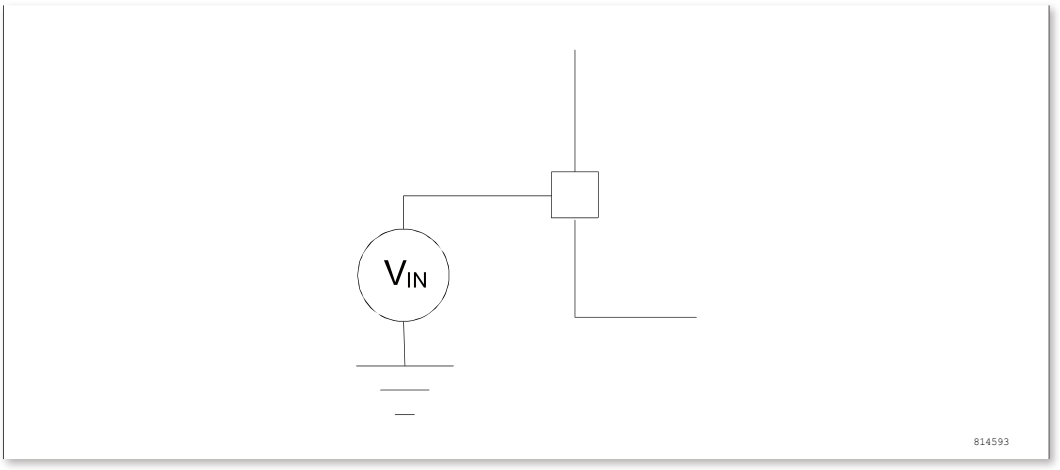

Figure 5-2 Pin input voltage

5.1.3 Power scheme

The power supply design scheme is shown in Figure 5-3.

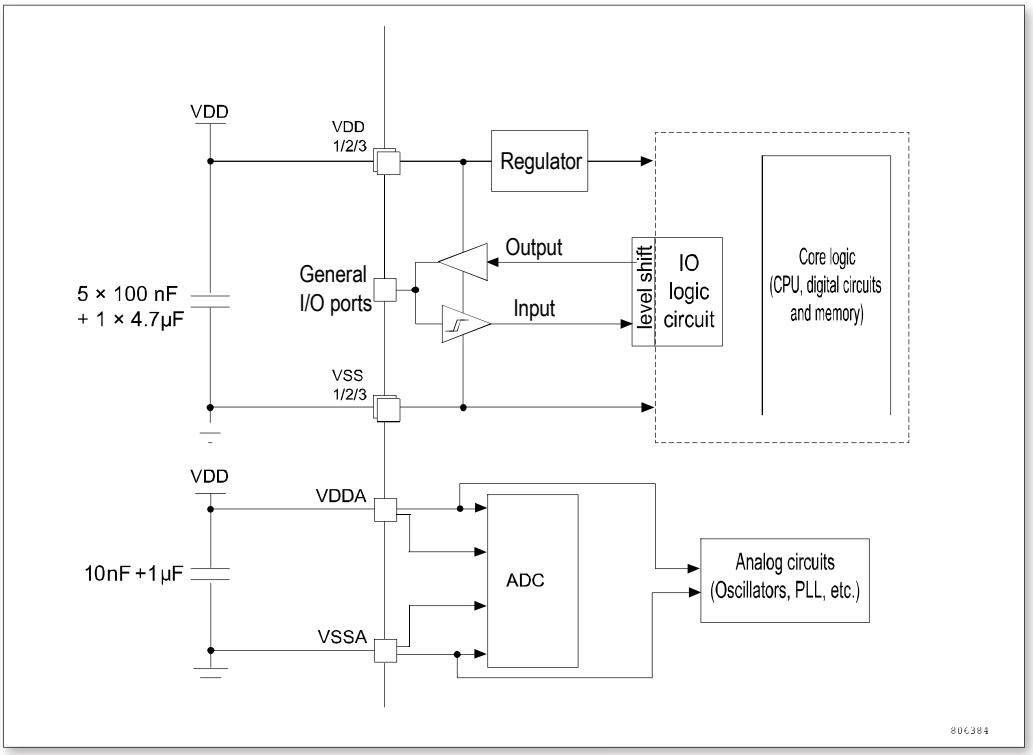

Figure 5-3 Power scheme

5.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 5-4.

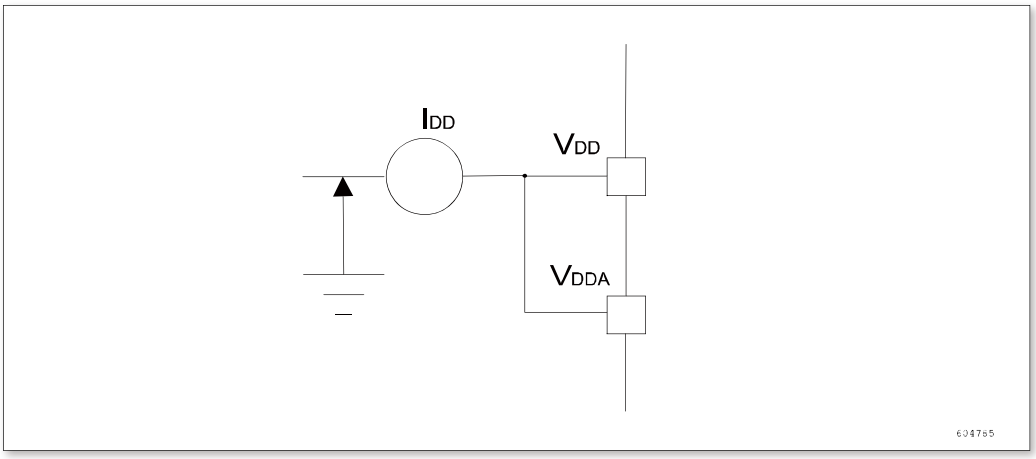

Figure 5-4 Current consumption measurement scheme

5.2 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 5-1, Table 5-2 and Table 5-3) may cause permanent damage to the

device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA})(1)	-0.3	5.8	V
V_{IN}(2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (V_{DD} and V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply system within the permitted range.
2. The maximum value of V_{IN} must be respected. Refer to Table 5-2 for the maximum allowed injected current values.

Table 5-2 Current characteristics

Symbol	Description	Maximum	Unit
$I_{VDD/VDDA}$ (1)	Total current through V_{DD}/V_{DDA} power pins (supply current) (1)	+120	mA
$I_{VSS/VSSA}$ (1)	Total current through V_{SS}/V_{SSA} ground pins (outflow current) (1)	-120	
I_{IO}	Output sink current on any I/O and control pins	+25	
	Output current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (6)	Other pins injection current (5)	±25	

1. All main power (V_{DD} and V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to an external power supply in the permitted range.
2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP package.
3. The reverse injection current can interfere with the analog performance of the device.
4. There is no forward injection on these I/Os, and no forward injection will occur when the input voltage is lower than the specified maximum value.
5. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.
6. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value) .

5.3 Operating condition

5.3.1 General operating condition

Table 5-3 General operating condition

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	48	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	-	-	48	
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	48	
V_{DD}	Digital circuit operating voltage	-	1.8	3.3	5.5	V
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD} (1)	2.5	3.3	5.5	
	Analog circuit operating voltage (Performance is not guaranteed)		1.8	-	2.5	
P_D	Power dissipation Temperature: T_A = 85°C (2)	LQFP64	-	-	339	mW
		LQFP48	-	-	357	
T_A	Ambient temperature (industrial level)	-	-40	-	85	℃
T_J	Junction temperature (3) (industrial level)	-	-40	-	105	℃

1. It is recommended that V_{DD} and V_{DDA} should be supplied with the same power supply, allowing a maximum difference of 300 mV between V_{DD} and V_{DDA} during power-up and normal operation.
2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

5.3.2 Operating condition at power-up/power-down

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-4 Operating condition at power-up/power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD} (1)(2)	V_{DD} rise time t_r	300	-	∞	us
	V_{DD} fall time t_f	300	-	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1. Drawn from comprehensive evaluation, not tested in production
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phase in the following waveform diagram, and no power-down is allowed during power-on process.
3. To ensure the reliability of chip power-on, all power-on should start from 0V.

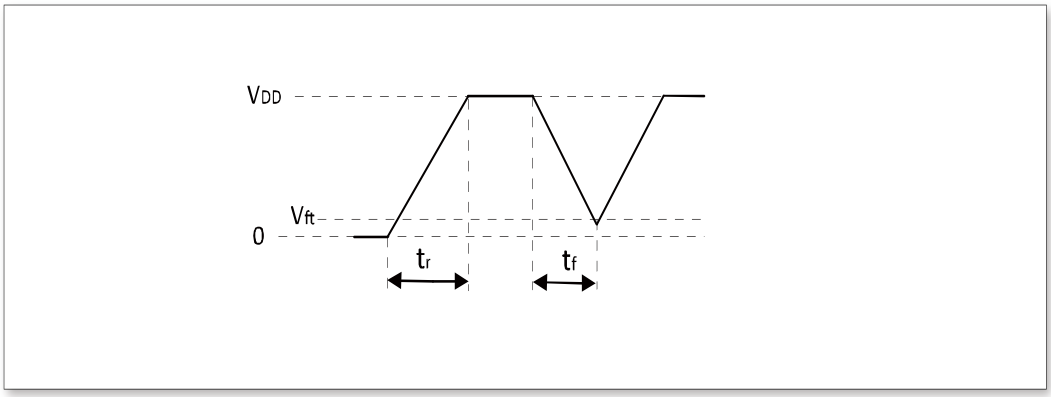

Figure 5-5 Power-on and power-down waveforms

5.3.3 Embedded reset and power control module characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed inTable 5-3.

Table 5-5 Embedded reset and power control module characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{POR/PDR}$ (1)	Power-on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	30	-	mV
$T_{RSTTEMPO}$ (2)(3)	Reset duration	-	-	4	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction

5.3.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed inTable 5-3.

Table 5-6 Built-in voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	T_A = 25°C	1.15	1.187	1.25	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	-	-	11.8	-	us

1. The shortest sampling time is obtained through multiple tests.
2. The conversion result of the built-in reference voltage ADC is stored in 0x1FFFF7E0 low 12bit.

5.3.5 Supply current characteristics

The current consumption is a function of multiple parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequency, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a set of reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned

- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle).
- The instruction prefetching function is on. When the peripherals are enabled: $f_{HCLK} = f_{PCLK1} = f_{PCLK2}$.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 5-3.

Table 5-7 Typical current consumption in Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Run mode	Internal clock source	48M	7.49	7.52	7.53	7.53	6.08	6.14	6.18	6.20	mA
			24M	5.46	5.47	5.49	5.50	4.88	4.88	4.88	4.89	
			8M	2.16	2.19	2.22	2.26	1.36	1.37	1.39	1.42	
			4M	1.21	1.22	1.25	1.29	0.60	0.60	0.63	0.66	
			2M	0.82	0.83	0.87	0.91	0.51	0.52	0.55	0.60	
			1M	0.59	0.61	0.60	0.64	0.41	0.40	0.42	0.49	
			500K	0.45	0.45	0.47	0.51	0.36	0.37	0.39	0.42	
			125K	0.34	0.34	0.37	0.40	0.33	0.34	0.36	0.40	

Table 5-8 Typical current consumption in Low Power Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Low Power Run mode	HSISEL = 1, HSI1MHz	1M	324.7	330.7	336.3	341.3	265.1	271.6	277.6	281.4	uA
		HSISEL = 0, HSI8MHz	2M	695.1	706.9	725.3	738.3	577.7	581.3	607.0	616.7	
			1M	447.5	454.3	466.5	473.3	391.4	391.7	407.8	414.8	
			512K	316.9	326.6	339.2	346.8	288.9	293.8	310.8	317.6	
			256K	208.1	217.0	230.5	239.6	201.1	206.3	224.5	233.8	
			128K	189.0	197.5	210.4	219.0	185.5	190.4	207.6	216.2	
		LSISEL = 00, LSI40KHz	40K	46.79	52.77	61.81	70.22	45.37	50.73	59.18	67.50	
		LSISEL = 01, LSI10KHz	10K	40.98	42.78	49.78	57.75	40.60	42.24	49.17	57.04	

Table 5-9 Typical current consumption in Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}			48M	6.47	6.50	6.50	6.50	3.52	3.52	3.51	3.52	mA

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
	Supply current in Sleep mode	Internal clock source	24M	3.58	3.58	3.58	3.59	2.11	2.09	2.09	2.10	
			8M	1.14	1.15	1.17	1.21	0.64	0.65	0.68	0.71	
			4M	0.74	0.75	0.77	0.81	0.49	0.49	0.51	0.55	
			2M	0.58	0.59	0.63	0.67	0.45	0.46	0.49	0.53	
			1M	0.44	0.46	0.49	0.51	0.39	0.40	0.41	0.46	
			500K	0.38	0.38	0.41	0.44	0.35	0.35	0.37	0.41	
			125K	0.34	0.34	0.36	0.40	0.33	0.33	0.35	0.39	

Table 5-11 Typical and maximum current consumption in Stop mode (1)

Symbol	Parameter	Conditions	Typical				Maximum	Unit
			-40℃	25℃	85℃	105℃	25℃	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	39.02	32.77	37.59	65.48	50.00	μA
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	0.37	0.43	2.63	16.74	1.00	

1. The I/O state is an analog input.

Table 5-12 Typical and maximum current consumption in Standby modes (1)

Symbol	Parameter	Conditions	Typical				Maximum	Unit
			-40℃	25℃	85℃	105℃	25℃	
I_{DDx}	Supply current in Standby mode	LSI, LSE, RTC, IWDG all disabled	0.24	0.31	1.44	8.00	1.00	μA
		LSI40K and IWDG enabled	0.61	0.76	2.06	8.80	-	
		LSI40K and RTC enabled	0.68	0.85	2.13	8.84	-	
		LSI10K and IWDG enabled	0.36	0.46	1.72	8.45	-	
		LSI10K and RTC enabled	0.38	0.48	1.73	8.44	-	
		LSE and RTC enabled	0.72	0.84	2.12	8.86	-	

1. The I/O state is an analog input.

Table 5-13 Typical and maximum current consumption in Shutdown mode (1)

Symbol	Parameter	Conditions	Typical				Maximum	Unit
			-40℃	25℃	85℃	105℃	25℃	
I_{DDx}	Supply current in Shutdown mode	Enter Shutdown mode after reset, V_{DD}=3.3V	0.076	0.119	1.058	6.545	0.50	μA

1. The I/O state is an analog input.

Built-in peripheral current consumption

The current consumption of the built-in peripheral is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load) .
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 5-3.

Table 5-14 Built-in peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	GPIOA	AHB	1.98	uA/MHz
	GPIOB		2.02	
	GPIOC		2.01	
	GPIOD		1.79	
	GPIOH		1.56	
	CRC		2.13	
	DMA		3.37	
	TIM16	APB2	3.62	
	TIM17		3.69	
	SPI1		7.74	
	UART1		7.26	
	SYSCFG		0.31	
	MCUDBG		0.09	
	COMP		0.50	
	EXTI		2.69	
	ADC		5.79	
	LPTIM1		1.49	
	LPUART		0.64	
	UART1		7.26	
	TIM3	APB1	5.87	
	TIM4		5.91	
	UART2		7.86	
	IRM		0.12	
	RTC		1.15	
	Backup registers		1.11	
	SPI2		8.66	
	IWDG		1.10	

Symbol	Parameter	Bus	Typical	Unit
	I2C1		9.20	
	Segment LCD		2.34	
	WWDG		0.34	

1. f_{HCLK} = 48MHz, f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

- Stop or Standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering the Sleep mode. The time given in the table below is obtained under the ambient temperature and the supply voltage listed in Table 5-3.

Table 5-15 Wake up time from Low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSI	3.4	us
t_{WUSTOP}	Wake up from Stop mode (regulator is in Run mode)	System clock is HSI	15	us
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode (regulator is in low power mode)	System clock is HSI	20	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR6[2:0] = 0x0	132	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR6[2:0] = 0x1	77	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR6[2:0] = 0x2	85	us
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR6[2:0] = 0x3	93	us
t_{WUSHDN}	Wake up from Shutdown mode	-	1090	us

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured by a high speed external clock source, and the ambient temperature and power supply voltage meet the general operating conditions.

Table 5-16 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time(1)	-	15	-	-	ns

1. Guaranteed by design, not tested in production

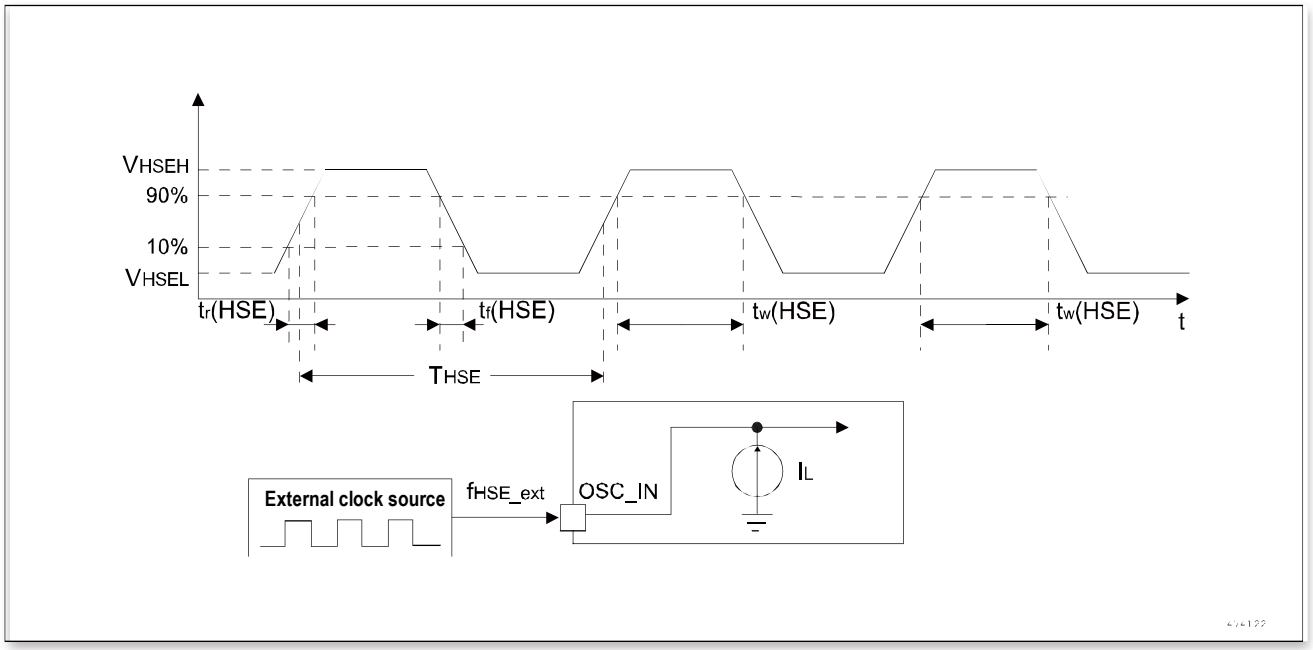

Figure 5-6 High-speed external clock source AC timing diagram

Low-speed external clock generated from an external source

The characteristic parameters given in the following table are measured by a low speed external clock source, and the ambient temperature and power supply voltage meet the general operating conditions.

Table 5-17 Low-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User external clock frequency (1)	-	-	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time (1)	-	250	-	-	ns

1. Guaranteed by design, not tested in production.

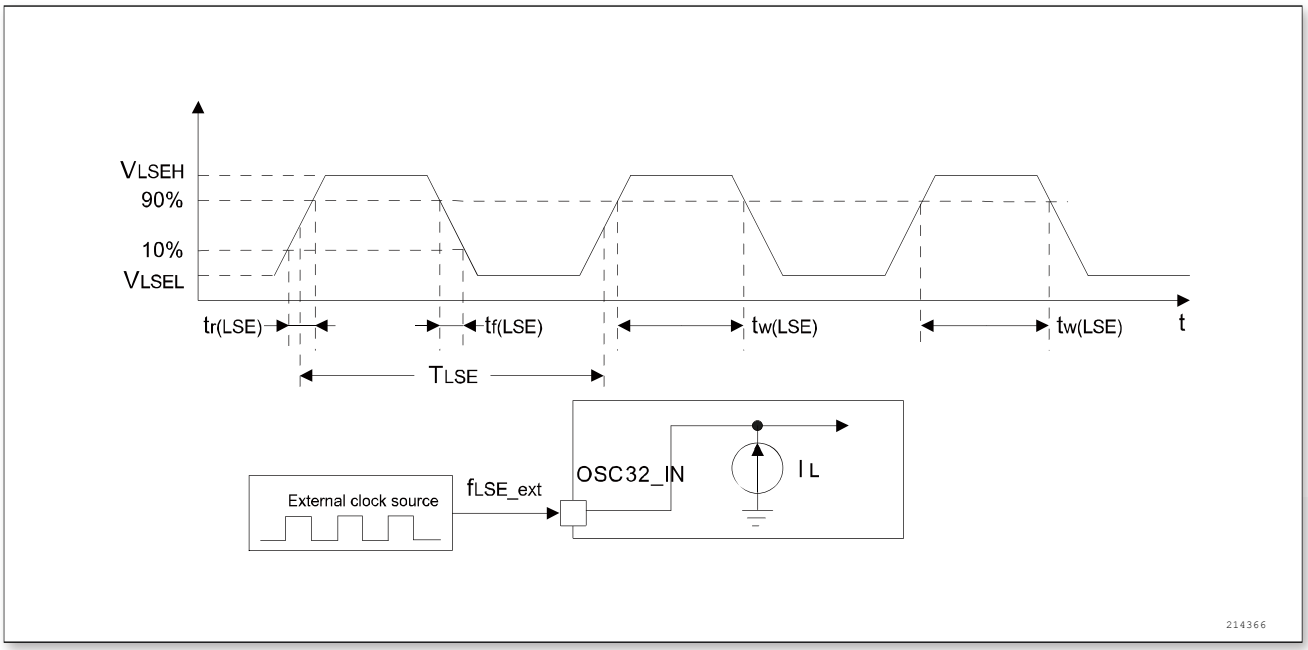

Figure 5-7 Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on the design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 5-18 HSE oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency (2)	1.8V<VDD<3.6V	4	8	12	MHz
		3.0V<VDD<5.5V	8	16	24	MHz
R_F	Feedback resistor (4)	-	-	1000	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2}(3) is 16pF)	f_{OSC_IN} =24M V_{DD}=3V	-	-	50	Ω
		f_{OSC_IN} =12M V_{DD}=2V	-	-	150	Ω
I_2	HSE current consumption	f_{OSC_IN} =24M ESR=30 V_{DD} = 3.3V，C_{L1} C_{L2}(3) is 20pF	-	0.8	-	mA
g_m	Oscillator transconductance	Start up	-	8	-	mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stable	-	7	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Drawn from comprehensive evaluation.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} have the same parameters. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the R_F resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment results in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
5. $t_{SU(HSE)}$ is the startup time measured from the time the HSE is enabled by software until a stable 8MHz oscillation is obtained. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

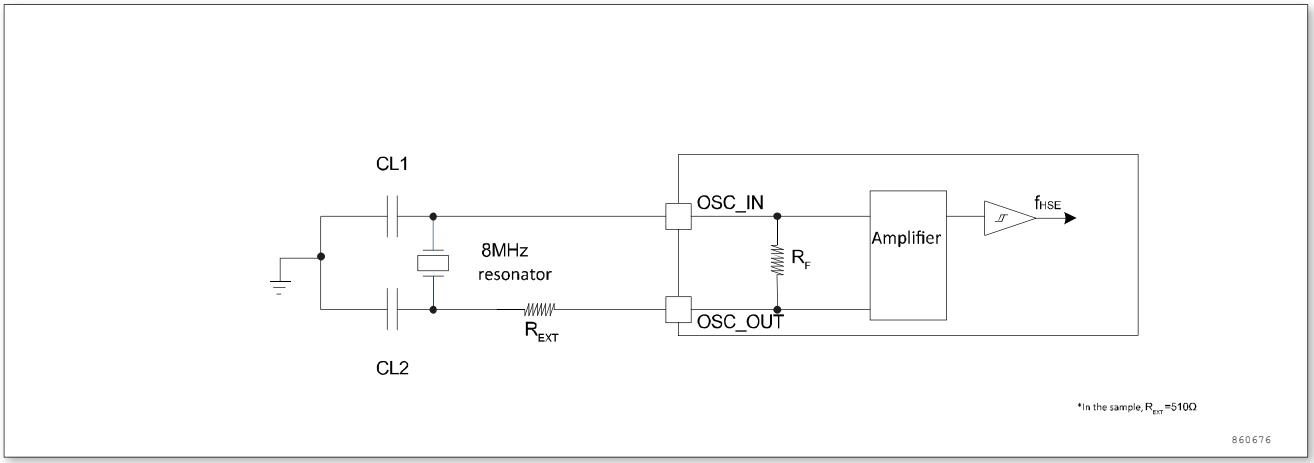

Figure 5-8 Typical application with an 8 MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768KHz crystal/ceramic resonator oscillator. All the information given in this section is based on the design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...). (Note: The crystal resonator mentioned is what we call crystal).

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 15 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The load capacitance is obtained from the formula below: $C_L = C_{L1} \times C_{L2}$ /

（C_{L1} + C_{L2}） + C_{stray}, in which C_{stray} is the capacitance of the pin and the PCB board or PCB related capacitance. Its typical value can be found in 2pF ~ 7pF.

Warning: To ensure that no value is greater than the maximum values of C_{L1} and C_{L2} (15pF), it is highly recommended to use a resonator with a load capacitance of $C_L \leq 7pF$, instead of a resonator with a load capacitance of 12.5pF. For example, if a resonator with a load capacitance of C_L = 6pF and C_{stray} = 2pF is selected, then C_{L1} = C_{L2} = 8pF.

Table 5-19 LSE oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency	2.0V<V_{DD}<5.5V	-	32.768	-	KHz
$I_{DD(LSE)}$ (2)	LSE current consumption	IBSEL=01 DR=00(recommend)	-	200	-	nA
		IBSEL=10 DR=01(Default)	-	300	-	nA
g_m	Oscillator transconductance	IBSEL=01 DR=00	-	2.8	-	uA/V
		IBSEL=10 DR=01	-	6.9	-	uA/V
$t_{SU(LSE)}$ (3)	Startup time	V_{DD} is stablized	-	1	3	s

1. Drawn from comprehensive evaluation.
2. A high-quality oscillator with small RS value (e.g., MSIVTIN 32.768KHz) can be selected to optimize current consumption. For details, please consult the crystal manufacturer.
3. $t_{SU(HSE)}$ is the startup time measured from the time the LSE is enabled by software until a stable 32.768KHz oscillation is obtained. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

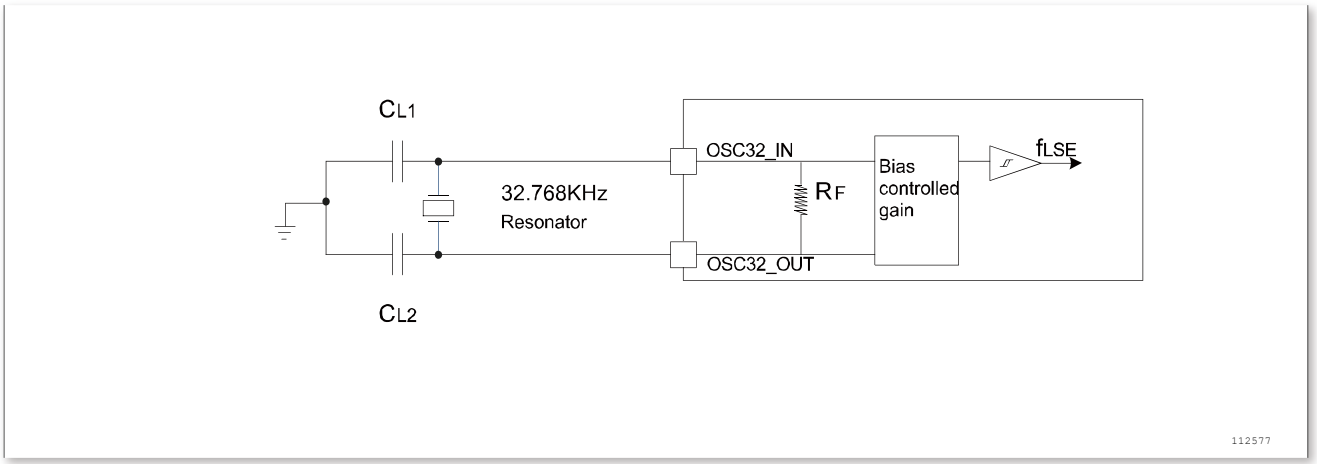

Figure 5-9 Typical application with a 32.768KHz crystal

5.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 5-20 HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI} (2)	Frequency	-	-	8	-	MHz
ACC_{HSI} (2)	HSI oscillator deviation	T_A = 0°C ~ 55°C	-1	-	+1	%
		T_A = -40°C ~ 85°C	-2.5	-	+2.5	%
$T_{stab(HSI)}$ (3)	HSI oscillator startup time	-	-	-	20	us
$I_{DD(HSI)}$ (3)	HSI oscillator power consumption	-	-	99	-	μA

1. V_{DD} = 3.3V, TA = -40℃~ 85℃, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 5-21 LSI 16KHz oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI} (2)	Frequency	-	-	16.384	-	KHz
ACC_{LSI} (2)	LSI oscillator deviation	T_A = 0°C ~ 55°C	-2	-	+2	%
		T_A = 0°C ~ 85°C	-5	-	+2	%
		T_A = -40°C ~ 0°C	-4	-	+6	%
$t_{SU(LSI)}$ (3)	LSI oscillator startup time	-	-	1	-	us
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	-	1.1	-	μA

1. V_{DD} = 3.3V, T_A = -40℃~ 85℃, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

Table 5-22 LSI 10KHz oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI} (2)	Frequency	-	-	10	-	KHz
ACC_{LSI} (2)	LSI oscillator deviation	T_A = -40°C~ 85°C	-50	-	+50	%
		T_A = 25°C	-10	-	+10	%
$t_{SU(LSI)}$ (3)	LSI oscillator startup time	-	-	-	1	ms
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	-	48	-	nA

1. V_{DD} = 3.3V, T_A = -40℃~ 85℃, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

Table 5-23 LSI 40KHz oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI} (2)	Frequency	-	-	40	-	KHz
ACC_{LSI} (2)	LSI oscillator deviation	T_A = -40°C~ 85°C	-50	-	+50	%
		T_A = 25°C	-10	-	+10	%
$t_{SU(LSI)}$ (3)	LSI oscillator startup time	-	-	-	600	us
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	-	62	-	nA

1. V_{DD} = 3.3V，T_A = -40℃~ 85℃, unless otherwise specified.
2. Drawn from comprehensive evaluation.
3. Guaranteed by design, not tested in production.

5.3.8 PLL characteristics

The relationship between the input clock f_{PLL_IN} and output clock f_{PLL_OUT} is:

Formula 1

$$\frac{f_{PLL\_IN}}{\mathrm{PLLDIV}[2:0]+1} = \frac{f_{PLL\_OUT}}{\mathrm{PLLMUL}[6:0]+1}$$

PLLMUL[6:0] and PLLDIV[2:0] are the frequency division ratio settings of the PLL frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general operating conditions.

Table 5-24 PLL characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL input clock (2)	-	4	8	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	20	-	80	%
f_{vco}	VCO output clock	-	80	-	200	MHz
f_{PLL_OUT}	PLL output clock	-	40	-	100	MHz
$I_{DD(PLL)}$	PLL current consumption	-	-	1500	-	uA

1. Guaranteed by design, not tested in production.
2. Use the correct multiplication factor to ensure the f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

5.3.9 Memory characteristics

Table 5-25 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	29.49	30.99	32.49	us

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ERASE}	Page (1024 bytes) erase time	-	8.11	9.11	10.11	ms
t_{ME}	Mass erase time	-	30.2	35.2	40.2	ms
I_{DD}	Supply current	Read mode 33MHz	-	2.5	3.5	mA
		Write mode	-	-	3.5	mA
		Erase mode	-	-	2	mA

Table 5-26 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = -40°C~ 85°C	20000	-	-	Cycles
T_{DR}	Data retention	T_A = 85℃	20	-	-	Years
		T_A = 25℃	100	-	-	

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by one electromagnetic event until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient Voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 5-27 EMS characteristics

Symbol	Parameter	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	V_{DD} = 3.3V， T_A = +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software. Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for this application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (e.g., control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.11 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU), the device is stressed to determine its performance in terms of electrical sensitivity, with the use of specific measurement methods.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JEDEC JS-001-2017/002-2018 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin. This test is compliant with EIA/JESD78E IC latch-up standard.

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 5-28 ESD & LU characteristics

Symbol	Parameter	Conditions	Class	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	C3	±1000	V
I_{LU}	Latch-up current	T_A = 85°C, conforming to JESD78E	II, A	±100	mA

5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below were measured according to the conditions in Table 5-3. All I/O ports are CMOS compatible.

Table 5-29 I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	3.3V	-	-	0.8	V
V_{IL}	Low level input voltage	5V	-	-	0.3*V_{DD}	V
V_{IH}	High level input voltage	3.3V	2.0	-	-	V
V_{IH}	High level input voltage	5V	0.7*V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	3.3V		0.1*V_{DD}		V
V_{hy}	Schmitt trigger hysteresis (1)	5V		0.1*V_{DD}		V
I_{lkg}	Input leakage current (2)	3.3V	-	0.1		μA
I_{lkg}	Input leakage current (2)	5V	-	0.1		μA
R_{PU}	Weak pull-up equivalent resistor (3)	3.3V V_{IN} = V_{SS}	29.24	50.26	79.18	kΩ
R_{PU}	Weak pull-up equivalent resistor (3)	5V V_{IN} = V_{SS}	29.24	50.26	79.18	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	3.3V V_{IN} = V_{DD}	27.46	48.62	77.56	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	5V V_{IN} = V_{SS}	27.46	48.62	77.56	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value
3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/output) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum rating given in Table 5-1:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating

current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.

- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 5-3. All I/O ports are CMOS compatible.

Table 5-30 Output voltage characteristics

SPEED[1:0]	Symbol	Parameter	Conditions	Typical	Unit
11	V_{OL}(1)(4)	Output low voltage	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.1	V
	V_{OH}(2)(4)	Output high voltage		2.9	
	V_{OL}(1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.15	
	V_{OH}(2)(3)	Output high voltage		2.8	
	V_{OL}(1)(3)	Output low voltage	$\|I_{IO}\|$=20mA, VDD=3.3V	0.3	
	V_{OH}(2)(3)	Output high voltage		2.0	
10	V_{OL}(1)(4)	Output low voltage	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.1	
	V_{OH}(2)(4)	Output high voltage		2.9	
	V_{OL}(1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.15	
	V_{OH}(2)(3)	Output high voltage		2.8	
	V_{OL}(1)(3)	Output low voltage	$\|I_{IO}\|$=20mA, VDD=3.3V	0.3	
	V_{OH}(2)(3)	Output high voltage		2.0	
01	V_{OL}(1)(4)	Output low voltage	$\|I_{IO}\|$= 6mA, VDD=3.3V	0.1	
	V_{OH}(2)(4)	Output high voltage		2.9	
	V_{OL}(1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA, VDD=3.3V	0.15	
	V_{OH}(2)(3)	Output high voltage		2.8	
	V_{OL}(1)(3)	Output low voltage	$\|I_{IO}\|$=20mA, VDD=3.3V	0.3	
	V_{OH}(2)(3)	Output high voltage		2.0	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.
3. Drawn from comprehensive evaluation.
4. Guaranteed by design, not tested in production.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise specified, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the conditions in Table 5-3.

Table 5-31 I/O AC characteristics (1)(2)(3)

SPEED[1:0]	Symbol	Parameter	Conditions	Typical	Unit
11	$t_{f(IO)out}$	Output fall time	C_L = 50pF V_{DD}=3.3V	10.5	ns
	$t_{r(IO)out}$	Output rise time		16.5	ns
10	$t_{f(IO)out}$	Output fall time		7.2	ns
	$t_{r(IO)out}$	Output rise time		11.3	ns
01	$t_{f(IO)out}$	Output fall time		3.7	ns
	$t_{r(IO)out}$	Output rise time		6.8	ns

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this chip user manual.
2. The maximum frequency is defined in Figure 5-10.
3. Guaranteed by design, not tested in production

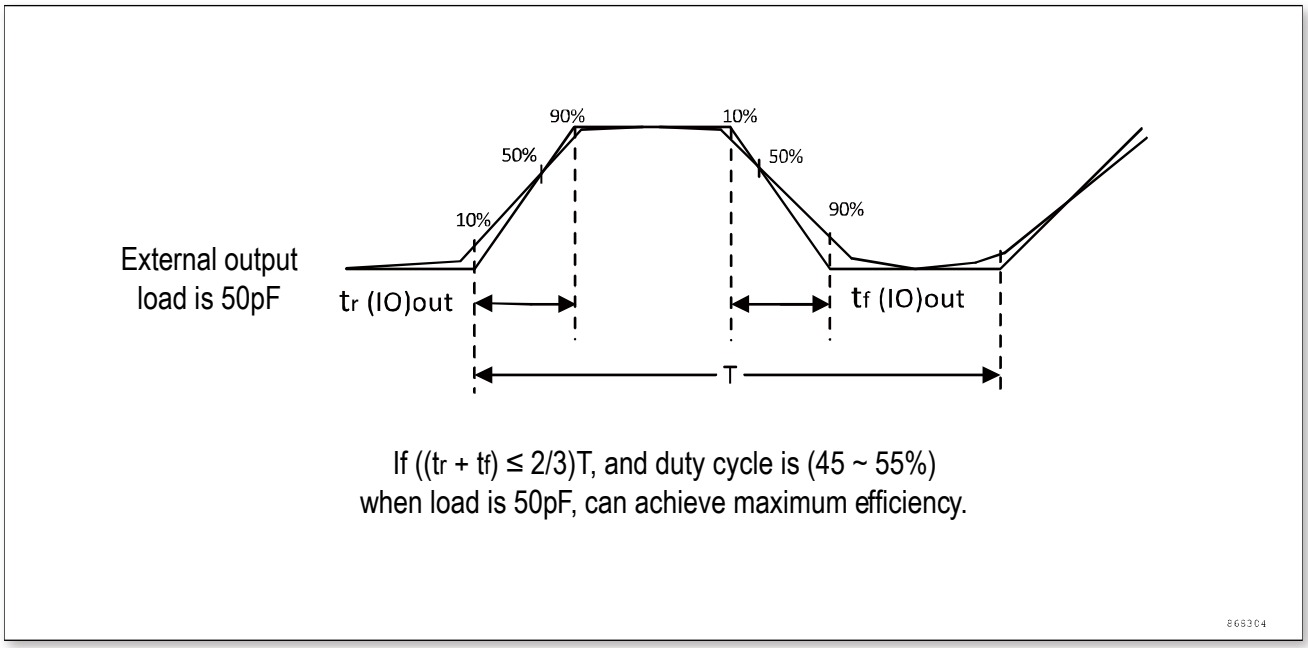

Figure 5-10 I/O AC characteristics

5.3.13 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters listed in the table below are measured under the ambient temperature and V_{DD} supply voltage in accordance with the condition summarized in Table 5-3.

Table 5-32 NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$ (1)	NRST input low voltage	V_{DD}=3.3V	-	-	0.8	V
$V_{IH(NRST)}$ (1)	NRST input high voltage	V_{DD}=3.3V	2.0	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD}=3.3V		0.1*VDD		V
R_{PU}	Weak pull-up equivalent resistor (2)	V_{IN} = V_{SS}	29.24	50.26	79.18	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	-	-	-	0.5	us
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse	-	4.0	-	-	us

1. Guaranteed by design, not tested in production.
2. The pull-up and pull-down resistors are MOS resistors.

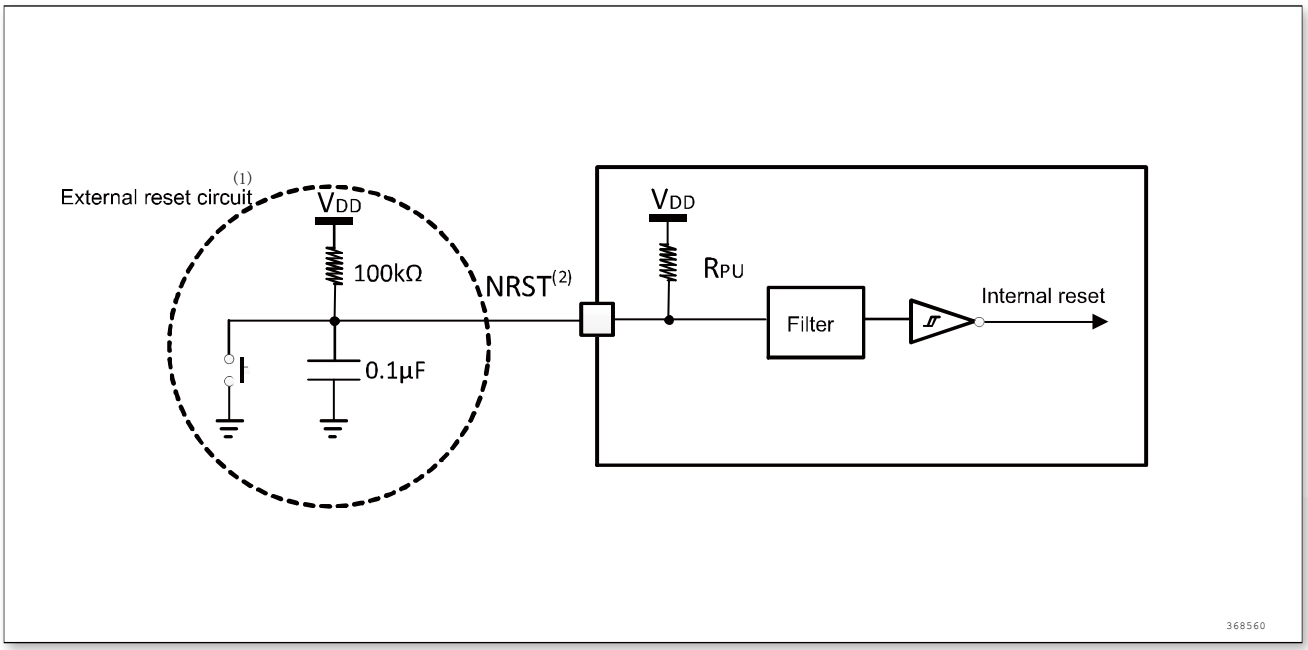

Figure 5-11 Recommended NRST pin protection

1. The reset network is to prevent parasitic reset.
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 5-32 , otherwise the MCU cannot be reset.

5.3.14 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), refer to section 5.3.12 I/O .

Table 5-33 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.9	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365.3	us
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjus 表)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	89.4	s
t_{MAX_IN}	TIM maximum input frequency	-	-	48	MHz

1. Guaranteed by design, not tested in production.

5.3.15 I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and VDD supply voltage conditions summarized in Table 5-3.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and VDD is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 5.3.12 I/O for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 5-34 I2C interface characteristics

Symbol	Parameter	Standard I2C(1)		Fast mode I2C(1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	9*t_{PCLK}	-	9*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	18*t_{PCLK}	-	18*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA setup time	1*t_{PCLK}	-	1*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (3)	- (4)	0 (3)	- (4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20×(V_{DD}/ 5.5V)	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us

Symbol	Parameter	Standard I2C(1)		Fast mode I2C(1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	$8*t_{PCLK} – 1$ (4)	-	$8*t_{PCLK}$ - 0.3 (4)	us
$t_{h(STA)}$	Start condition hold time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	us
$t_{su(STA)}$	Start condition setup time	$19*t_{PCLK}$	-	$17*t_{PCLK}$	-	us
$t_{su(STO)}$	Stop condition setup time	$17*t_{PCLK}$	-	$17*t_{PCLK}$	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	$484*t_{PCLK}$	-	$144*t_{PCLK}$	-	us
C_b	Capacitive load of each bus	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be greater than 3MHz to achieve standard mode I2C frequencies. It must be greater than 12MHz to achieve fast mode I2C frequencies.
3. Ensure SCL drops below $0.3V_{DD}$ on falling edge before SDA crosses into the indeterminate range of $0.3V_{DD}$ to $0.7V_{DD}$.

NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to $0.3V_{DD}$ should be used to insert a delay of the SDA transition with respect to SCL.

4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
6. $t_{vd(ACK)}$ = time for acknowledgement signal from SCL LOW to SDA output.

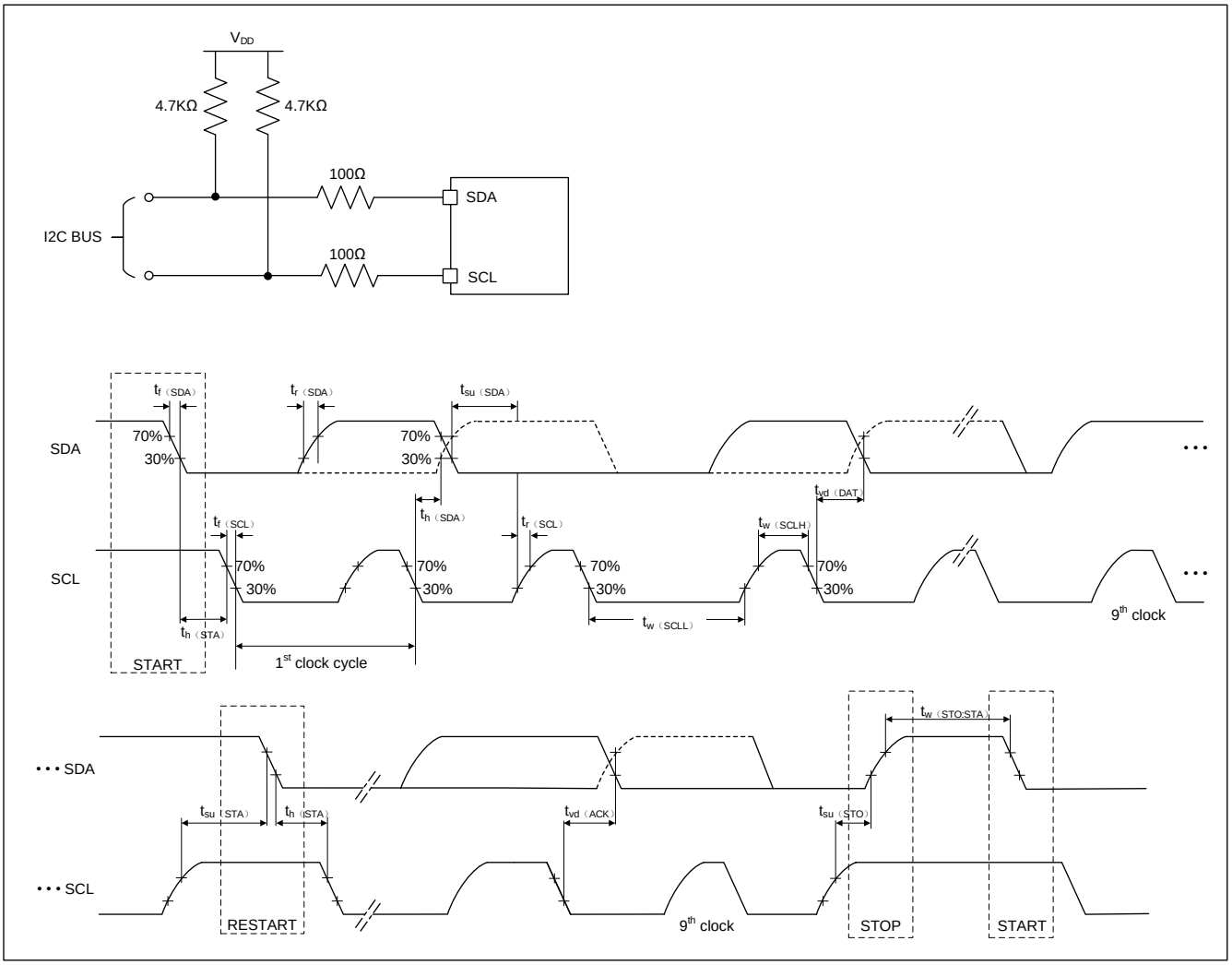

Figure 5-12 I2C bus AC waveform and measurement circuit (1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

5.3.16 SPI interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 5-3.

Refer to section 5.3.12 I/O for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 5-35 SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$)	SPI clock frequency	Master mode	-	18	24	MHz
		Slave mode	-	9	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	-	6	ns

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$t_{c(SCK)}/2$	-	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$t_{c(SCK)}/2$	-	-	ns
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)}/2-6$	-	$t_{c(SCK)}/2+6$	ns
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)}/2-6$	-	$t_{c(SCK)}/2+6$	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	$38-N*t_{c(SCK)}/2$ (2)	-	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	$N*t_{c(SCK)}/2-10$ (2)	-	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	-	16	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	$25-N*t_{c(PCLK)}$ (3)	$32-N*t_{c(PCLK)}$ (3)	$48-N*t_{c(PCLK)}$ (3)	ns
$t_{h(MO)}$ (1)	Data output hold time	Master mode (after enable edge)	-2	-	-	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	$10-N*t_{c(PCLK)}$ (3)	-	-	

1. Drawn from comprehensive evaluation.
2. The sampling point of the received data can be adjusted, when the host is in the high-speed mode. Adjustment can be made to $t_{su(MI)}$ by configuring the control bit RXEDGE of the register CCTL in order to optimize the timing margin, where the N value is shown below:

   If RXEDGE=1, then N=0; if RXEDGE=1, then N=（f_{PCLK}/f_{SCK}）/2;
3. The control bit TXEDGE of the CCTL register can be configured to make the early release of slave output SO to the pin possible (without waiting for the input clock SCK edge) in order to optimiza the timing margin, where the N value is shown below:

   If TXEDGE=0, then N=0; if TXEDGE=1, then

   When $7<=f_{PCLK}/f_{SCK}<8$, N=3;

   When $6<=f_{PCLK}/f_{SCK}<7$, N=2;

   When $5<=f_{PCLK}/f_{SCK}<6$, N=1;

   When $4<=f_{PCLK}/f_{SCK}<5$, N=0.

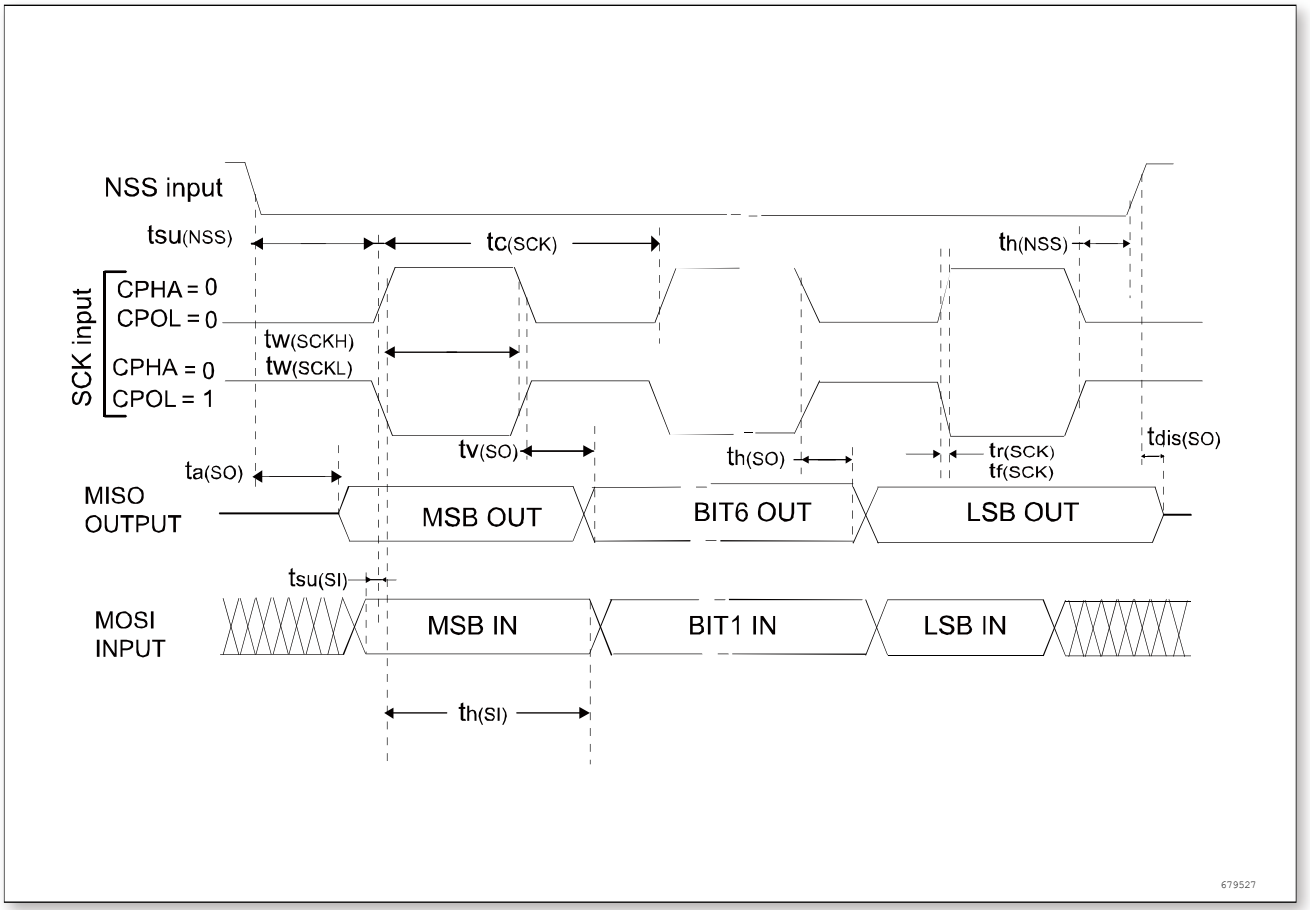

Figure 5-13 SPI timing diagram slave mode and CPHA = 0, CPHASEL = 1

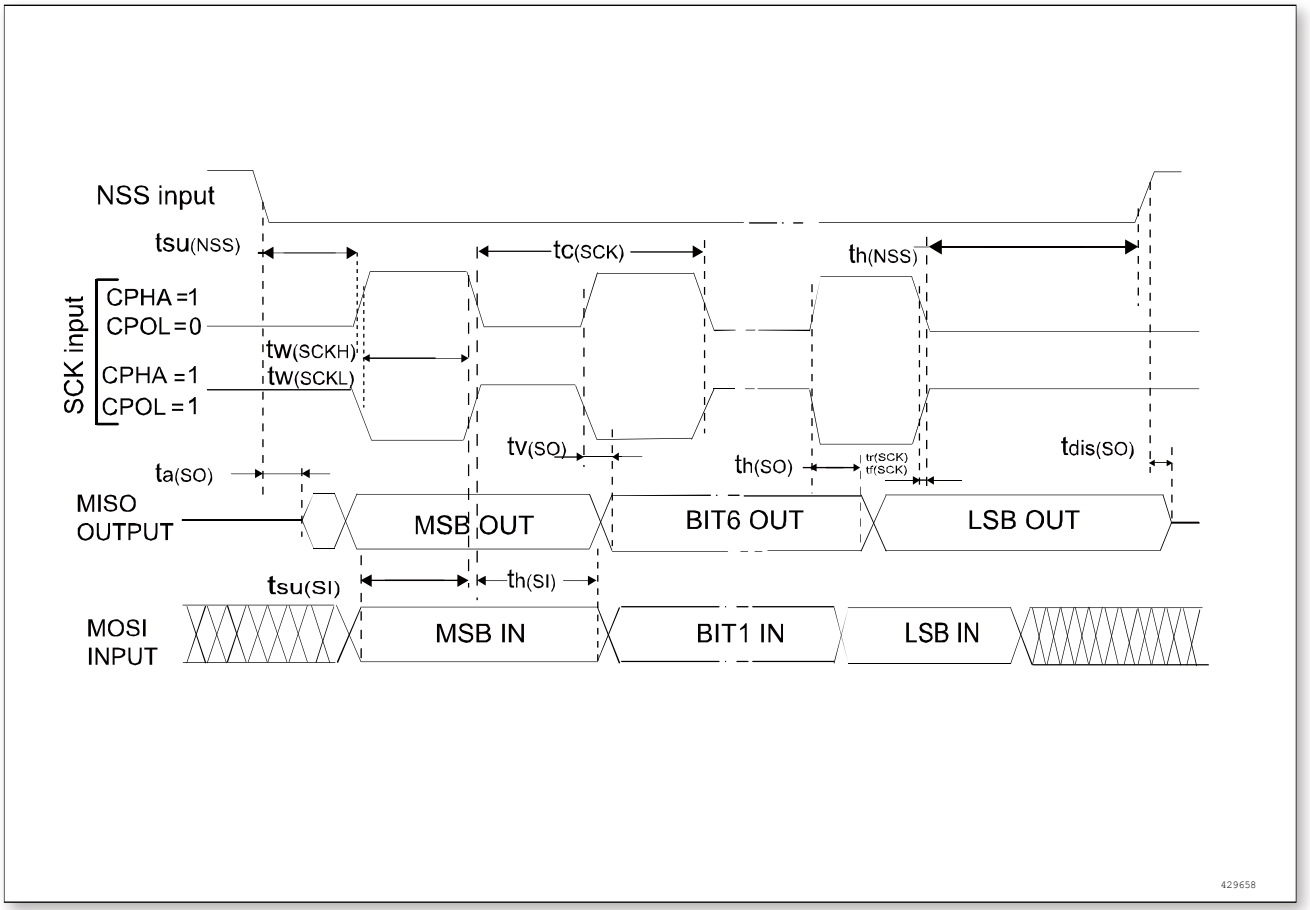

Figure 5-14 SPI timing diagram slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ 和 $0.7V_{DD}$。

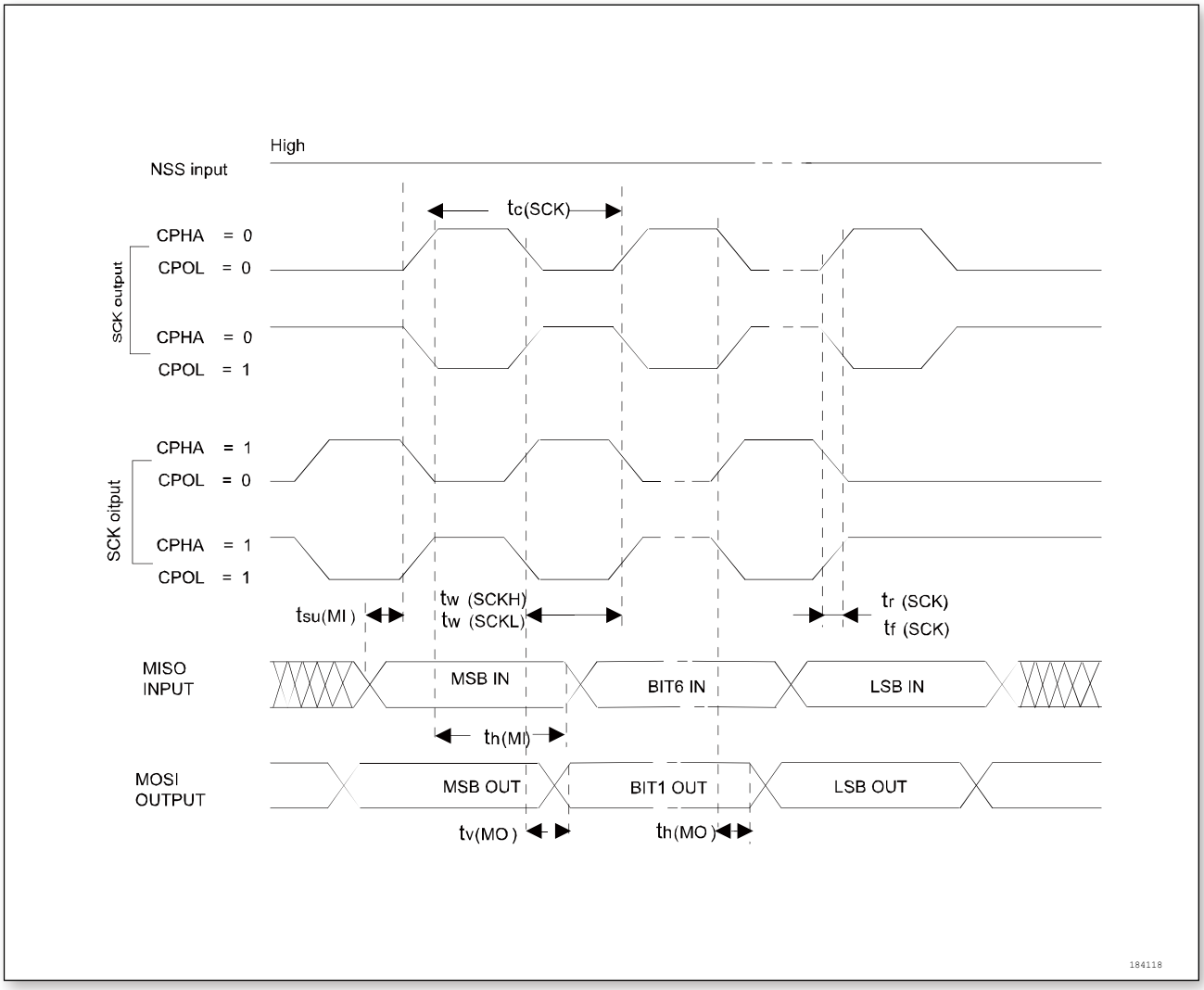

Figure 5-15 SPI timing diagram master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ 和 $0.7V_{DD}$。

5.3.17 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 5-3.

Table 5-36 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S(1)	Sampling frequency	-	-	-	1	MHz
f_{TRIG}(1)		f_{ADC} = 16MHz	-	-	1	MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	External trigger frequency (3)	-	-	-	16	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	See equation 2			kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC}(1)	Internal sample and hold capacitance	-	-	-	10	pF
t_{STAB}(1)	Stabilization time	-	-	-	10	us
t_{latr}(1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	us
			2.5	-	240.5	$1/f_{ADC}$
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	us
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	11	-	bit

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product, V_{REF+} is internally connected to V_{DDA}, V_{REF-} is internally connected to V_{SSA}.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of $1/f_{ADC}$ must be added.

Input impedance

Formula 2

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above (Formula 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 5-37 Maximum R_{AIN} at f_{ADC}=15MHz(1)

TS (cycles)	tS (us)	Maximum RAIN (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2

TS (cycles)	tS (us)	Maximum RAIN (kΩ)
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

Table 5-38 ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-3.5/+3.5	LSB
EO	Offset error		-2.5/+2.5	
EG	Gain error		-1/+2	
ED	Differential linearity error		-0.8/+1.5	
EL	Integral linearity error		-2.5/+2.5	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the range specified for $I_{INJ(PIN)}$ and $\Sigma_{IINJ(PIN)}$ in section 5.2 Absolute maximum rating does not affect the ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 5-16.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

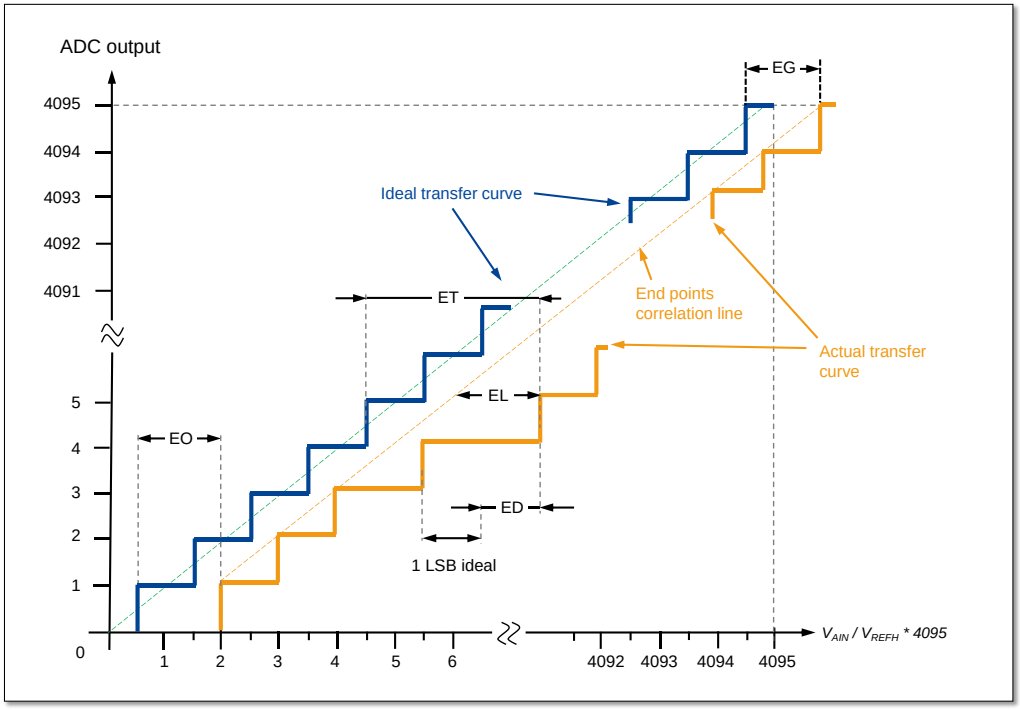

Figure 5-16 Schematic diagram of ADC static parameters

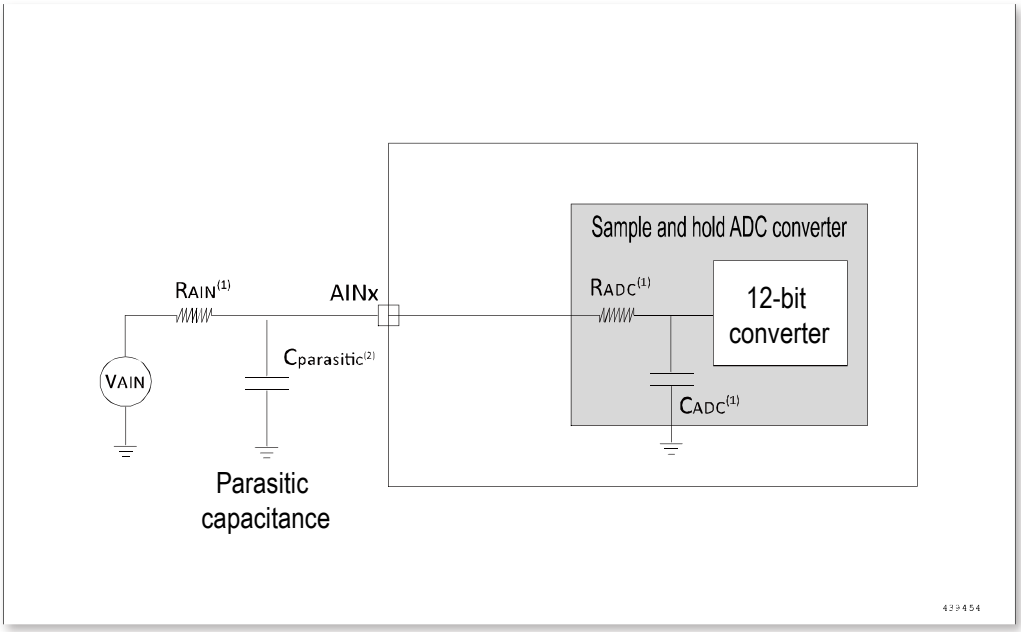

Figure 5-17 Typical connection diagram using the ADC

1. Refer to Table 5-36 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The decoupling of power supply must be connected as shown below. The 10nF capacitor

in the figure must be ceramic, and it should be as close as possible to the MCU chip.

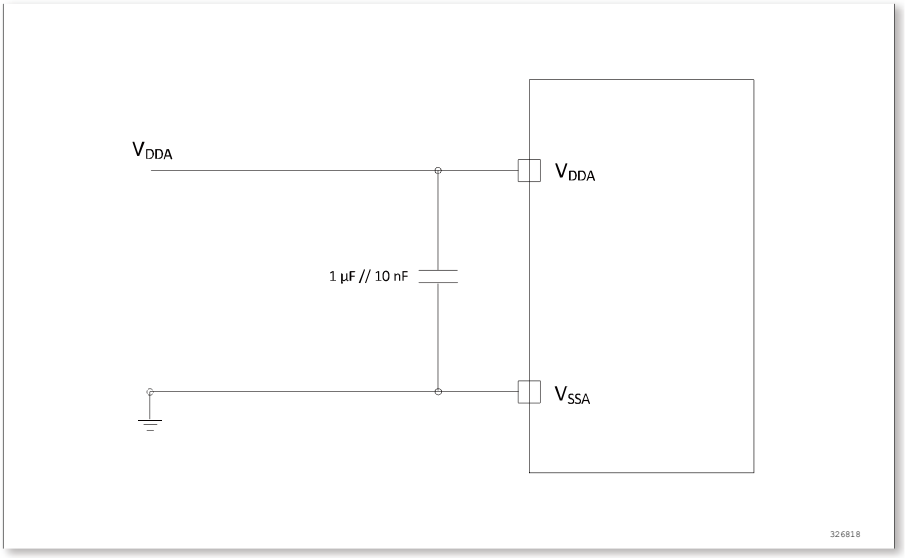

Figure 5-18 Power supply and reference power supply decoupling circuit

5.3.18 Temperature sensor characteristics

The temperature sensor is calculated with the following equation:

Temperature equation

$$TS_{adc} = 25 + \frac{Value * V_{DDA} - offset * 3300}{4096 * Avg\_Slope}$$

V_{DDA}: The V_{DDA} voltage from the current sampling of ADC, and the unit is mV.

Offset: The conversion result obtained at 25°C, is stored in Flash space 0x1FFFF7E6, where the typical voltage values at 25°C and 3.3V can be referenced to V_{25} in Table 5-39.

Value: The conversion result from the current sampling of ADC.

Avg_Slope: The average slope (expressed in mV/°C) of the temperature and voltage curve. For the typical values, refer to Table 5-39.

Table 5-39 Temperature sensor characteristics (3)(4)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature	-	±10	-	°C
Avg_Slope (1)	Average slope	-	-3.67	-	mV/°C
V_{25} (1)	Voltage at 25℃	1.10	1.260	1.50	V
t_{START} (2)	Setup time	-	-	10	us
t_{S_temp} (2)	ADC sampling time when reading temperature	-	11.8	-	us

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by application through multiple circulations.

4. V_{DD} = 3.3V.

5.3.19 Comparator characteristics

Table 5-40 Comparator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
V_{HYST}	Hysteresis	HYST = 00, MODE = 1	-	0	-	mV
		HYST = 01, MODE = 1	12.99	23.01	32.99	
		HYST = 10, MODE = 1	25	36.99	44.99	
		HYST = 11, MODE =1	76.97	104.91	123	
		HYST = 00, MODE =0	-	0	-	
		HYST = 01, MODE =0	10.97	20.97	30.96	
		HYST = 10, MODE =0	19.26	30.65	41.6	
		HYST = 11, MODE =0	90.98	128.9	180.94	
V_{OFFSET}	Offset voltage	MODE = 1	-	±13.0	±14.87	mV
		MODE = 0	-	±13.0	±15.31	
t_{DELAY}	Propagation delay	HYST = 0, MODE = 1	142.6	278.9	425.9	ns
		HYST = 0, MODE = 0	25.19	47.6	66.84	
I_q	Average working current	MODE = 1, $V_{INP} > V_{INM}$	0.271	0.409	0.861	uA
		MODE = 1, $V_{INP} < V_{INM}$	0.437	0.675	1.394	
		MODE = 0, $V_{INP} > V_{INM}$	1.292	2.05	3.55	
		MODE = 0, $V_{INP} < V_{INM}$	2.535	4.05	7.283	

5.3.20 Segment LCD characteristics

Table 5-41 Segment LCD characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{LCD}	Supply voltage of LCD controller	-	1.8	-	5.5	V
C_{LCDCAP}	LCD external capacitance	Only for charge pump is enabled	cc	0.1	-	uF
C_{V4}	LCD V4 pin external capacitance	Only for 1/4 bias mode	-	0.1	-	uF
C_{V3}	LCD V3 pin external capacitance	Only for 1/4 or 1/3 bias mode	-	0.1	-	uF
C_{V2}	LCD V2 pin external capacitance	Only for 1/4, 1/3 or 1/2 bias mode	-	0.1	-	uF
C_{V1}	LCD V1 pin external capacitance	Only for 1/4, 1/3 or 1/2 bias mode	-	0.1	-	uF
C_G	External glass capacitance	-	-	-	8	nF
f_{FR}	LCD frame frequency	-	10	-	100	Hz
V_{LCDCP}	Charge pump output voltage supplied to LCD controller (bias mode 1 - charge pump boost)	CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 0	-	2.64	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 1	-	2.76	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 2	-	2.88	-	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 3	-	3.00	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 4	-	3.12	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 5	-	3.24	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 6	-	3.36	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 7	-	3.48	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 8	-	3.96	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 9	-	4.14	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 10	-	4.32	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 11	-	4.50	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 12	-	4.68	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 13	-	4.86	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 14	-	5.04	-	V
		CPMODE = 10, REFEN = 1, VDDEN = 0, CC = 15	-	5.22	-	V
I_{LCD} (1)	LCD current consumption	LCD clock provided by LSE, 4 x COM, 1/3 bias, 32Hz frame frequency, all segments on	-	0.49	-	uA
		LCD clock provided by LSE, 8 x COM, 1/4 bias, 32Hz frame frequency, all segments on	-	0.50	-	uA
		LCD clock provided by LSI10K, 4 x COM, 1/3 bias, 32Hz frame frequency, all segments on	-	0.22	-	uA
		LCD clock provided by LSI10K, 8 x COM, 1/4 bias, 32Hz frame frequency, all segments on	-	0.21	-	uA
I_{LCDLP} (1)	LCD low power mode current consumption	LCD clock provided by LSE, 4 x COM, 1/3 bias, 32Hz frame frequency, all segments on, low power mode	-	0.49	-	uA
		LCD clock provided by LSE, 8 x COM, 1/4 bias, 32Hz frame frequency, all segments on, low power mode	-	0.50	-	uA
		LCD clock provided by LSI10K, 4 x COM, 1/3 bias, 32Hz frame frequency, all segments on, low power mode	-	0.22	-	uA
		LCD clock provided by LSI10K, 8 x COM, 1/4 bias, 32Hz frame frequency, all segments on, low power mode	-	0.21	-	uA

1. The LCD screen is not connected during the test. Because the current consumption of different LCD models may differ a lot, it's recommended that users test the current consumption for their

own LCD screens.

6 Package dimensions

6.1 LQFP64

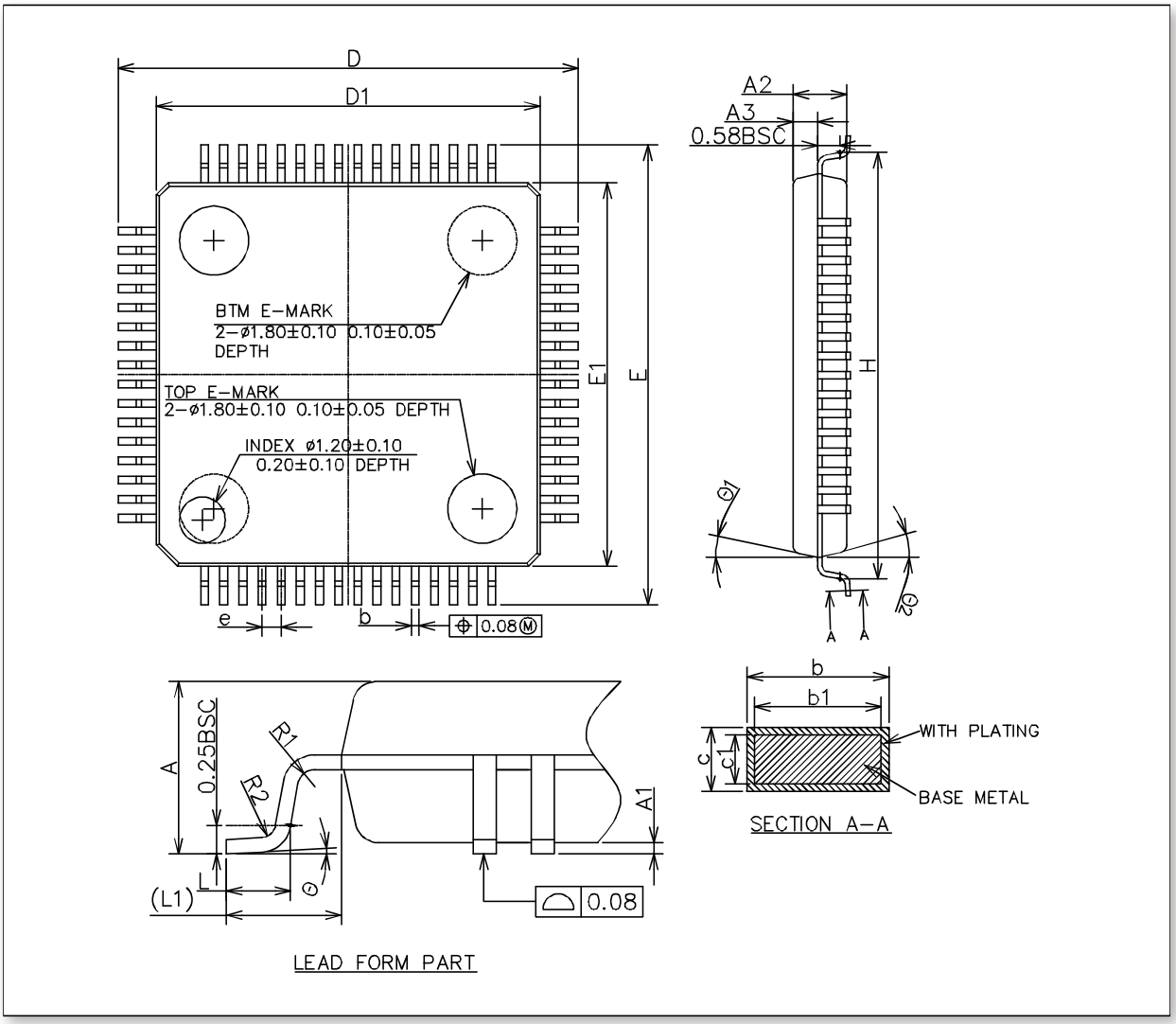

Figure 6-1 LQFP64, 64-pin quad flat no-lead package outline

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

Package dimensions

Table 6-1 LQFP64 package dimension details

ID	Milimeter		
	Minimum	Typical	Maximum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	-	0.50	-
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

6.2 LQFP48

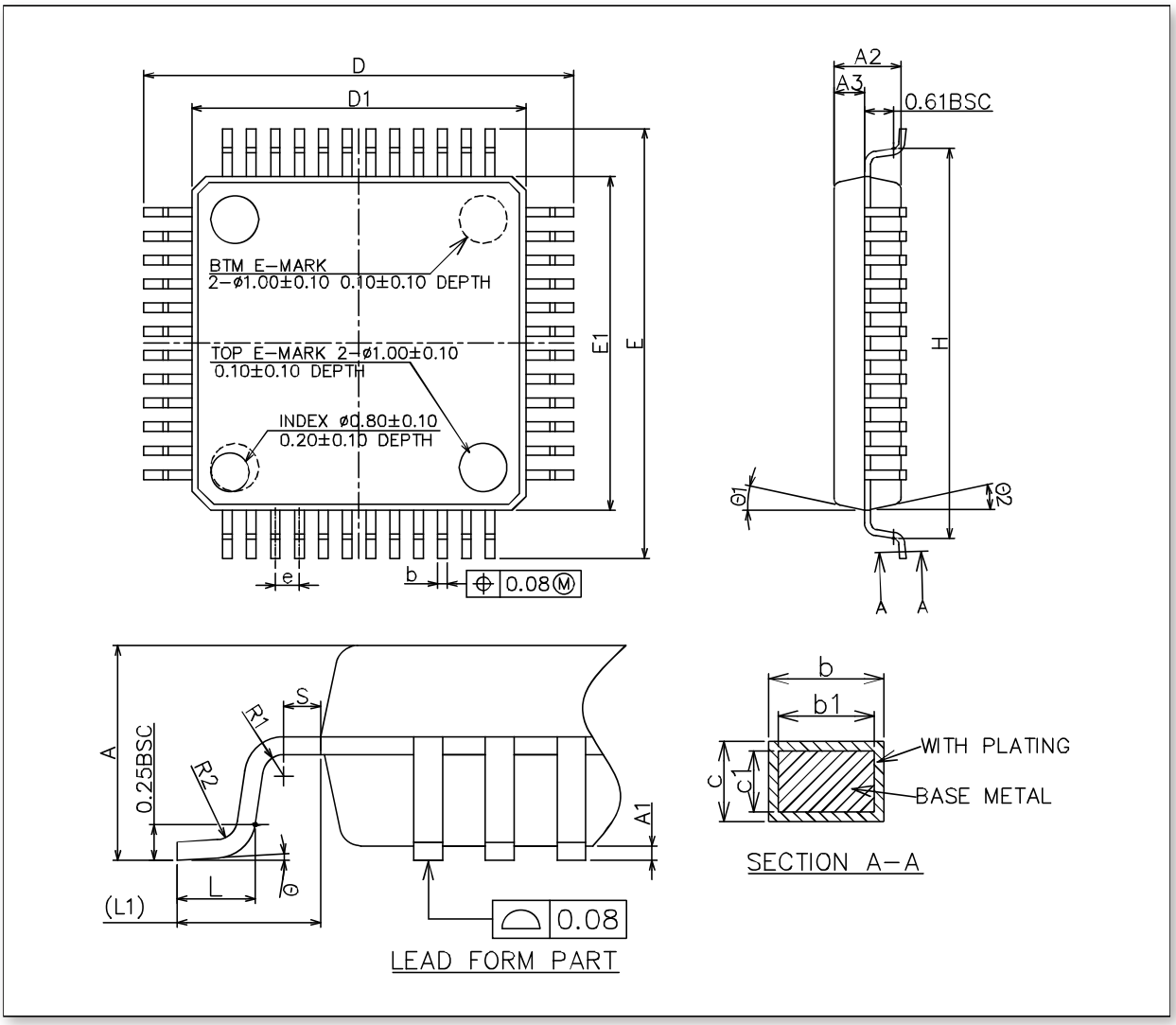

Figure 6-2 LQFP48, 48-pin quad flat no-lead package outline

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

Table 6-2 LQFP48 package dimension details

ID	Milimeter		
	Minimum	Typical value	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	-	0.50	-
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

7 Revision history

Table 7-1 Revision history

Date	Version	Content
2024.09.20	Rev1.0	Upgraded to Rev1.0
2022/12/18	Rev0.91	1. Updated the layout of Ordering table 2. Added deviation data over multiple temperature ranges in HSI oscillator characteristics (1) 3. Added deviation data over multiple temperature ranges in LSI 16KHz oscillator characteristics (1) 4. Extended the temperature range in Flash memory endurance and data retention 5. Added class level to ESD & LU characteristics
2022/10/18	Rev0.9	1. Added current consumption for LCD module to Segment LCD characteristics 2. Added ESD and LU data to ESD & LU characteristics 3. Added current consumption data to Typical current consumption in Low Power Run mode 4. Updated note number in LSE oscillator characteristics (1) 5. Added temperature condition to Flash memory endurance and data retention 6. Added limit value at room temperature to Typical and maximum current consumption in Stop mode (1), Typical and maximum current consumption in Standby modes (1), Typical and maximum current consumption in Shutdown mode (1) 7. Added limit value to Comparator characteristics 8. Added limit value at room temperature to Built-in voltage reference 9. Added V25 limit value at room temperature to Temperature sensor characteristics (3)(4) 10. Added L0136B and L0131B models to Ordering table
2022/4/6	Rev0.5	First public release