Product Brief

MM32L0130

Arm® Cortex®-M0+ based 32-bit Microcontrollers

Revision: 1.0

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1 Introduction

1.1 Overview

The MM32L0130 microcontrollers are based on Arm® Cortex®-M0+ core. These devices have a maximum clocked frequency of 48MHz, built-in 64KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one analog comparator, two 16-bit general purpose timers, two 16-bit basic timers, one low power timer and one RTC, as well as communication interfaces including two UART, one low power UART, two SPI or I2S and one I2C.

The operating voltage of this product series is 1.8V to 5.5V, and the operating temperature range (ambient temperature) is -40°C to 85°C. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

- Air-conditioner remote controllers
- Thermostat
- Ear and forehead thermometers
- Portable medical equipment
- Gas, water, heat meters
- Small appliances

This product series is available in LQFP64 and LQFP48 packages.

1.2 Key features

- Core and system
  - 32-bit Arm® Cortex®-M0+
  - Frequency up to 48MHz
- Memory
  - Up to 64KB embedded Flash storage
  - Up to 8KB SRAM
  - Embedded Bootloader to support In-System-Programming (ISP)
- Clock, reset and power management
  - Power supply ranges from 1.8 to 5.5V
  - Power-on and Power-down reset (POR/PDR), Brown-out reset (BOR), Programmable voltage detector (PVD)
  - 4 to 24MHz high speed crystal oscillator
  - External 32.768KHz low speed oscillator (with LSE Bypass function)
  - 8MHz factory-trimmed high speed RC oscillator, frequency deviation over full

temperature and voltage range is within ±2.5%

  - Integrated PLL to generate up to 48MHz system clock and support multiple prescaler rate to provide clock sources to bus matrix and peripherals
  - 32.768KHz low speed oscillator, frequency deviation over full temperature and voltage range is within ±2.5%
- Low power
  - Several low-power modes, including Lower Power Run, Sleep, Low Power Sleep, Stop, Deep Stop, Standby and Shutdown modes
- One DMA controller with 5 channels to support peripherals including timers, ADC, UART, LPUART, I2C, SPI, and SLCD
- Total 9 timers:
  - Two 16-bit general purpose timers (TIM3 / TIM4), with up to four input capture or output compare channels and can be used for infrared decode
  - Two 16-bit basic timers (TIM16 / TIM17), with one input capture or output compare channel and one complementary output, support hardware dead-time insertion, emergency brake when fault detected, and integrated modulator circuit for infrared control
  - One low power timer (LPTIMER), able to wake up CPU in all modes except for Standy and Shutdown mode
  - Two watchdog timers, including one independent watchdog (IWDG) and one window watchdog (WWDG)
  - One RTC real-time clock, support calendar function
  - One 24-bit Systick timer
- Up to 57 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All I/O ports can accept input or generate output signal voltage level lower than V_{DD}
- Up to 6 communication interfaces:
  - Two UART
  - One low power UART (LPUART)
  - One I2C
  - Two SPI (support I2S mode)
- One Infra-Red Modulator (IRM), supports ASK/PSK/FSK modulation
- One segment LCD driver module (SLCD), which can drive 40x4 or 36x8 segments
- One 12-bit Analog-to-Digital converter (ADC), support 1μs conversion duration, with up to 15 external inputs and 1 internal inputs
  - Conversion range: 0 to V_{DDA}
  - Configurable sampling cycles and resolution
  - On-chip temperature sensor

  - On-chip voltage sensor
- One analog comparator
- Embedded CRC engine, supports 8/16/32-bit configurable polynomial
- 96bit unique chip ID (UID)
- Debug mode
  - Serial-debug-interface (SWD)
- Available in LQFP64 and LQFP48 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers / Features		MM32L0131 C6P/C7P	MM32L0136 C6P/C7P
CPU frequency		48 MHz	
Flash - KB		64	64
SRAM - KB		8	8
Timers	16-bit GP	2	2
	Basic	2	2
	Low power	1	1
Interfaces	UART	2	2
	LPUART	1	1
	I2C	1	1
	SPI/I2S	2	2
GPIO		41/57	41/57
SLCD		-	4x40 or 8x36 (LQFP64) 4x24 or 8x20 (LQFP48)
IRM		√	√
12-bit ADC	Modules	1	1
	Channels	11/15	11/15
Comparator		1	1
RTC		√	√
Supply voltage		1.8V ~ 5.5V	
Temperature range		-40°C ~ +85°C	
Package		LQFP48/64	LQFP48/64

2.2 Marking information

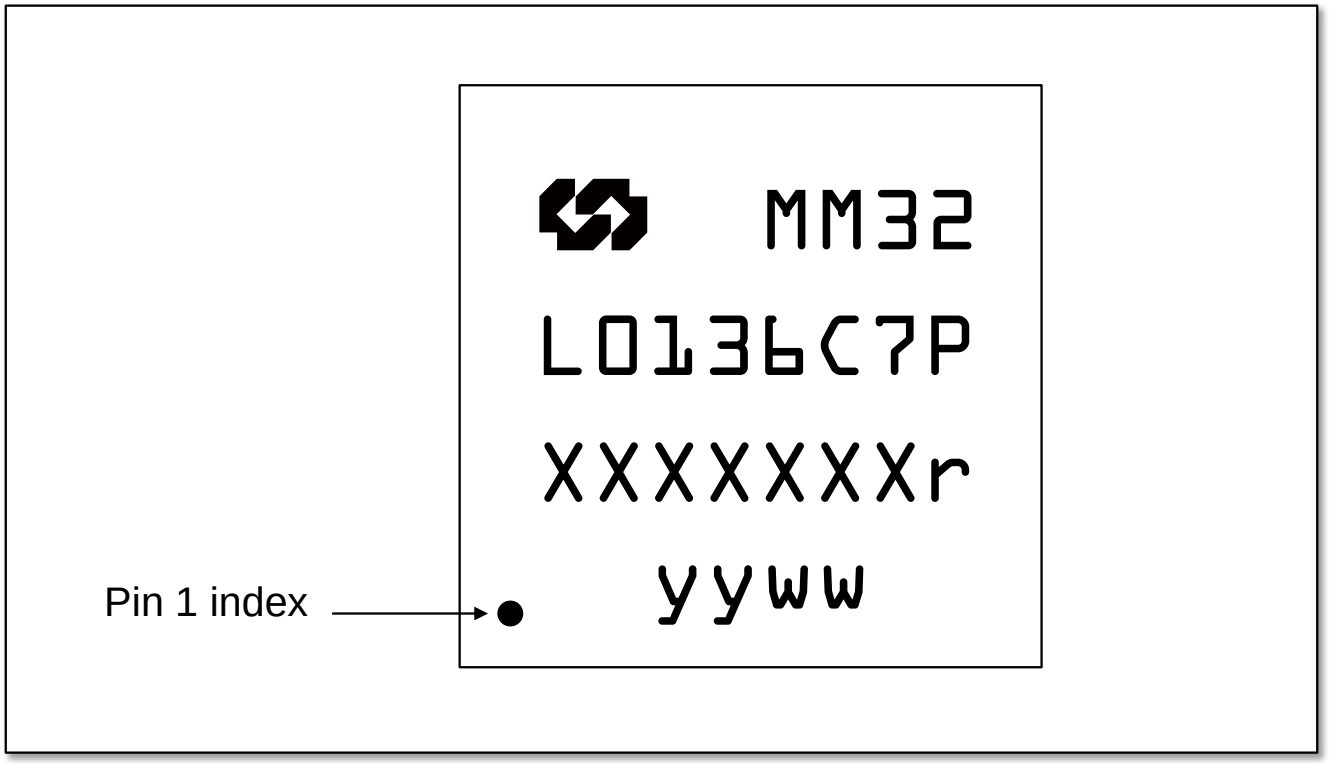

Figure 2-1 LQFP package marking

LQFP package has the following topside marking:

- 1st line: MM32
  - Company logo + first part of product name.
- 2nd line: L013xxxx
  - Second part of product name.
- 3rd line: XXXXXXXr
  - Trace code + revision code, the “r” means chip revision.
- 4th line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

3 Functional description

3.1 Block diagram

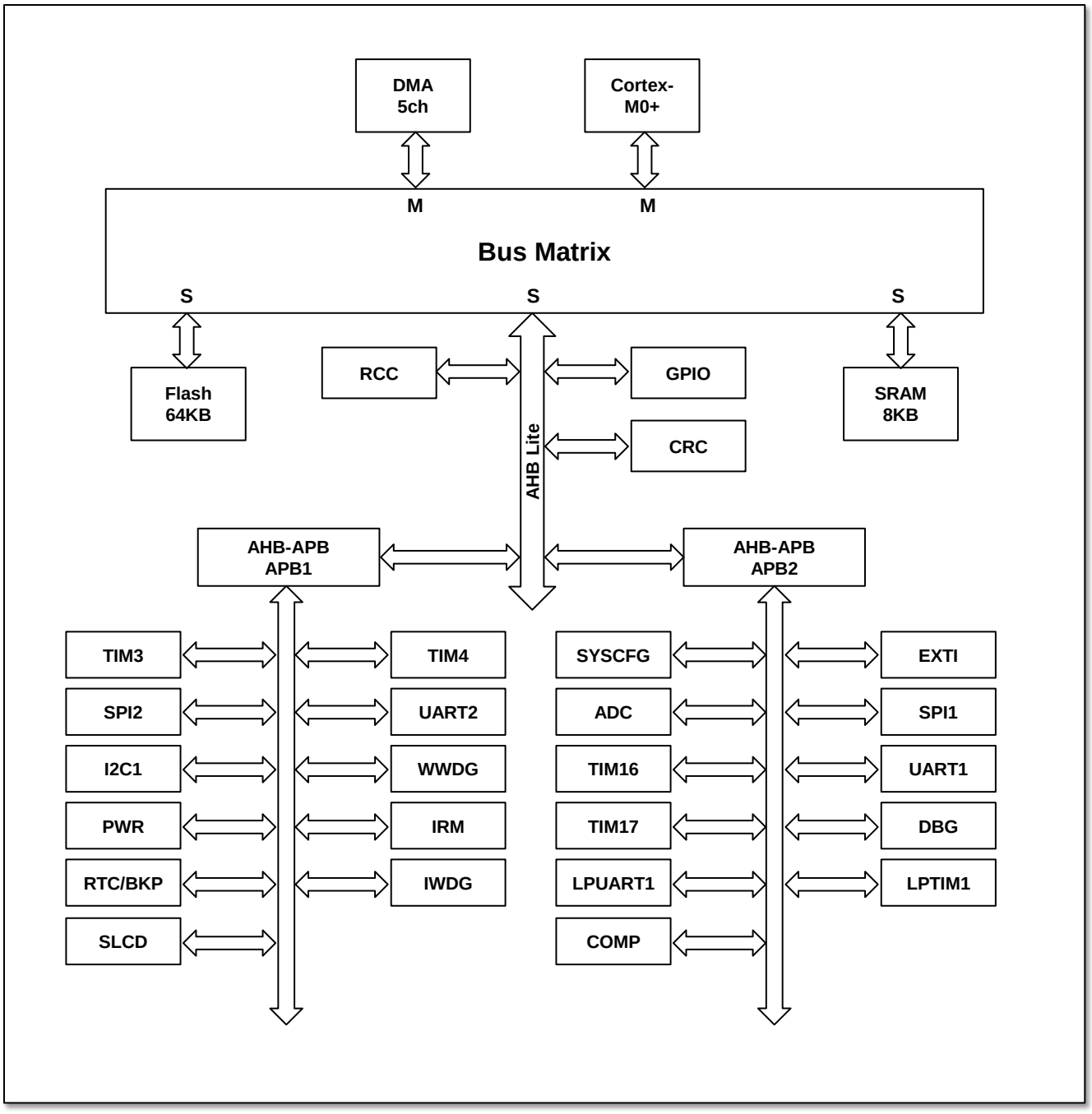

Figure 3-1 System block diagram

3.2 Core introduction

The Arm® Cortex®-M0+ processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The Arm® Cortex®-M0+ is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded Arm core, this product is compatible with all the tools and software for Arm-based products.

3.3 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.4 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x0000 0000 - 0x0000 FFFF	64 KB	Map to main Flash, system memory or SRAM according to boot configuration
	0x0000 0000 - 0x07FF FFFF	~128 MB	Reserved
	0x0800 0000 - 0x0800 FFFF	64 KB	Main Flash
	0x0801 0000 - 0x1FFD FFFF	~383 MB	Reserved
	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 - 0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000 - 0x1FFE 15FF	1.5 KB	Encrypted area
	0x1FFE 1600 - 0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5KB	Option bytes
	0x1FFF FA00 - 0x1FFF FFFF	1.5KB	Reserved
SRAM	0x2000 0000 - 0x2000 1FFF	8 KB	SRAM
	0x2000 2000 - 0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000 – 0x4000 03FF	1 KB	Reserved
	0x4000 0400 – 0x4000 07FF	1 KB	TIM3
	0x4000 0800 – 0x4000 0BFF	1 KB	TIM4

Bus	Address range	Size	Peripheral
	0x4000 0C00 – 0x4000 27FF	7 KB	Reserved
	0x4000 2800 – 0x4000 2BFF	1 KB	RTC/BKP
	0x4000 2C00 – 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 – 0x4000 33FF	1 KB	IWDG
	0x4000 3400 – 0x4000 37FF	1 KB	Reserved
	0x4000 3800 – 0x4000 3BFF	1 KB	SPI2
	0x4000 3C00 – 0x4000 43FF	2 KB	Reserved
	0x4000 4400 – 0x4000 47FF	1 KB	UART2
	0x4000 4800 – 0x4000 53FF	3 KB	Reserved
	0x4000 5400 – 0x4000 57FF	1 KB	I2C1
	0x4000 5800 – 0x4000 6FFF	1 KB	Reserved
	0x4000 7000 – 0x4000 73FF	1 KB	PWR
	0x4000 7400 – 0x4000 8FFF	1 KB	Reserved
	0x4000 9000 – 0x4000 93FF	1 KB	IRM
	0x4000 9400 – 0x4000 97FF	1 KB	LCD
	0x4000 9800 – 0x4000 FFFF	26 KB	Reserved
APB2	0x4001 0000 – 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 – 0x4001 07FF	1 KB	EXTI
	0x4001 0800 – 0x4001 0BFF	1 KB	LPUART1
	0x4001 0C00 – 0x4001 23FF	6 KB	Reserved
	0x4001 2400 – 0x4001 27FF	1 KB	ADC
	0x4001 2800 – 0x4001 2BFF	1 KB	LPTIM1
	0x4001 2C00 – 0x4001 2FFF	1 KB	Reserved
	0x4001 3000 – 0x4001 33FF	1 KB	SPI1
	0x4001 3400 – 0x4001 37FF	1 KB	DBG
	0x4001 3800 – 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 – 0x4001 3FFF	1 KB	COMP
	0x4001 4000 – 0x4001 43FF	1 KB	Reserved
	0x4001 4400 – 0x4001 47FF	1 KB	TIM16
	0x4001 4800 – 0x4001 4BFF	1 KB	TIM17
	0x4001 4C00 – 0x4001 FFFF	45 KB	Reserved
AHB	0x4002 0000 – 0x4002 03FF	1KB	DMA
	0x4002 0400 – 0x4002 0FFF	3KB	Reserved
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 1400 – 0x4002 1FFF	3KB	Reserved
	0x4002 2000 – 0x4002 23FF	1KB	Flash Interface
	0x4002 2400 – 0x4002 2FFF	3KB	Reserved
	0x4002 3000 – 0x4002 33FF	1KB	CRC

Bus	Address range	Size	Peripheral
	0x4002 3400 – 0x47FF FFFF	~128MB	Reserved

3.5 Flash

This product provides up to 64KB embedded Flash memory available for storing code and data.

3.6 SRAM

This product provides up to 8KB embedded SRAM.

3.7 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0+) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.8 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB2 clock period.

3.9 Clock and boot

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator

when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 48MHz. Figure 3-2 shows the clock tree architecture.

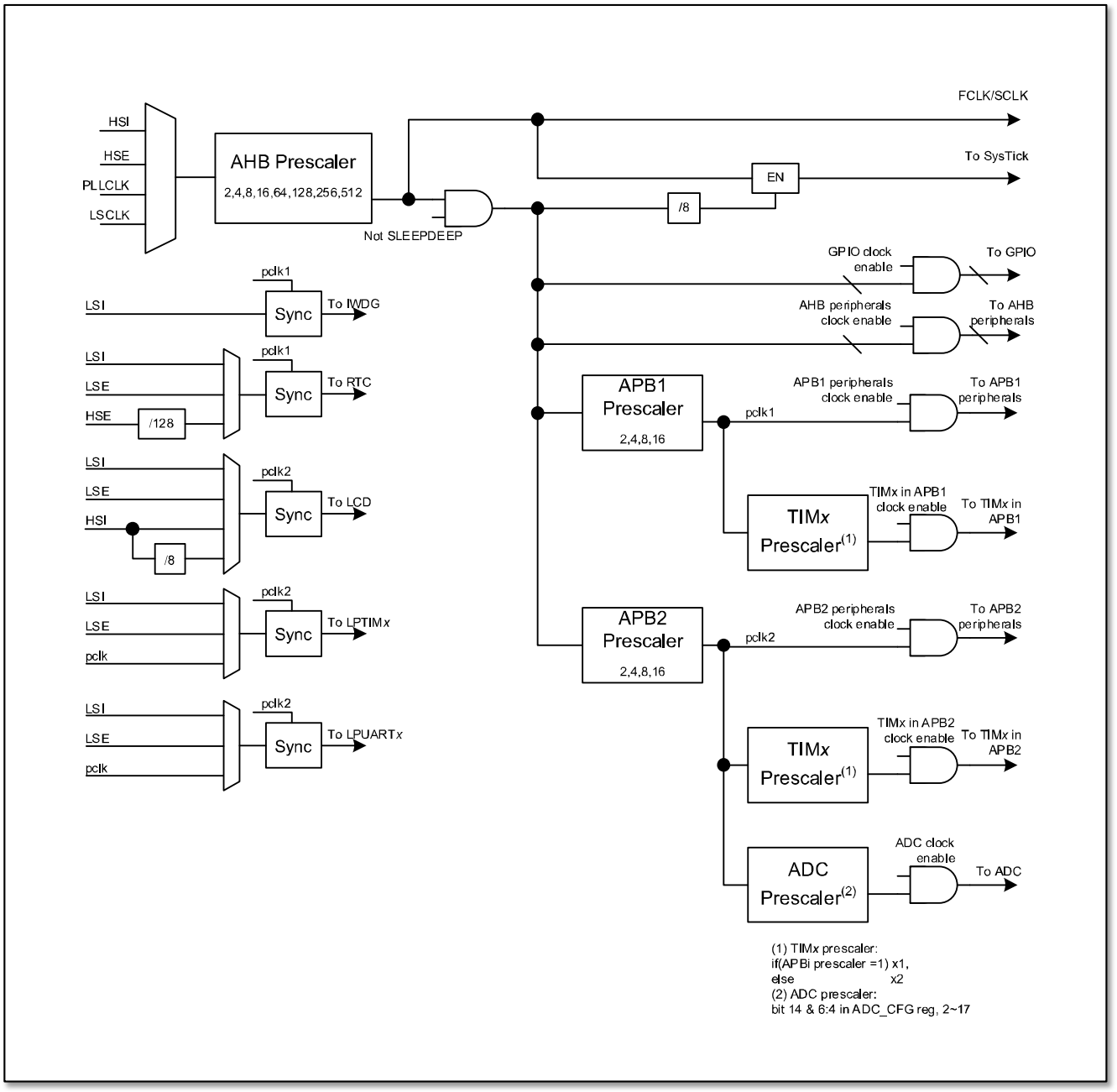

Figure 3-2 Clock tree

3.10 Boot modes

During boot, BOOT0 pins and BOOT bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory

- Boot from embedded SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.11 Power supply schemes

- V_{DD} = 1.8V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 1.8V ~ 5.5V(1): ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.

1. Note: only when V_{DDA} = 2.5V ~ 5.5V, the analog performance is guaranteed to be consistent with this Data Sheet.

3.12 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

3.13 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.14 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Low power run mode

The Low Power Run mode is enabled through the VCORE provided by the low-power

voltage regulator to minimize the operating current of the regulator. This code is executed from the SRAM or Flash and the CPU frequency is limited to 2MHz.

Sleep mode

In the Sleep mode, only the CPU stops working. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Low power sleep mode

The system enters the mode from the Low Power Run mode. Only the CPU stops working. The system returns to the Low Power Run mode when it is woken up by an event or an interrupt.

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers.

The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the signals configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Deep stop mode

This mode has the same status as the Stop mode, although less power is consumed.

Standby mode

The Standby mode allows to achieve the lowest power consumption. It is based on the CPU deep sleep mode, with the voltage regulator disabled. The entire 1.5V power supply domain is disconnected. PLL, HSI and HSE oscillators are also turned off. The device exits Standby mode when a rising edge on the WKUP pin, an external reset of NRST pin, or an IWDG reset occurs. The device also can be woken up and reset by the watchdog timer. After entering the Standby mode, the contents of SRAM and registers will be lost. Only backup registers and standby circuits remain powered.

Shutdown mode

The lowest system power consumption is achieved in shutdown mode. In shutdown mode, all internal voltage regulators are turned off, BOR is turned off, and only POR and a few other V_{DD} domain circuits are left to work normally (PMU part logic/POR/IO Wakeup logic).

3.15 DMA

This product has a 5-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

DMA can be used for peripherals include UART, I2C, SCLD, SPI, ADC, and timers.

3.16 Timers and watchdogs

This product has two general purpose timers, two basic timers, one low power timer, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 3-2 Feature summary of timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
General purpose	TIM3/TIM4	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM16/TIM17	16-bit	up, down, up/down	1 to 65536	Yes	1	Yes
Low power	LPTIM1	16-bit	up	Any integer between 1 ~ 128	Yes	No	No

General-purpose timer (TIM3 / TIM4)

This product has two general-purpose timers (TIM3, TIM4). The timer has a 16-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function. In debug mode, the counter stops counting, and PWM output will be disabled. Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

Basic timer (TIM16 / TIM17)

This product has two basic timers (TIM16, TIM17). Each timer is composed of one 16-bit auto-load up/down counter, one 16-bit prescaler and one independent channel, each channel can be used for input capture, output compare, PWM and single pulse output. When work as PWM mode, this timer has a complementary output port, which can generate complementary PWM pair, supports hardware dead-time insertion function.

Low-power timer (LPTIM1)

This product has one 16-bit low power timer (LPTIM1). LPTIM consists of a 16-bit

counter that provides users with convenient count timing. LPTIM features low power and can work under multiple low-power modes. Without internal clock running, it can work with external clock running and achieve external pulse counting in sleep mode. It can also achieve low-power timeout wake-up through external input trigger signals. LPTIM has multiple features such as external clock count, timeout wake-up and PWM output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40KHz internal clock oscillator and as it operates independently from the main clock, it can operate in Shutdown and Standby modes. It can be used to either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog has a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the entire system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.17 Real-time clock (RTC)

Real-time clock (RTC) is an independent timer, supports hardware calendar function.

3.18 Backup register

The backup register is composed of 10 16-bit registers used to store user application data located in the backup area. They are not reset by a system or power reset, or when the system wakes up from Standby mode.

3.19 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open drain), as input (with/without pull-up/pull-down) or as peripheral alternate function port. Most GPIO

pins are shared with digital or analog alternate peripherals.

The peripheral function of the I/O pin can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.20 UART

This product has up to two UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. All UART interfaces support DMA operation.

3.21 LPUART

This product has one low power UART (LPUART) interface. Compared with UART, it has an extremely low power consumption, and can run and wake up chip in the Sleep and Deep sleep mode. LPUART can be configured to support multiple commonly used baud rate.

3.22 I2C

This product has up to one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard and fast mode. The I2C interface supports 7-bit or 10-bit addressing.

3.23 SPI

This product has up to two SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 12 Mbps in master mode and 6 Mbps in slave mode. All SPI interfaces support DMA operation.

3.24 I2S

This product has up to two I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.25 Infra-Red Modulator (IRM)

This product has one Infra-Red Modulator (IRM) module. The IRM module uses the

on-chip timer and serial port to realize ASK/PSK/FSK modulation of data to meet the needs of infra-red code transmission.

3.26 Segment LCD driver (SLCD)

This product has built-in segment LCD driver (SLCD), the specific functions are as follows:

- Capable to drive 40x4 or 36x8 segments
- Any LCD pin can be configured as COM or SEG function
- Built-in charge pump to keep the LCD clear when the supply voltage drops
- Supports static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycles
- Configurable 1/2, 1/3, 1/4 bias voltage
- Adjustable contrast
- Flexible control of display frame rate
- Built-in 16*32bit display data register to store display data
- Support blinking function, can be configured to blink 1 to 8 segments or all segments, configurable 0.5Hz/1Hz/2Hz/4Hz frequency
- Workable in all low power modes except Shutdown mode

3.27 ADC

This product has one 12-bit analog/digital converter (ADC), with up to 15 external channels available, supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

3.28 COMP

The device embeds two comparators that can work either standalone (all terminals are available on I/Os) or together with the timers. COMP can be used as follows:

- Trigger low-power mode wake-up event by the analog signal

- Adjust the analog signal
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Reusable I/O pin
  - Internal comparison voltage CRV can be division voltage value of V_{DDA} or internal reference voltage
- Programmable hysteresis voltage
- Programmable speed and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminal, which can trigger the following events:
  - Capture event
- Break event of rapidly turning off PWM

3.29 CRC

This product has one CRC calculation unit, supports 8/16/32-bit configurable polynomial.

3.30 SWD

This product equips Arm standard two-wire serial debug interface (SWD)

4 Pinout and assignment

4.1 Pinout diagram

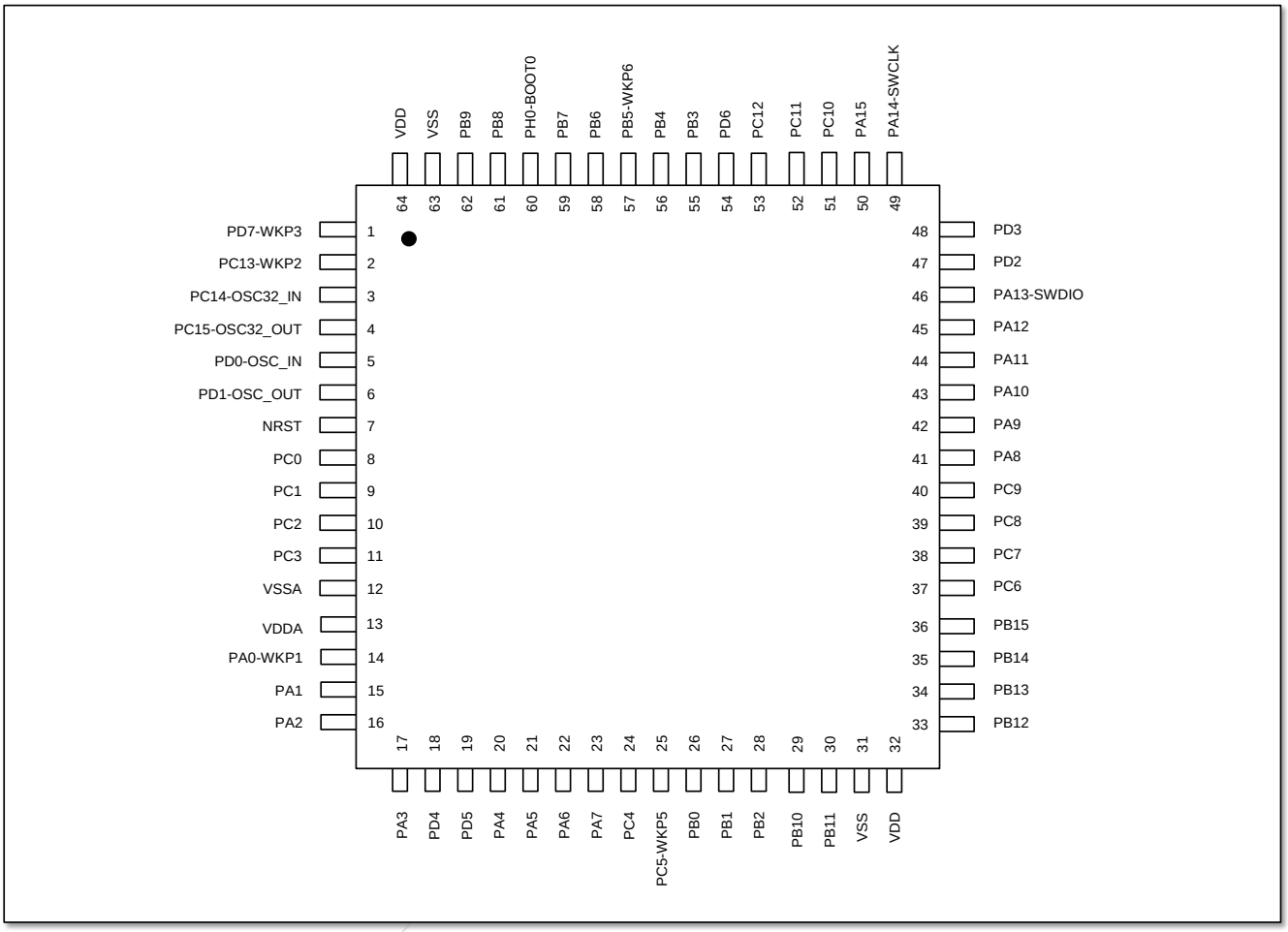

Figure 4-1 LQFP64 pinout diagram

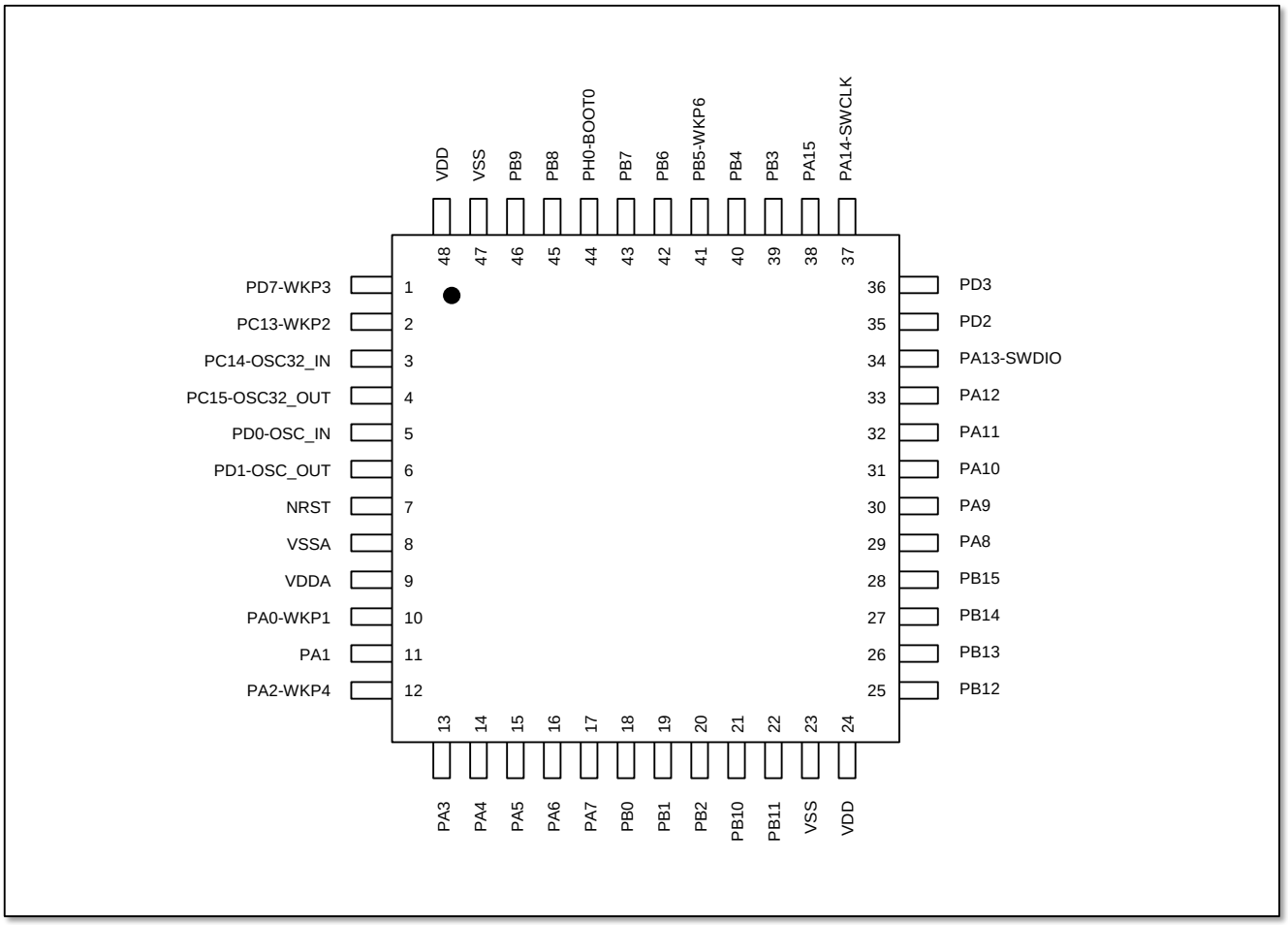

Figure 4-2 LQFP48 pinout diagram

4.2 Pin assignment

Table 4-1Pin assignment table

Pin ID		Name	Type(1)	I/O level(2)	Main function	Multiplex function	LCD function	Additional function
LQFP 64	LQFP 48							
1	1	PD7	I/O	TC	PD7	TIM3_CH1 TIM4_CH4 TIM17_CH1	L1	WKP3
2	2	PC13	I/O	TC	PC13	TIM4_CH1/TIM4_ETR	L0	WKP2 RTC_TAMP1 RTC_TS RTC_OUT(3)
3	3	PC14	I/O	TC	PC14	TIM4_CH2	-	-
4	4	PC15	I/O	TC	PC15	TIM4_CH3	-	-
5	5	PD0	I/O	TC	PD0	I2C1_SDA UART1_TX SPI1_MOSI/I2S1_SD	-	-
6	6	PD1	I/O	TC	PD1	I2C1_SCL UART1_RX SPI1_MISO/I2S1_MCK	-	-
7	7	NRST	NRST	-	NRST	-	-	-
8	-	PC0	I/O	TC	PC0	EVENTOUT LPUART1_TX	L43	-
9	-	PC1	I/O	TC	PC1	EVENTOUT LPUART1_RX	L42	-
10	-	PC2	I/O	TC	PC2	EVENTOUT SPI2_MISO/I2S2_MCK LPTIM1_TRIGGER	L41	-
11	-	PC3	I/O	TC	PC3	EVENTOUT SPI2_MOSI/I2S2_SD LPTIM1_OUT	L40	-
12	8	VSSA	S	-	VSSA	-	-	-
13	9	VDDA	S	-	VDDA	-	-	-
14	10	PA0	I/O	TC	PA0	UART2_CTS TIM4_CH1/TIM4_ETR UART1_RX CPT1_OUT	L39	WKP1 TAMP2
15	11	PA1	I/O	TC	PA1	UART2_RTS TIM4_CH2 UART1_TX	L38	-
16	12	PA2	I/O	TC	PA2	UART2_TX TIM4_CH3	L37	WKP4
17	13	PA3	I/O	TC	PA3	UART2_RX TIM4_CH4	L36	-
18	-	PD4	I/O	TC	PD4	SPI1_MISO/I2S1_MCK	L35	-
19	-	PD5	I/O	TC	PD5	SPI1_MOSI/I2S1_SD	L34	-
20	14	PA4	I/O	TC	PA4	SPI1_NSS/I2S1_WS LPUART1_TX TIM16_CH1N	L33	-
21	15	PA5	I/O	TC	PA5	SPI1_SCK/I2S1_CK TIM4_CH1/TIM4_ETR LPUART1_RX TIM17_CH1N	L32	-
22	16	PA6	I/O	TC	PA6	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM16_CH1 EVENTOUT CPT1_OUT	L31	-

Pin ID		Name	Type(1)	I/O level(2)	Main function	Multiplex function	LCD function	Additional function
LQFP 64	LQFP 48							
23	17	PA7	I/O	TC	PA7	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM17_CH1 EVENTOUT	L30	-
24	-	PC4	I/O	TC	PC4	EVENTOUT UART2_TX TIM3_CH1 SPI1_MOSI/I2S1_SD	L29	-
25	-	PC5	I/O	TC	PC5	UART2_RX TIM3_CH2 SPI1_MISO/I2S1_MCK	L28	WKP5
26	18	PB0	I/O	TC	PB0	TIM3_CH3	L27	-
27	19	PB1	I/O	TC	PB1	TIM3_CH4	L26	-
28	20	PB2	I/O	TC	PB2	EVENTOUT	L25	-
29	21	PB10	I/O	TC	PB10	TIM4_CH3 I2C1_SCL SPI2_SCK/I2S2_CK	L24	-
30	22	PB11	I/O	TC	PB11	EVENTOUT TIM4_CH4 I2C1_SDA	L23	-
31	23	VSS_1	S	-	VSS_1	-	-	-
32	24	VDD_1	S	-	VDD_1	-	-	-
33	25	PB12	I/O	TC	PB12	SPI2_NSS/I2S2_WS EVENTOUT	L22	-
34	26	PB13	I/O	TC	PB13	SPI2_SCK/I2S2_CK LPTIM1_TRIGGER I2C1_SCL TIM17_CH1	L21	-
35	27	PB14	I/O	TC	PB14	SPI2_MISO/I2S2_MCK RTC_OUT (4) LPTIM1_OUT I2C1_SDA	L20	-
36	28	PB15	I/O	TC	PB15	SPI2_MOSI/I2S2_SD	L19	-
37	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM3_CH3 SPI1_NSS/I2S1_WS	L18	-
38	-	PC7	I/O	TC	PC7	TIM3_CH2 SPI1_SCK/I2S1_CK	L17	-
39	-	PC8	I/O	TC	PC8	TIM3_CH3	L16	-
40	-	PC9	I/O	TC	PC9	TIM3_CH4	L15	-
41	29	PA8	I/O	TC	PA8	MCO RTC_OUT (4)	L14	-
42	30	PA9	I/O	TC	PA9	UART1_TX I2C1_SCL MCO IROUT	L13	-
43	31	PA10	I/O	TC	PA10	TIM17_BKIN1 UART1_RX I2C1_SDA TIM16_CH1 IROUT	L12	-
44	32	PA11	I/O	TC	PA11	UART1_CTS I2C1_SCL CPT1_OUT	L11	-
45	33	PA12	I/O	TC	PA12	UART1_RTS I2C1_SDA	L10	-

Pin ID		Name	Type(1)	I/O level(2)	Main function	Multiplex function	LCD function	Additional function
LQFP 64	LQFP 48							
46	34	PA13	I/O	TC	PA13	SWDIO UART1_TX	-	-
47	35	PD2	I/O	TC	PD2	I2C1_SCL SPI1_NSS/I2S1_WS	L9	-
48	36	PD3	I/O	TC	PD3	I2C1_SDA SPI1_MISO/I2S1_MCK	L8	-
49	37	PA14	I/O	TC	PA14	SWCLK UART2_TX UART1_RX	-	-
50	38	PA15	I/O	TC	PA15	SPI1_NSS/I2S1_WS UART2_RX TIM4_CH1/TIM4_ETR SPI2_SCK/I2S2_CK	L7	-
51	-	PC10	I/O	TC	PC10	UART1_TX SPI2_MISO/I2S2_MCK	L6	-
52	-	PC11	I/O	TC	PC11	UART1_RX SPI2_MOSI/I2S2_SD	L5	-
53	-	PC12	I/O	TC	PC12	UART1_TX SPI2_NSS/I2S2_WS	L4	-
54	-	PD6	I/O	TC	PD6	TIM3_ETR	V4/L58	-
55	39	PB3	I/O	TC	PB3	SPI1_SCK/I2S1_CK TIM4_CH2	V3/L59	-
56	40	PB4	I/O	TC	PB4	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM17_BKIN2	V2/L60	-
57	41	PB5	I/O	TC	PB5	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM16_BKIN1	V1/L61	WKP6
58	42	PB6	I/O	TC	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM4_CH1	LCDCAP2/L62	-
59	43	PB7	I/O	TC	PB7	UART1_RX I2C1_SDA TIM17_CH1N TIM4_CH2	LCDCAP1/L63	-
60	44	PH0	I/O	TC	PH0	-	-	BOOT0
61	45	PB8	I/O	TC	PB8	LPUART1_RX I2C1_SCL TIM16_CH1 TIM4_CH3 IROUT	L3	-
62	46	PB9	I/O	TC	PB9	LPUART1_TX I2C1_SDA TIM17_CH1 EVENTOUT SPI2_NSS/I2S2_WS TIM4_CH4	L2	-
63	47	VSS_3	S	-	VSS_3	-	-	-
64	48	VDD_3	S	-	VDD_3	-	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.
3. RTC_OUT from RTC domain
4. RTC_OUT from core domain

4.3 Pin multiplexing

Table 4-2 PA PA port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM4_CH1/TIM4_ETR	-	-	-	UART1_RX	CPT1_OUT
PA1	-	UART2_RTS	TIM4_CH2	-	-	-	UART1_TX	-
PA2	-	UART2_TX	TIM4_CH3	-	-	-	-	-
PA3	-	UART2_RX	TIM4_CH4	-	-	-	-	-
PA4	SPI1_NSS/I2S1_WS	-	-	LPUART1_TX	-	TIM16_CH1N	-	-
PA5	SPI1_SCK/I2S1_CK	-	TIM4_CH1/TIM4_ETR	LPUART1_RX	-	TIM17_CH1N	-	-
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	-	TIM16_CH1	EVENTOUT	CPT1_OUT
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	-	-	-	TIM17_CH1	EVENTOUT	-
PA8	MCO	-	RTC_OUT(2)	-	-	-	-	-
PA9	-	UART1_TX	-	-	I2C1_SCL	MCO	-	IROUT
PA10	TIM17_BKIN1	UART1_RX	-	-	I2C1_SDA	-	TIM16_CH1	IROUT
PA11	-	UART1_CTS	-	-	-	I2C1_SCL	-	CPT1_OUT
PA12	-	UART1_RTS	-	-	-	I2C1_SDA	-	-
PA13	SWDIO	-	-	UART1_TX	-	-	-	-
PA14	SWCLK	UART2_TX	-	UART1_RX	-	-	-	-
PA15	SPI1_NSS/I2S1_WS	UART2_RX	TIM4_CH1/TIM4_ETR	SPI2_SCK/I2S2_CK	-	-	-	-

Table 4-3 PB port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	-	-	-	-	-	-
PB1	-	TIM3_CH4	-	-	-	-	-	-
PB2	-	-	EVENTOUT	-	-	-	-	-
PB3	SPI1_SCK/I2S1_CK	-	TIM4_CH2	-	-	-	-	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	-	TIM17_BKIN2	-	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN1	-	-	-	-	-
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	TIM4_CH1	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM4_CH2	-
PB8	LPUART1_RX	I2C1_SCL	TIM16_CH1	-	-	-	TIM4_CH3	IROUT
PB9	LPUART1_TX	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS/I2S2_WS	TIM4_CH4	-
PB10	-	-	TIM4_CH3	I2C1_SCL	-	SPI2_SCK/I2S2_CK	-	-
PB11	EVENTOUT	-	TIM4_CH4	I2C1_SDA	-	-	-	-
PB12	SPI2_NSS/I2S2_WS	-	-	EVENTOUT	-	-	-	-
PB13	SPI2_SCK/I2S2_CK	-	-	LPTIM1_TRIGGER	-	I2C1_SCL	TIM17_CH1	-
PB14	SPI2_MISO/I2S2_MCK	-	RTC_OUT(2)	LPTIM1_OUT	-	I2C1_SDA	-	-
PB15	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-

Table 4-4 PC port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	LPUART1_TX	-	-	-	-	-
PC1	EVENTOUT	-	LPUART1_RX	-	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I2S2_MCK	-	LPTIM1_TRIGGER	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I2S2_SD	-	LPTIM1_OUT	-	-	-	-
PC4	EVENTOUT	-	-	UART2_TX	-	TIM3_CH1	SPI1_MOSI/I2S1_SD	-
PC5	-	-	-	UART2_RX	-	TIM3_CH2	SPI1_MISO/I2S1_MCK	-
PC6	TIM3_CH1	-	-	-	-	TIM3_CH3	SPI1_NSS/I2S1_WS	-
PC7	TIM3_CH2	-	-	-	-	-	SPI1_SCK/I2S1_CK	-
PC8	TIM3_CH3	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-
PC10	-	-	UART1_TX	SPI2_MISO/I2S2_MCK	-	-	-	-
PC11	-	-	UART1_RX	SPI2_MOSI/I2S2_SD	-	-	-	-
PC12	-	-	UART1_TX	SPI2_NSS/I2S2_WS	-	-	-	-
PC13	-	-	-	-	-	-	TIM4_CH1/TIM4_ETR	-
PC14	-	-	-	-	-	-	TIM4_CH2	-
PC15	-	-	-	-	-	-	TIM4_CH3	-

Table 4-5 PD port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	-	UART1_TX	-	SPI1_MOSI/I2S1_SD	-	-
PD1	-	I2C1_SCL	-	UART1_RX	-	SPI1_MISO/I2S1_MCK	-	-
PD2	-	I2C1_SCL	-	-	-	-	SPI1_NSS/I2S1_WS	-
PD3	-	I2C1_SDA	-	-	-	-	SPI1_MISO/I2S1_MCK	-
PD4	SPI1_MISO/I2S1_MCK	-	-	-	-	-	-	-
PD5	SPI1_MOSI/I2S1_SD	-	-	-	-	-	-	-
PD6	TIM3_ETR	-	-	-	-	-	-	-
PD7	-	-	-	-	-	TIM3_CH1	TIM4_CH4	TIM17_CH1

Table 4-6 PH port multiplexing AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PH0	-	-	-	-	-	-	-	-

5 Package dimensions

5.1 LQFP64

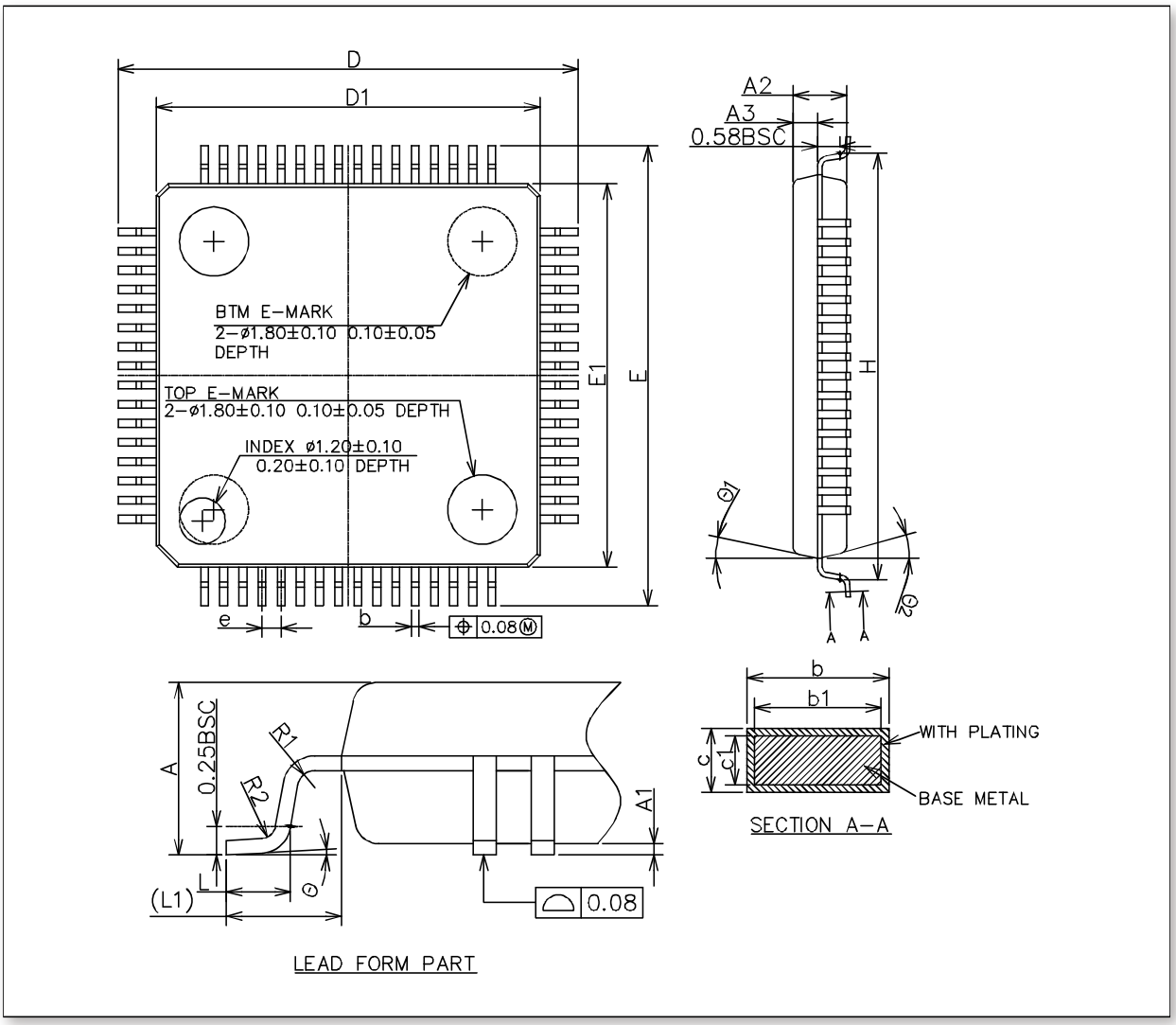

Figure 5-1 LQFP64 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-1 LQFP64 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

5.2 LQFP48

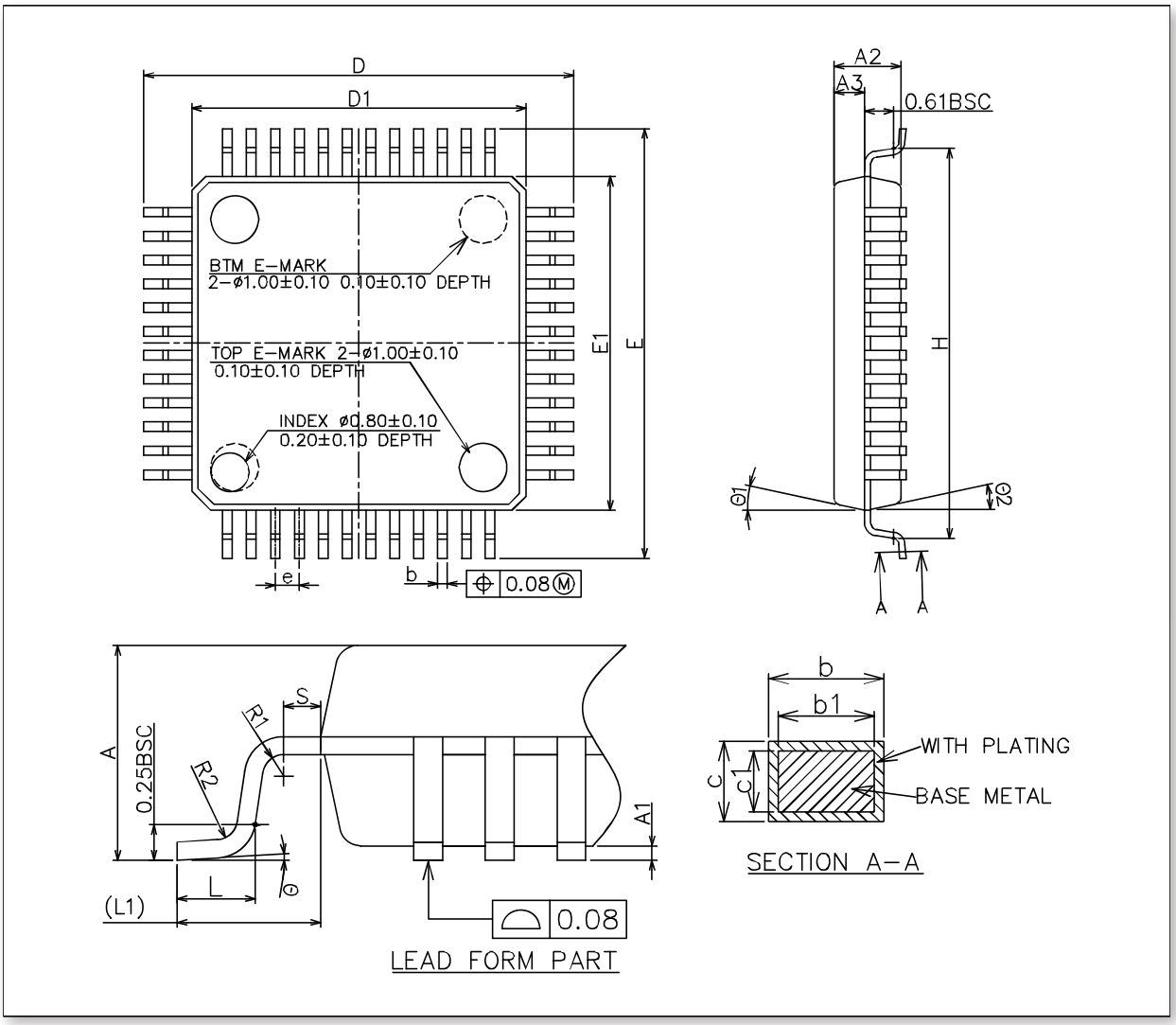

Figure 5-2 LQFP48 package dimension

1. The figure is not drawn to scale.
2. Dimensions are in millimeters.

Package dimensions

Table 5-2 LQFP48 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

6 Part identification

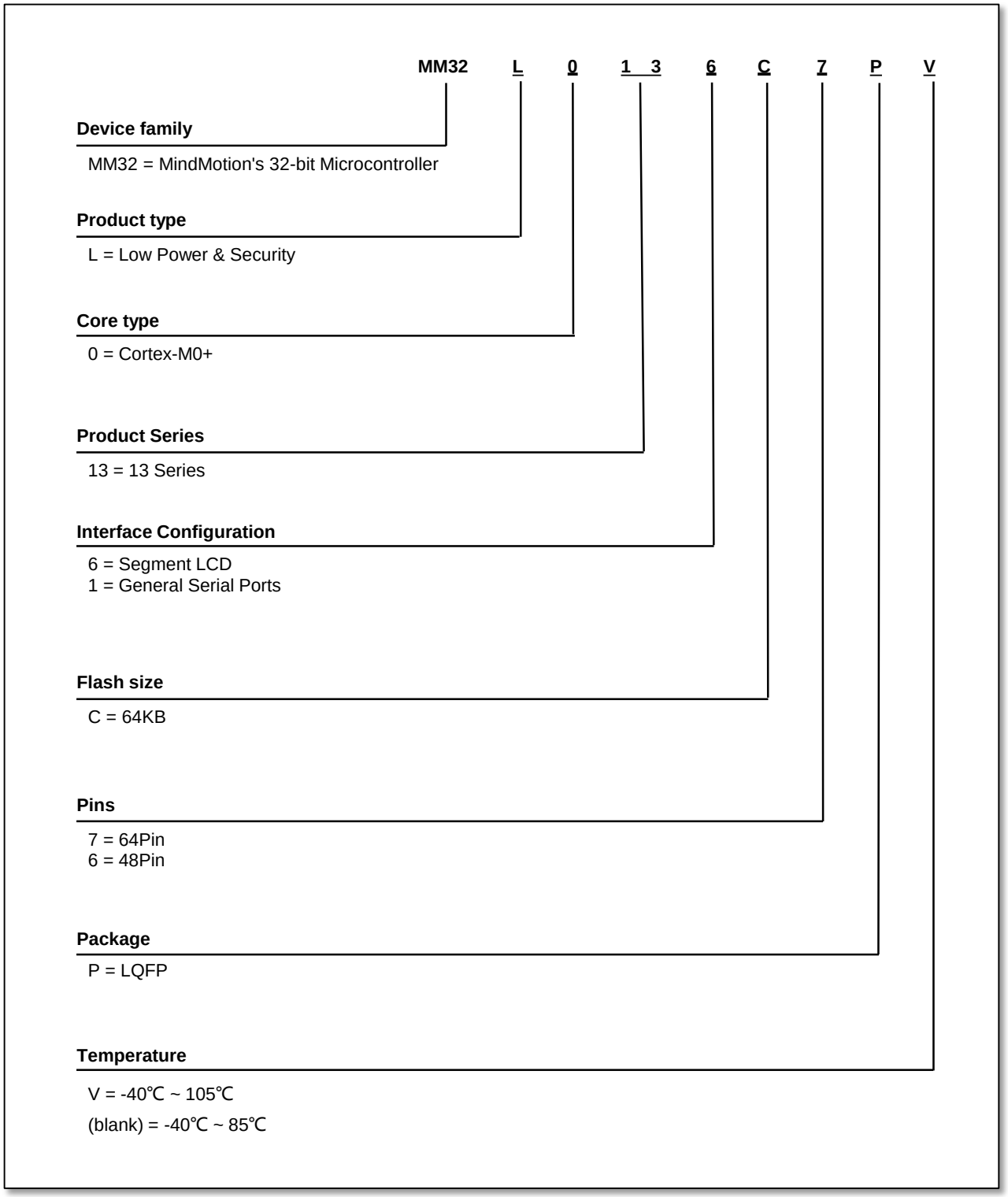

Figure 6-1 Part number naming rule

7 Revision history

Date	Revision	Description
2021/09/07	Rev1.0	Initial release